DATA SHEET

Si3218x: ProSLIC® Single-Channel Foreign Exchange Subscriber (FXS) Solutions

Applications

- VoIP gateways and routers
- xDSL Integrated Access Devices (IADs)
- Optical Network Terminals/Units (ONTs/ONUs)
- Analog Terminal Adapters (ATAs)
- Cable embedded Multimedia Terminal Adapter (eMTA)
- Wireless Fixed Terminals (WFTs)
- Wireless Local Loop (WLL)
- WiMAX® Customer Premises Equipment (CPE)

Features

- Complete Foreign Exchange Station (FXS) solution in a 6 x 6 mm package
- Performs all Battery feed, Over-voltage protection, Ringing, Signaling, Coding, Hybrid, and Test (BORSCHT) functions
- Ideal for short to medium loops
- Global programmability
- Patented low-power ringing
- Simplified configuration and diagnostics
  - Supported by ProSLIC® API
  - Audio diagnostics with loopback
  - Integrated test load
- Ultra low power consumption
- Wideband voice support
- On-hook transmission
- Loop or ground start operation
- Smooth polarity reversal
- A-Law/µ-Law companding, linear PCM
- Flexible integrated tracking dc-to-dc controller supporting patent pending low-cost capacitive boost configuration
- Software-programmable parameters:
  - Ringing frequency, amplitude, cadence, and waveshape
  - Two-wire ac impedance
  - Transhybrid balance
  - DC current loop feed (10 to 45 mA)
  - Loop closure and ring trip thresholds
  - Ground key detect threshold
  - Pulse metering
- DTMF generation
- DTMF detection (Si31285)
- 3.3 V operation
- Support for 1.8 V I/O
- Maximum battery up to –106 V
- PCM/SPI interface
- 40-pin (6 mm x 6 mm) Quad Flat No-lead (QFN) package (MSL3 260 °C per JEDEC J-STD-020)
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.

Description

The Si3218x devices are single-channel ProSLIC products that implement a complete FXS telephony interface solution in accordance with all relevant global specifications.

The Si3218x ProSLIC ICs operate from a 3.3 V supply and interface to a standard PCM/SPI digital interface with 3.3 V or 1.8 V I/O.

The Si3218x integrated dc-to-dc controller automatically generates the optimal battery voltages required for each linestate.

1. Functional Description

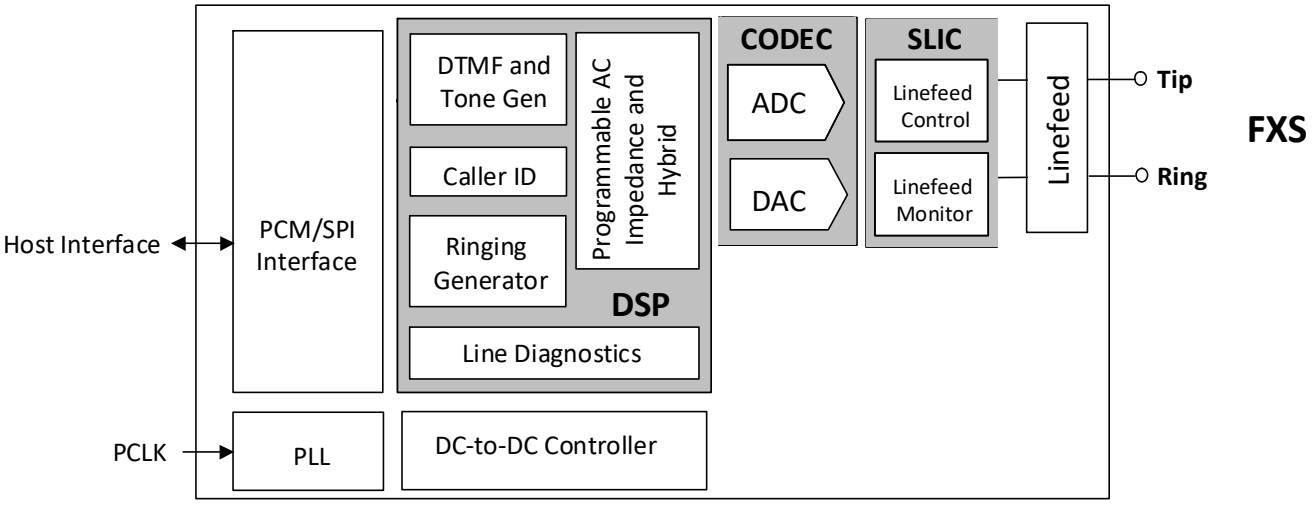

Figure 1. Functional Block Diagram

The Si3218x series provides all SLIC, codec, DTMF detection, and signal generation functions needed for one complete analog telephone interface. The Si3218x performs all BORSCHT functions. It also supports extensive metallic loop and self-test capabilities.

The Si3218x supports wideband audio (150 Hz to 6.8 kHz) compliant with PKT-SP-HDV-104-120823, and is configurable to support the full ITU-T-G.722-201209 bandwidth (50 Hz to 7 kHz). The wideband mode provides an expanded audio band with a 16 kHz sample rate for enhanced audio quality.

The Si3218x series supports a standard PCM/SPI digital interface.

The Si3218x incorporates a programmable dc-to-dc converter controller that reacts to line conditions to provide the optimal battery voltage required for each line-state. Si3218x ICs are available with voltage ratings of –106 V.

Programmable on-hook voltage, programmable off-hook loop current, reverse polarity operation, loop or ground start operation, and on-hook transmission are supported. Loop current and voltage are continuously monitored by an integrated monitoring ADC.

The Si3218x supports low power ringing with or without a programmable dc offset. The available voltage offset, frequency, waveshape, and cadence options are designed to ring the widest variety of terminal devices and to reduce external controller requirements.

A complete audio transmit and receive path is integrated, including ac impedance and hybrid gain. These features are software-programmable, allowing a single hardware design to meet global requirements.

2. Pin Descriptions

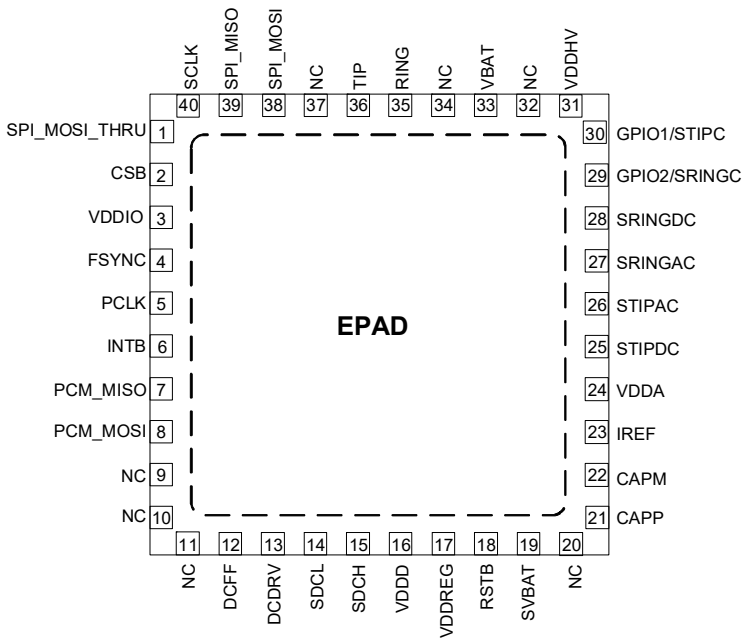

Figure 2. Pinout (Top View)

Table 1. Pin Descriptions

Pin	Name	Description
1	SPI_MOSI_THRU	SPI_MOSI pass through. Cascaded SPI_MOSI signal for daisy chain mode.
2	CSB	Chip select input. Active low. When inactive, SCLK and SPI_MOSI are ignored and SPI_MISO is high impedance. When active, the serial port is operational.
3	VDDIO	Digital I/O supply voltage. 3.3 V or 1.8 V digital power supply for internal circuitry.
4	FSYNC	Frame sync clock input. 8 kHz frame synchronization signal for the PCM bus. May be short or long pulse format.
5	PCLK	PCM bus clock input. Clock input for PCM bus timing.
6	INTB	Interrupt output. Maskable interrupt output. Open drain output for wire-ORed operation.
7	PCM_MISO	Transmit PCM output. PCM master input, slave output. Output data to PCM bus.
8	PCM_MOSI	Transmit PCM input. PCM master output, Slave input. Input data from PCM bus.
9	NC	No connection. This pin should be left unconnected.
10	NC	No connection. This pin should be left unconnected.
11	NC	No connection. This pin should be left unconnected.
12	DCFF	DC-to-dc charge pump output.
13	DCDRV	DC drive, dc-to-dc converter control signal output which drives external transistor.
14	SDCL	DC monitor, dc-to-dc converter monitor input used to detect overcurrent situations in the converter.
15	SDCH	DC monitor, dc-to-dc converter monitor input used to detect overcurrent situations in the converter.
16	VDDD	IC voltage supply. 3.3 V digital power supply for internal circuitry.

Table 1. Pin Descriptions (Continued)

Pin	Name	Description
17	VDDREG	Regulated core power supply.
18	RSTB	Reset input. Active low input. Hardware reset used to place all control registers in the default state.
19	SVBAT	VBAT sense. Input used to sense voltage on dc-to-dc converter output voltage lead.
20	NC	No connection. This pin should be left unconnected.
21	CAPP	SLIC stabilization capacitor. Capacitor used in low pass filter to stabilize SLIC feedback loops.
22	CAPM	SLIC stabilization capacitor. Capacitor used in low pass filter to stabilize SLIC feedback loops.
23	IREF	Current reference input. Connects to an external resistor used to provide a high accuracy reference current.
24	VDDA	Analog supply voltage. Analog 3.3 V power supply for internal analog circuitry.
25	STIPDC	Tip dc sense. Analog dc input used to sense voltage on tip lead.
26	STIPAC	Tip ac sense. Analog ac input used to sense voltage on tip lead.
27	SRINGAC	Ring ac sense. Analog ac input used to sense voltage on ring lead.
28	SRINGDC	Ring dc sense. Analog dc input used to sense voltage on ring lead.
29	SRINGC	Ring coarse sense input. Voltage sensing outside protection circuit.
30	STIPC	Tip coarse sense input. Voltage sensing outside protection circuit.
31	VDDHV	Analog supply voltage. Analog 3.3 V power supply for internal analog circuitry.
32	NC	No connection. This pin should be left unconnected.
33	VBAT	Battery voltage supply. Connect to battery supply from dc-to-dc converter.
34	NC	No connection. This pin should be left unconnected.
35	RING	Ring terminal. Connect to the ring lead of the subscriber loop.
36	TIP	Tip terminal. Connect to the tip lead of the subscriber loop.
37	NC	No connection. This pin should be left unconnected.
38	SPI_MOSI	Serial port data input. SPI master output, slave input. Input control data from Serial Peripheral Interface (SPI) bus.
39	SPI_MISO	Serial port data output. SPI master input, slave output. Output control data to SPI bus.
40	SCLK	Serial port bit clock input. Serial port clock input. Controls the serial data on SPI_MISO and latches the data on SPI_MOSI.

3. Electrical Specifications

Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Value	Unit
Supply voltage	V_{DD}, V_{DDIO}	–0.5 to 4.0	V
Digital input voltage	V_{IND}	–0.3 to 3.6	V
Battery supply voltage	V_{BAT}	+0.4 to –112	V
Tip or ring voltage	V_{TIP}, V_{RING}	V_{BAT} –0.4	V
Tip or ring current	I_{TIP}, I_{RING}	±100	mA

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet.

ESD Handling: *Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.*

Table 3. Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient temperature	T_A	F-grade	0	25	70	°C
		G-grade	–40	25	85	°C
Silicon junction temperature, high voltage die	T_{JHV}	Continuous	–	–	Internally limited	°C
Silicon junction temperature, low voltage die	T_{JLV}	Continuous	–	–	125	°C
Supply voltage	V_{DDD}	–	3.13	3.3	3.47	V
Battery voltage[2]	V_{BAT}	–	–106	–	–15	V
I/O supply voltage	V_{DDIO}	–	1.71	–	3.47	V

1. All minimum and maximum specifications apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C, unless otherwise stated.
2. Minimum and maximum battery voltage limits are dependent upon loop conditions and dc-to-dc converter configuration.

Table 4. Thermal Conditions

Parameter	Symbol	Test Condition	Value	Unit
Storage temperature range	T_{STG}		–55 to 150	°C
Thermal resistance, typical QFN 40[1]	Θ_{JA}		33.8	°C/W
	Θ_{JB}		17.3	°C/W
	Θ_{JC}		20.5	°C/W
Maximum junction temperature, (high voltage die)[2]	T_{JHV}	Continuous	Internally limited	°C
Maximum junction temperature (low voltage die)[3]	T_{JLV}		125	°C

1. The thermal resistance of an exposed pad package is assured when the recommended printed circuit board layout guidelines are followed. The specified performance requires that the exposed pad be soldered to an exposed copper surface of at least equal size and that multiple vias are added to enable heat transfer between the top-side copper surface and a large internal/bottom copper plane. Thermal resistance values are empirical measurements taken from evaluation boards.
2. The Si3218x linefeed is equipped with on-chip thermal limiting circuitry that shuts down the circuit when the junction temperature exceeds the thermal shutdown threshold. The thermal shutdown threshold is normally set to 145 °C; when in the ringing state the thermal shutdown is set to 200 °C.
3. Operation of the Si3218x above 125 °C junction temperature may degrade device reliability.

Table 5. Power Supply Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply currents: reset	I_{DD}[2]	V_T and V_R = Hi-Z, RSTB = 0	–	6.14	–	mA
	I_{VBAT}		–	0	–	mA
Supply currents: high impedance, open	I_{DD}	V_T and V_R = Hi-Z	–	20.2	–	mA
	I_{VBAT}		–	0.19	–	mA
Supply currents: forward/reverse, on-hook	I_{DD}	V_{TR} = –48 V, Automatic power save mode enabled	–	11.06	–	mA
	I_{VBAT}		–	0.25	–	mA
Supply currents: forward/reverse, on-hook	I_{DD}	V_{TR} = –48 V, Automatic power save mode disabled	–	30.33	–	mA
	I_{VBAT}		–	1.51	–	mA
Supply currents: tip/ring open, on-hook	I_{DD}	V_T or V_R = –48 V V_R or V_T = Hi-Z, Automatic power save mode enabled	–	11.02	–	mA
	I_{VBAT}		–	0.25	–	mA
Supply currents: tip/ring open, on-hook	I_{DD} I_{VBAT}	V_T or V_R = –48 V V_R or V_T = Hi-Z, Automatic power save mode disabled	–	29.59	–	mA
			–	0.86	–	mA
Supply currents: forward/reverse OHT, on-hook	I_{DD}	V_{TR} = 48 V	–	43.79	–	mA
	I_{VBAT}		–	2.28	–	mA
Supply currents: forward/reverse active, off-hook	I_{DD}	I_{LOOP} = 20 mA, R_{LOAD} = 200 Ω	–	44.56	–	mA
	I_{VBAT}		–	21.53	–	mA
Supply currents: ringing	I_{DD}	V_{TR} = 55 V_{RMS} + 0 V_{DC}, low power ringing, sinusoidal, f = 20 Hz R_{LOAD} = 5 REN = 1400 Ω	–	33.75	–	mA
	I_{VBAT}		–	33.21	–	mA

1. All specifications are for tracking a low-cost capacitive boost dc-to-dc converter at 25 °C. V_{DDD} = 3.3 V; V_{DC} = 12 V.
2. I_{DD} throughout includes I_{DDIO}.

Table 6. AC Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
TX/RX Performance					
Overload compression	Two-wire to PCM	See Figure 7 on page 13	–	–	
Single frequency distortion	Two-wire to PCM or PCM to two-wire: 200 Hz to 3.4 kHz	–	–	–40	dB
	PCM to two-wire to PCM: 200 Hz to 3.4 kHz, 16-bit linear mode	–	–	–63	dB
Signal-to- (noise + distortion) ratio[1]	200 Hz to 3.4 kHz TX or RX path. Active off-hook, and OHT, any Z_T	See Figure 6 on page 13	–	–	
Audio tone generator signal-to-distortion ratio[1]	0 dBm 0, active off-hook, and OHT, any Z_T	46	–	–	dB
Intermodulation distortion		–	–	–41	dB
Gain accuracy[1]	Two-wire to PCM or PCM to two-wire				dB
	1014 Hz, any gain setting	–0.2	–	0.2	dB
Attenuation distortion versus frequency	0 dBm 0[2]	See Figure 8 on page 14 and Figure 9 on page 15			
Group delay versus frequency		See Figure 10 on page 16 and Figure 11 on page 16			
Gain tracking[3]	1014 Hz sine wave, reference level –10 dBm signal level	–	–	–	–
	3 dB to –37 dB	–	–	0.25	dB
	–37 dB to –50 dB	–	–	0.5	dB
	–50 dB to –60 dB	–	–	1.0	dB
Round-trip group delay	1014 Hz, within same timeslot	–	450	500	µs
Two-wire return loss[4]	200 Hz to 3.4 kHz	26	30	–	dB
Transhybrid balance[4]	300 Hz to 3.4 kHz	26	30	–	dB
Noise Performance					
Idle channel noise[5]	C-message weighted	–	8	12	
	Psophometric weighted	–	–82	–78	dBmP
PSRR from V_{DDD}, V_{DDIO} @ 3.3 V	RX and TX, 200 Hz to 3.4 kHz	–	55	–	dB
Longitudinal Performance					
Longitudinal to metallic/PCM balance (forward or reverse)	200 Hz to 1 kHz	58	60	–	dB
	1 kHz to 3.4 kHz	53	58	–	dB
Metallic/PCM to longitudinal balance	200 Hz to 3.4 kHz	40	–	–	dB
Longitudinal impedance	200 Hz to 3.4 kHz at tip or ring	–	50	–	W
Longitudinal current capability	Active off-hook 60 Hz, Register 73 = 0x0B	–	25	–	mA

1. Analog signal measured as V_{TIP} to V_{RING}. Assumes ideal line impedance matching.
2. 0 dBm 0 is equal to 0 dBm into 600 Ω.
3. The quantization errors inherent in the µ/A-law companding process can generate slightly worse gain tracking performance in the signal range of 3 to –37 dB for signal frequencies that are integer divisors of the 8 kHz PCM sampling rate.
4. V_{DD} = 3.3 V, V_{BAT} = –52 V, no fuse resistors; RL = 600 Ω, ZS = 600 Ω synthesized using RS register coefficients.
5. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed –55 dBm.

Table 7. Linefeed Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC feed current		Differential	–	–	45	mA
		Common mode	–	–	30	mA
		Differential and common mode	–	–	45	mA
DC loop current accuracy		I_{LIM} = 18 mA	–	–	10	%
DC open circuit voltage accuracy		Active mode; V_{OC} = 48 V, V_{TIP} to V_{RING}	–	–	4	V
DC differential output resistance	R_{DO}	$I_{LOOP} < I_{LIM}$	160	–	640	Ω
DC on-hook voltage accuracy: ground start (tip open)	V_{OHTO}	$I_{RING} < I_{LIM}$; V_{RING} compared to ground, V_{RING} = –51 V	–	–	4	V
DC output resistance: ground start (tip open)	R_{ROTO}	$I_{RING} < I_{LIM}$; ring to ground	160	–	640	Ω
DC output resistance: ground start (tip open)	R_{TOTO}	Tip to ground	400	–	–	kΩ
Loop closure detect threshold accuracy		I_{THR} = 13 mA	–	–	10	%
Ground key detect threshold accuracy		I_{THR} = 13 mA	–	–	10	%
Ring trip threshold accuracy		AC detection, V_{RING} = 70 Vpk, no offset, I_{TH} = 80 mA	–	–	4	mA
		DC detection, 20 V dc offset, I_{TH} = 13 mA	–	–	1	mA
		DC detection, 0 V dc offset, R_{loop} = 1500 Ω	–	–	3	mA
Ringing amplitude	$V_{RINGING}$	Open circuit, V_{BAT} = –106 V	–104	–	–	V_{PK}
Sinusoidal ringing total harmonic distortion	R_{THD}	50 V_{RMS}, 0 V_{OFFSET}, 0 to 5 REN	–	1	–	%
Ringing frequency accuracy		f = 16 Hz to 60 Hz	–	–	1	%
Ringing cadence accuracy		Accuracy of on/off times	–	–	50	ms
Loop voltage sense accuracy		V_{TIP} to V_{RING} = 48 V	–	2	4	%
Loop current sense accuracy		I_{LOOP} = 18 mA	–	7	10	%
Power alarm threshold accuracy		Power threshold = 1.0 W V_{BAT} = –56 V, Loop current = 40 mA, R_{LOAD} = 600 Ω	–	15	–	%

Table 8. Digital I/O Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	SCLK, CSB, SPI_MOSI, PCLK, FSYNC, PCM_MOSI, RSTB	0.7 x V_{DDIO}	–	V_{DDIO}	V
Low-level input voltage	V_{IL}	SCLK, CSB, SPI_MOSI, PCLK, FSYNC, PCM_MOSI, RSTB	–	–	0.3 x V_{DDIO}	V
High-level output voltage	V_{OH}	SPI_MISO, SPI_MOSI_THRU, PMC_MISO, INTB: I/O = –4 mA	V_{DDIO} – 0.6	–	–	V
Low-level output voltage	V_{OL}	SPI_MISO, SPI_MOSI_THRU, PMC_MISO, INTB: I/O = 4 mA	–	–	0.4	V
SPI_MOSI_THRU and RSTB internal pullup current			33	42	65	µA
Input leakage current	IL		–	–	10	µA

Table 9. Charge Pump Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output voltage (DCDRV, DCFF)	V_{CP}		2 x V_{DD} – 1	–	2 x V_{DD}	V
Output current	I_{CP}		–	–	3[1]	mA

1. Peak drive current capability is >60 mA.

Table 10. Switching Characteristics: General Inputs[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RSTB pulse width (PCM/SPI interface)	t_{RST}		200	–	–	µs
RSTB high to first SPI transfer start (PCM/SPI interface)	t_{RCS}		5	–	–	ms

1. All timing referenced to 50% level of waveform. Input test levels are V_{IH} = V_{DD} to 0.4 V, V_{IL} = 0.4 V. Rise and fall times are referenced to 20% and 80% levels of the waveform.

4. Timing

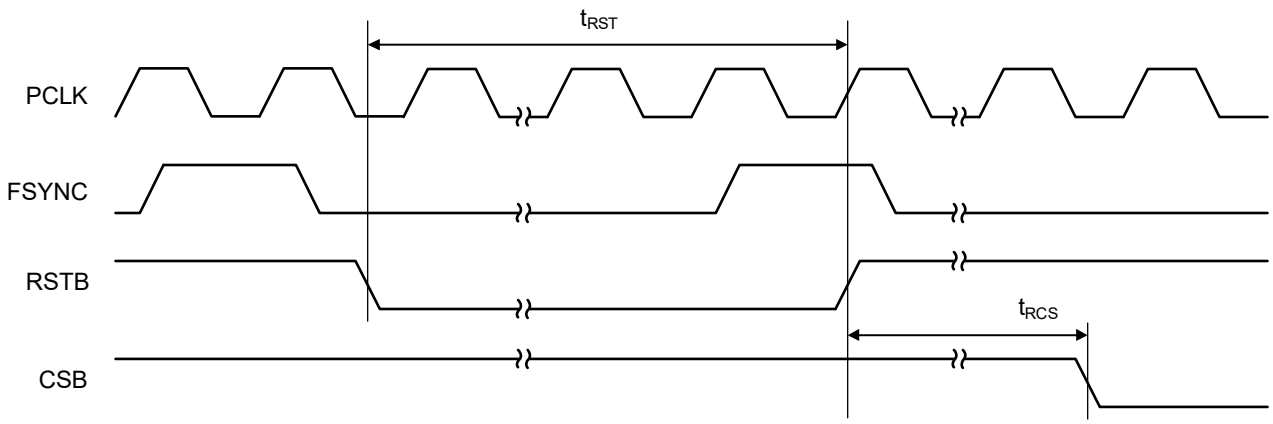

Figure 3. Reset Timing Diagram

Table 11. SPI Switching Characteristics[1, 2]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Cycle time, SCLK	t_c		83	–	–	ns
Rise time, SCLK	t_r		–	–	25	ns
Fall time, SCLK	t_f		–	–	25	ns
Delay time, SCLK fall to SPI_MISO active	t_{d1}		–	–	20	ns
Delay time, SCLK fall to SPI_MISO transition	t_{d2}		–	–	20	ns
Delay time, CSB rise to SPI_MISO tristate	t_{d3}		–	–	20	ns
Setup time, CSB to SCLK fall	t_{su1}		25	–	–	ns
Hold time, CSB to SCLK rise	t_{h1}		20	–	–	ns
Setup time, SPI_MOSI to SCLK rise	t_{su2}		25	–	–	ns
Hold time, SPI_MOSI to SCLK rise	t_{h2}		20	–	–	ns
Delay time between chip selects	t_{cs}		220	–	–	ns
SPI_MOSI to SPI_MOSI_THRU propagation delay	t_{d4}		–	4	10	ns

1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_{DDIO} – 0.4$ V, $V_{IL} = 0.4$ V.
2. Characteristics for outputs specified with CL = 20 pF.

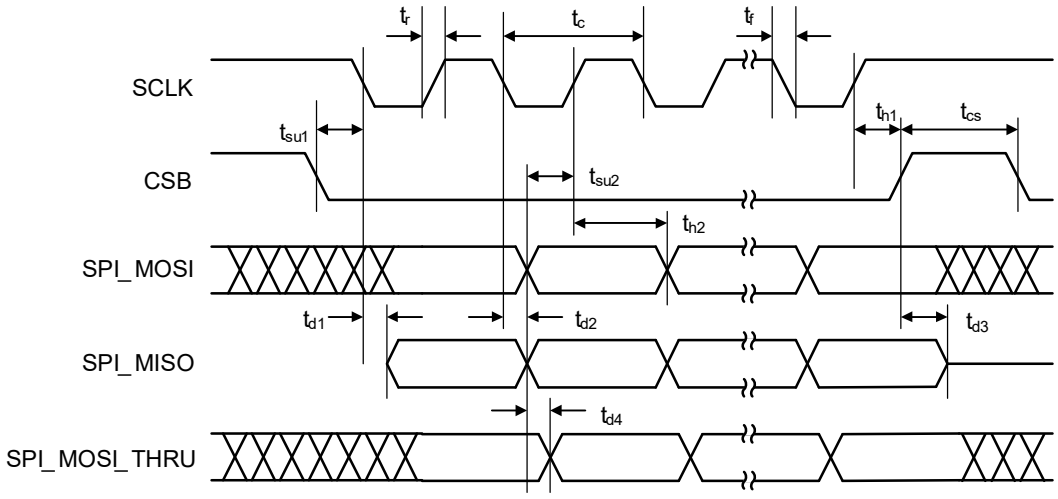

Figure 4. SPI Timing Diagram

Table 12. PCM Highway Interface: Switching Characteristics

Parameter	Symbol	Test Condition	Min[1]	Typ[1]	Max[1]	Unit
PCLK period	t_p		122	–	1953	ns
PCLK jitter tolerance	$t_{jitter\ (FXS)}$		–	–	8	ns_{RMS}
Valid PCLK inputs[2]			–	256		kHz
			–	512	–	kHz
			–	768	–	kHz
			–	1.024	–	MHz
			–	1.536	–	MHz
			–	1.544	–	MHz
			–	2.048	–	MHz
			–	4.096	–	MHz
			–	8.192	–	MHz
FSYNC period[3]	t_{fs}		–	125	–	µs
PCLK duty cycle tolerance	t_{dty}		40	50	60	%
FSYNC jitter tolerance[4]	t_{jitter}		–	–	±120	ns
Rise time, PCLK	t_r		–	–	25	ns
Fall time, PCLK	t_f		–	–	25	ns
Delay time, PCLK rise to PCM_MISO active	t_{d1}		–	–	20	ns
Delay time, PCLK rise to PCM_MISO transition	t_{d2}		–	–	20	ns
Delay time, PCLK rise to PCM_MISO tristate[5]	t_{d3}		–	–	20	ns

Table 12. PCM Highway Interface: Switching Characteristics (Continued)

Parameter	Symbol	Test Condition	Min[1]	Typ[1]	Max[1]	Unit
Setup time, FSYNC to PCLK fall	t_{su1}		25	–	–	ns
Hold time, FSYNC to PCLK fall	t_{h1}		20	–	–	ns
Setup time, PCM_MOSI to PCLK fall	t_{su2}		25	–	–	ns
Hold time, PCM_MOSI to PCLK fall	t_{h2}		20	–	–	ns
FSYNC pulse width	t_{wfs}		t_p	–	125	µs-t_p

1. All timing is referenced to the 50% level of the waveform. Input test levels are V_{IH} to $V_{I/O}$ –0.4 V, V_{IL} = 0.4 V.
2. A constant PCLK and FSYNC are required.
3. FSYNC source is assumed to be 8 kHz under all operating conditions.
4. FSYNC jitter tolerance relative to PCLK.
5. Specification applies to PCLK fall to PCM_MISO tristate when that mode is selected.

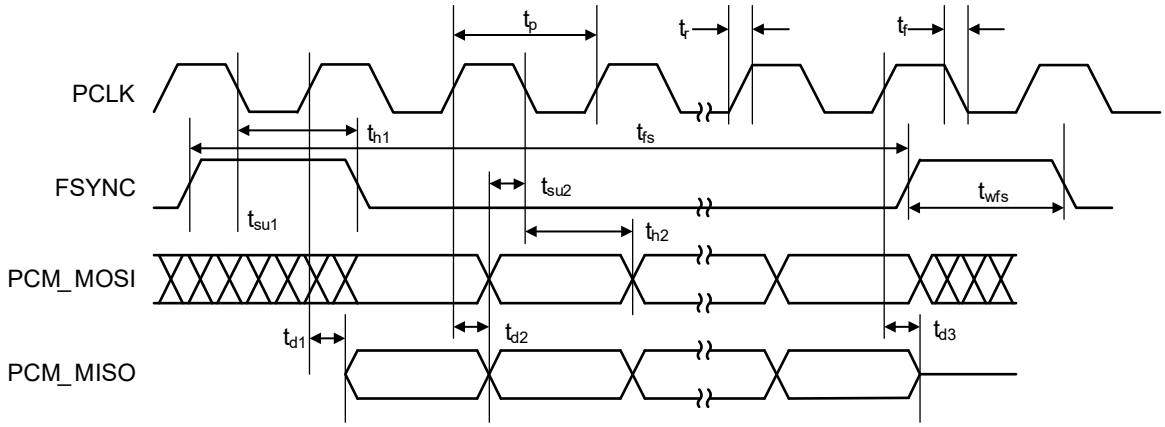

Figure 5. PCM Highway Interface Timing Diagram

5. Typical Performance Characteristics

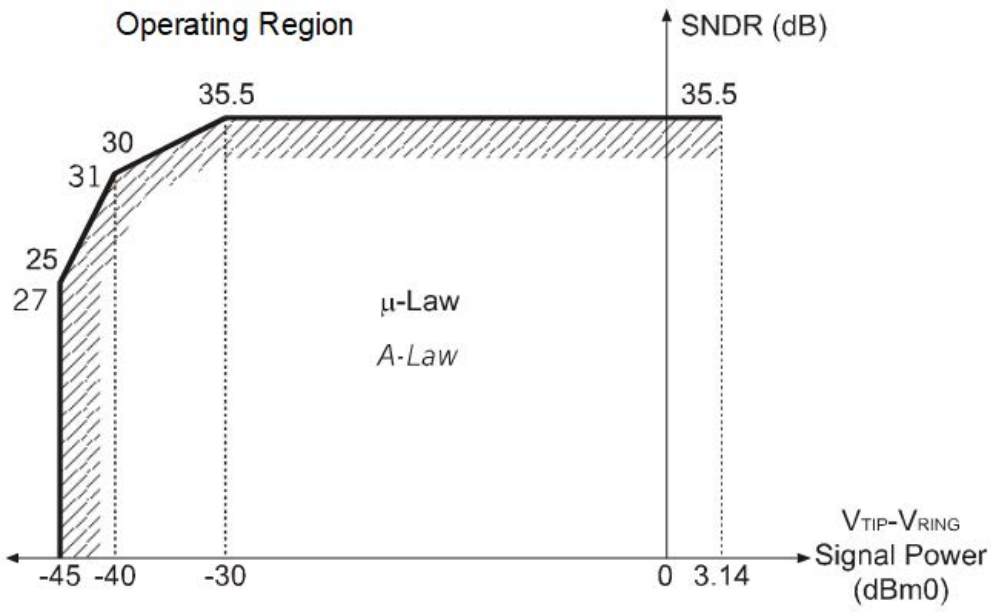

Figure 6. Transmit and Receive Path Signal-to-Noise-and-Distortion Ratio (SNDR)

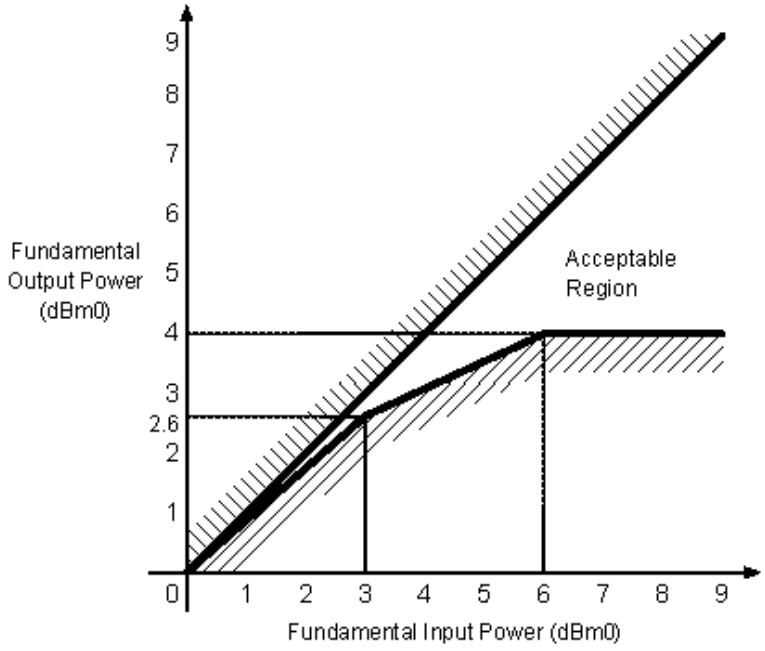

Figure 7. Overload Compression Performance

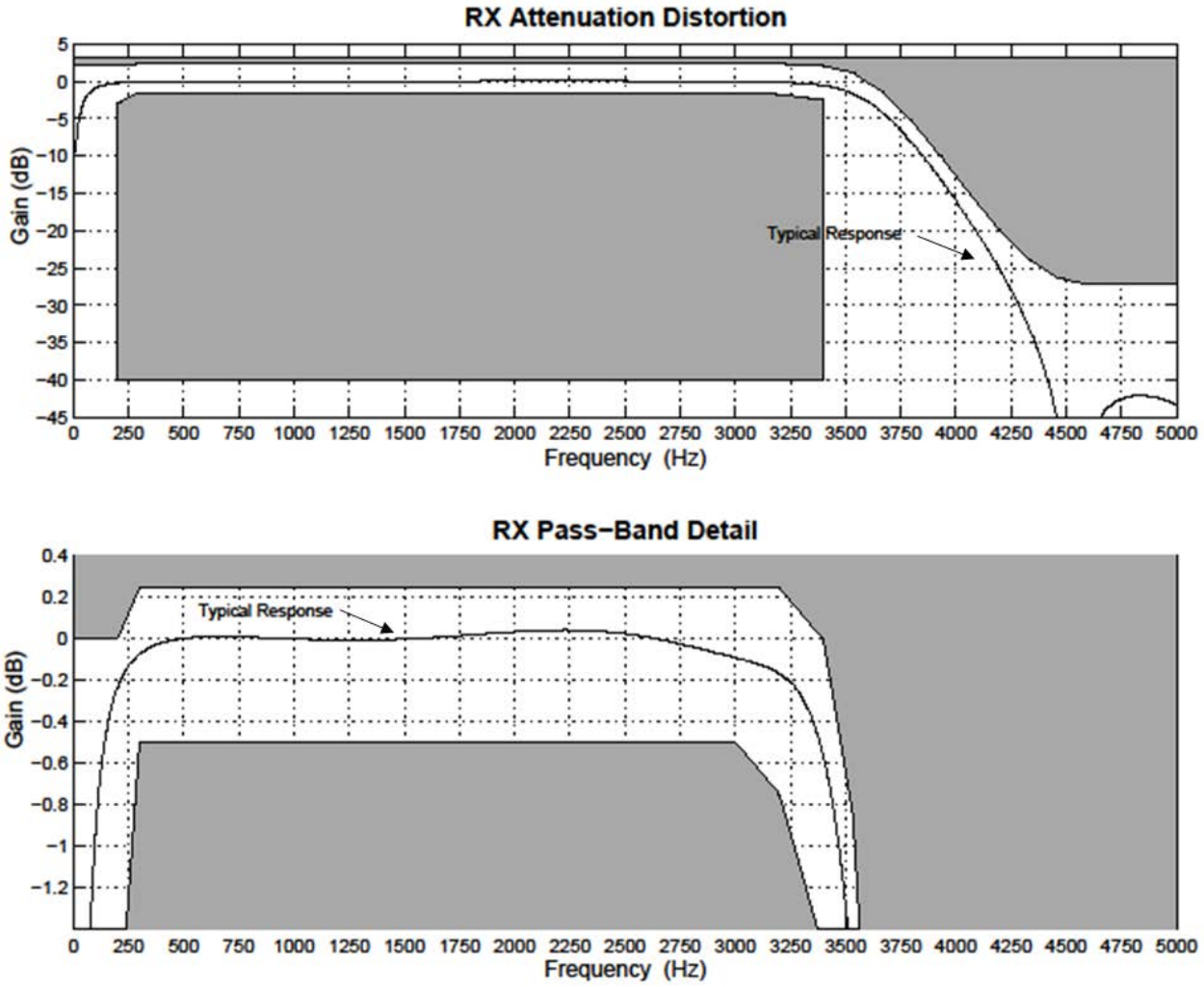

Figure 8. Receive Path Frequency Response

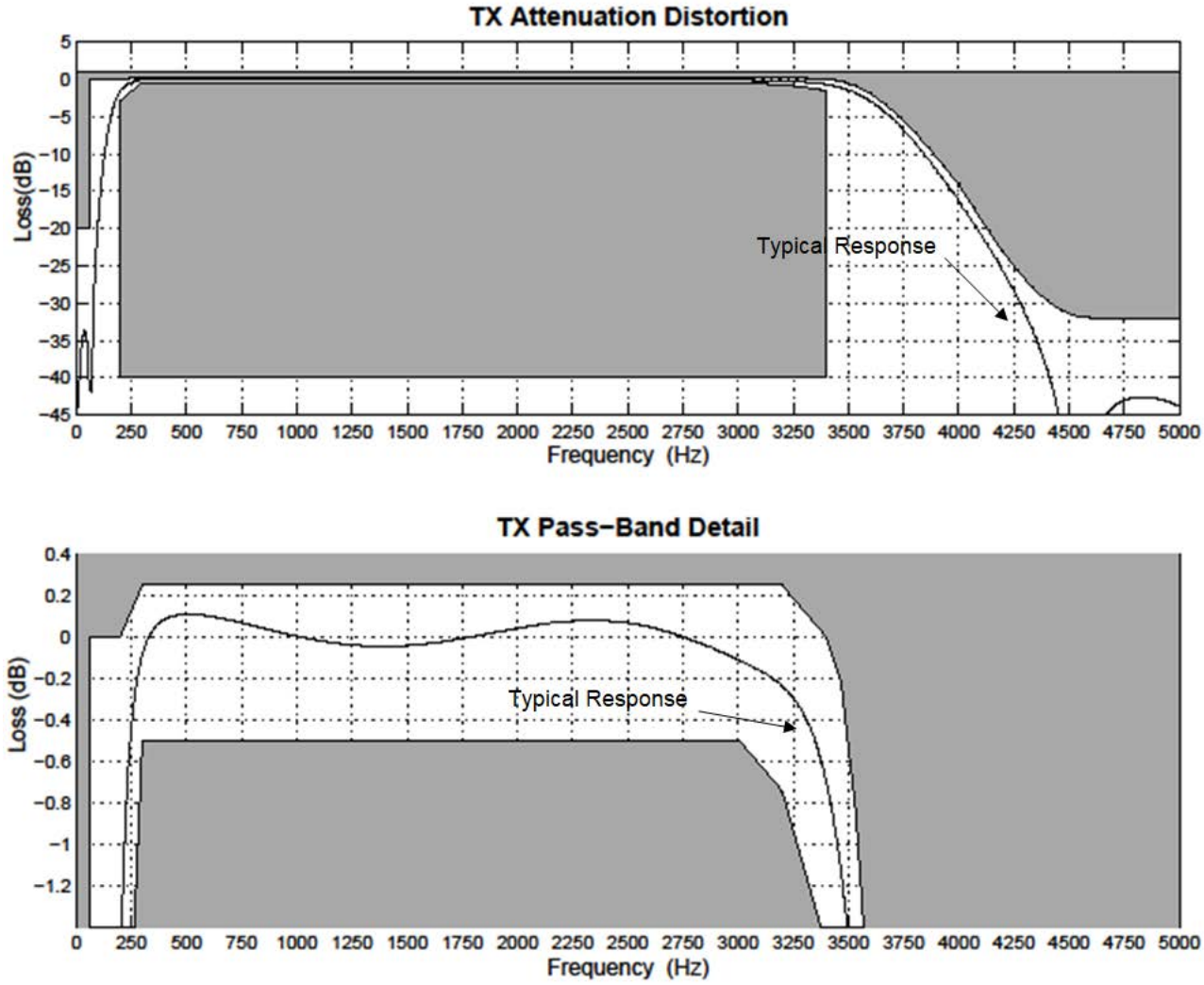

Figure 9. Transmit Path Frequency Response

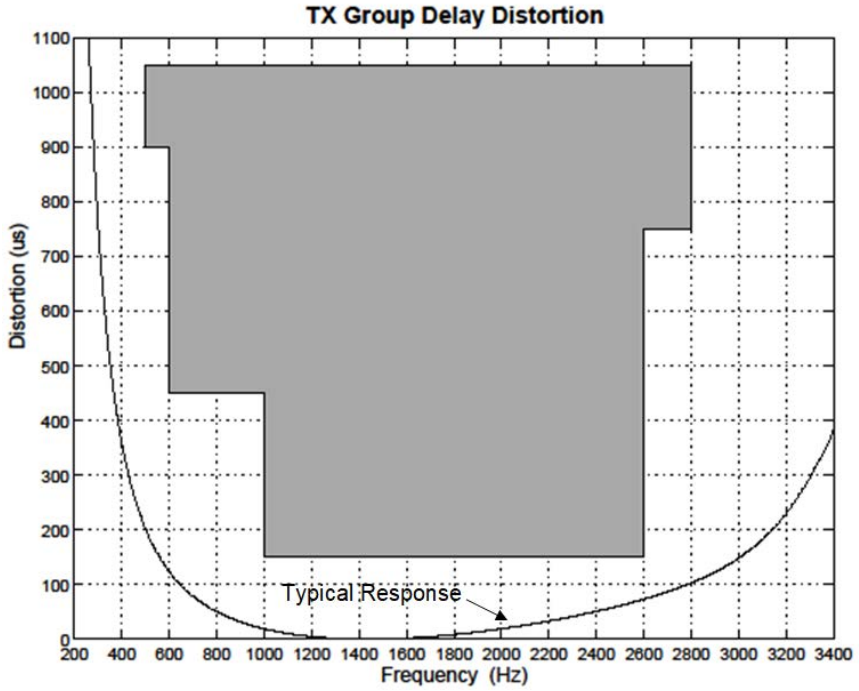

Figure 10. Transmit Group Delay Distortion

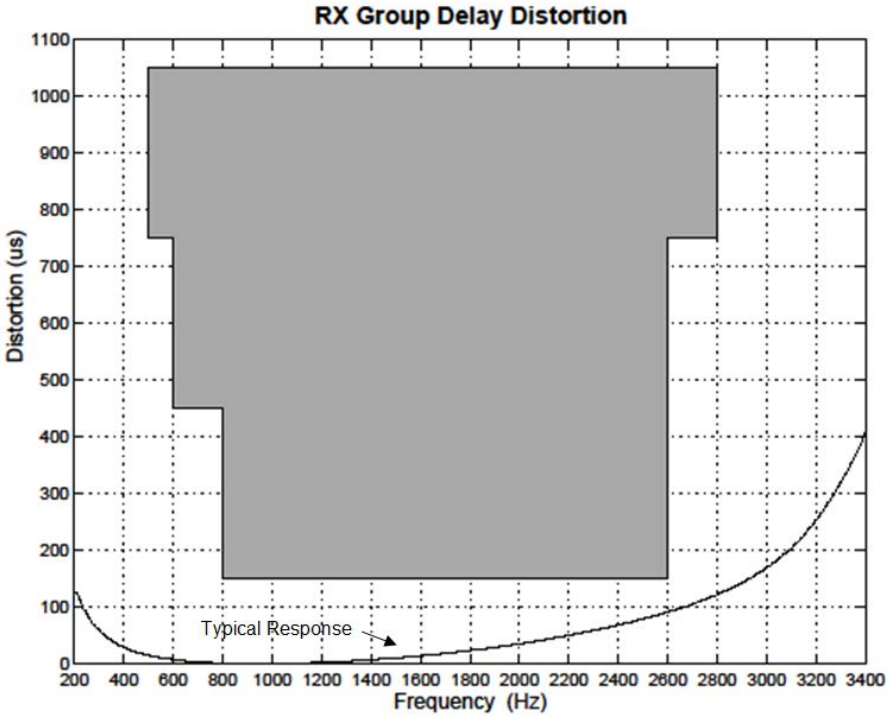

Figure 11. Receive Group Delay Distortion

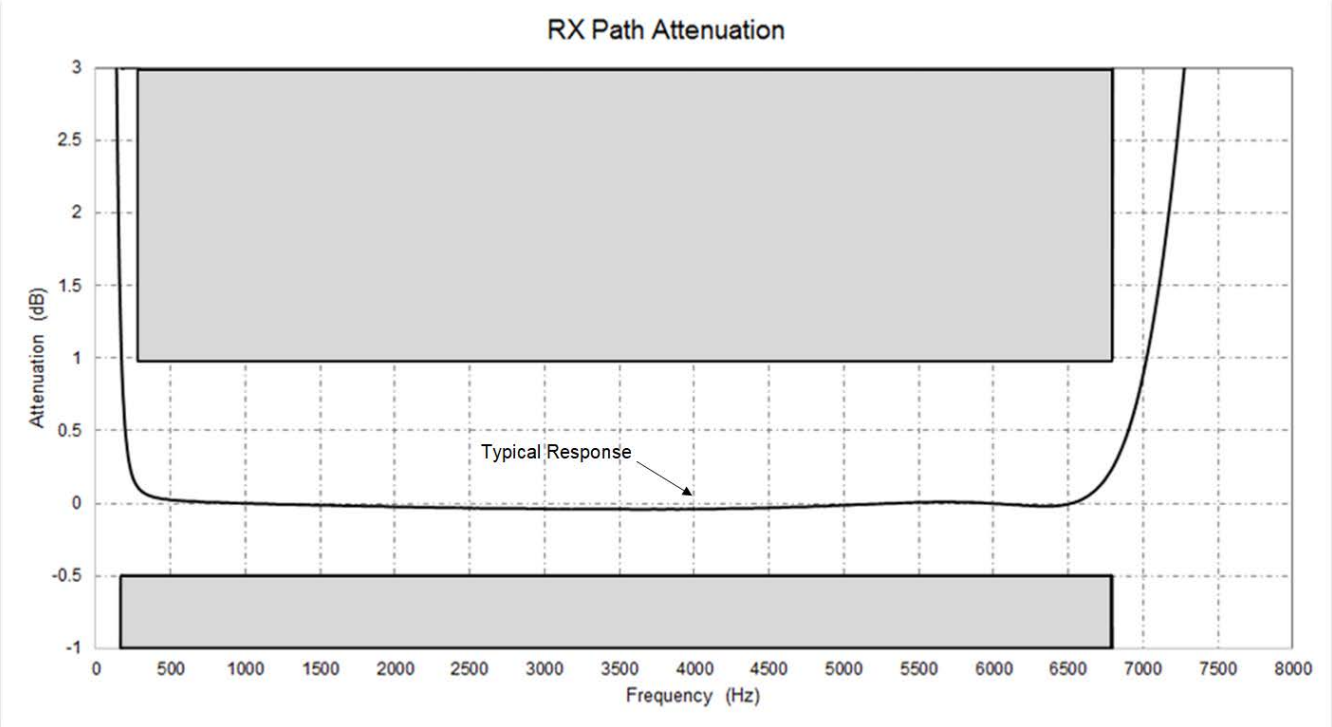

Figure 12. Receive Wideband Frequency Response

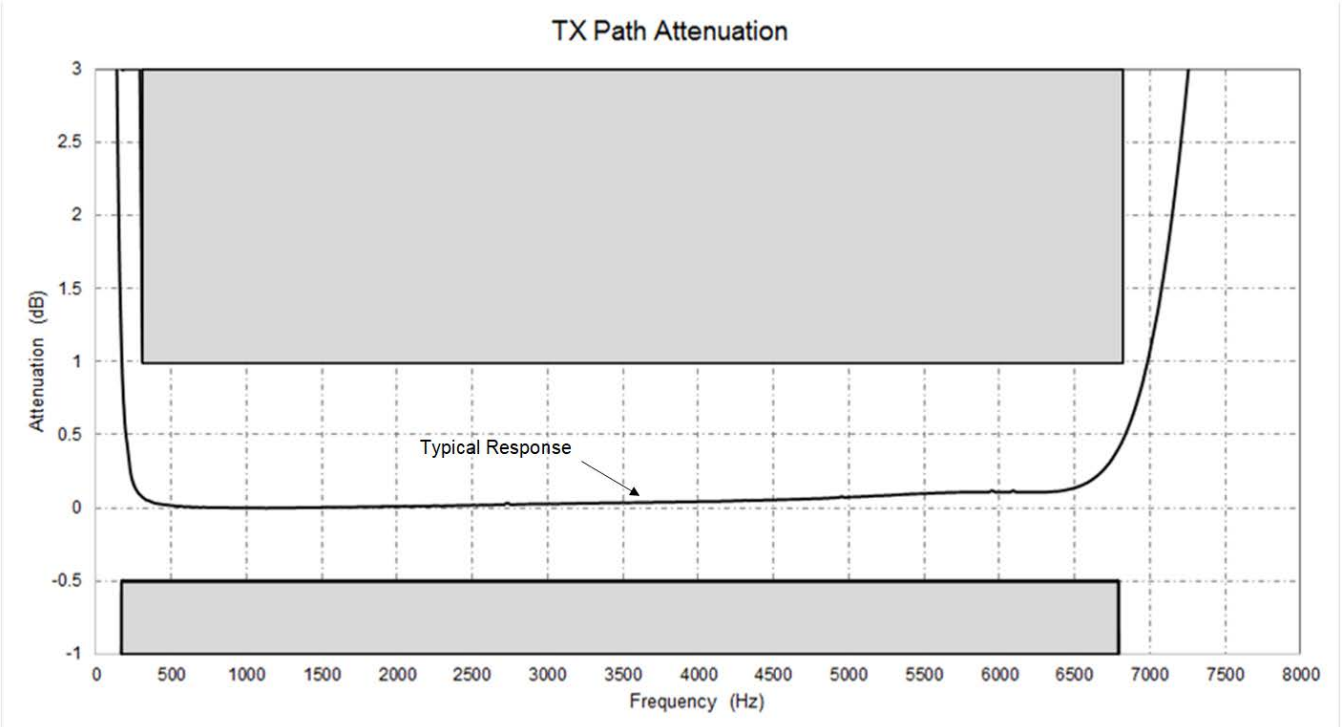

Figure 13. Transmit Wideband Frequency Response

6. Foreign Exchange Subscriber Features

6.1. DC Feed Characteristics

ProSLIC internal linefeed circuitry provides completely programmable dc feed characteristics.

When in the active state, the ProSLIC operates in one of three dc linefeed operating regions: a constant-voltage region, a constant-current region, or a resistive region, as shown in the figure below. The constant-voltage region has a low resistance, typically 160 Ω. The constant-current region approximates infinite resistance.

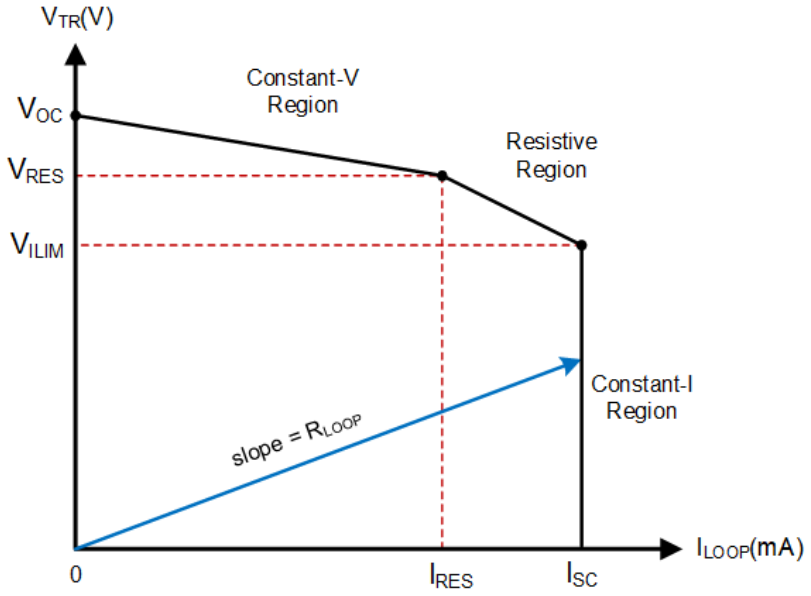

Figure 14. Dual ProSLIC DC Feed Characteristics

6.2. Linefeed Operation States

The linefeed interface includes eight different register-programmable operating states as listed in Table 13, “Linefeed Operating States,” on page 19. The *open* state is the default condition in the absence of any preloaded register settings. The device may also automatically enter the open state in the event of a linefeed fault condition.

6.3. Line Voltage and Current Monitoring

The ProSLIC continuously monitors the tip, ring, and battery voltages and currents via an on-chip monitor ADC and stores the resulting values in individual RAM locations. Additionally, the loop voltage (V_{TIP} to V_{RING}), loop current, and longitudinal current values are calculated based on the tip and ring measurements and are stored in unique register locations for further processing. The ADC updates all registers at a rate of 2 kHz or greater.

6.4. Power Monitoring and Power Fault Detection

The Si3218x line monitoring functions are used to continuously protect against excessive power conditions. The Si3218x contains an on-chip, analog sensing diode that provides real-time temperature data and turns off the device when a preset threshold is exceeded.

If the Si3218x detects a fault condition or overpower condition, it automatically sets that device to the open state and generates a *power alarm* interrupt.

The interrupt can be masked, but masking the automatic transition to open is not recommended since it is used to protect the Si3218x HVIC under excessive power conditions. The various power alarms and linefeed faults supporting automatic intervention are described below:

1. Total power exceeded
2. Excessive foreign current or voltage on tip and/or ring
3. Thermal shutdown event

6.5. Thermal Overload Shutdown

If the die temperature exceeds the maximum junction temperature threshold, TJ_{MAX}, of 145 °C or 200 °C, the device has the ability to shut itself down to a low-power state without user intervention.

Table 13. Linefeed Operating States

Linefeed State	Description
Open	Output is high-impedance, and all line supervision functions are powered down. Audio is also powered down. This is the default state after powerup, or following a hardware reset. This state can also be used in the presence of line fault conditions and to generate open switch intervals (OSIs). This state is used in the line diagnostics mode as a high impedance state during linefeed testing. A power fault condition may also force the device into the open state.
Forward active Reverse active	Linefeed circuitry and audio are active. In forward active state, the tip lead is more positive than the ring lead. In reverse active state, the ring lead is more positive than the tip lead.
Forward OHT Reverse OHT	Provides data transmission during an on-hook loop condition (such as when transmitting caller ID data between ringing bursts). Linefeed circuitry and audio are active. In Forward OHT state, the tip lead is more positive than the ring lead. In reverse OHT state, the ring lead is more positive than the tip lead.
Tip open	Provides an active linefeed on the ring lead and sets the tip lead to high impedance (≥400 kΩ) for ground start operation in forward polarity. Loop closure and ground key detect circuitry are active.
Ring open	Provides an active linefeed on the tip lead and sets the ring lead to high impedance (≥400 kΩ) for ground start operation in reverse polarity. Loop closure and ground key detect circuitry are active.
Ringing	Drives programmable ringing signal onto tip and ring leads with or without dc offset.
Line diagnostics	The channel is put into diagnostic mode. In this mode, the channel has special diagnostic resources available.

6.6. Loop Closure Detection

The Si3218x provides a completely programmable loop closure detection mechanism. The loop closure detection scheme provides two unique thresholds to allow hysteresis, and also includes a programmable debounce filter to eliminate false detection. A loop closure detect status bit provides continuous status. A maskable interrupt bit is also provided.

6.7. Ground Key Detection

The Si3218x provides a ground key detect mechanism using a programmable architecture similar to the loop closure scheme. The ground key detect scheme provides two unique thresholds to allow hysteresis and also includes a programmable debounce filter to eliminate false detection. A ground key detect status bit provides continuous status. A maskable interrupt bit is also provided.

6.8. Ringing Generation

The Si3218x supports the patented low-power ringing (LPR) method exclusively, which when used with a tracking battery scheme, maximizes the ringing power transfered to the load and reduces overall power consumption. Ringing is fully programmable, including frequency, amplitude, dc offset, wave shape and crest factor. The Si3218x also supports automatic ring cadencing and ringtrip detection (ac and dc).

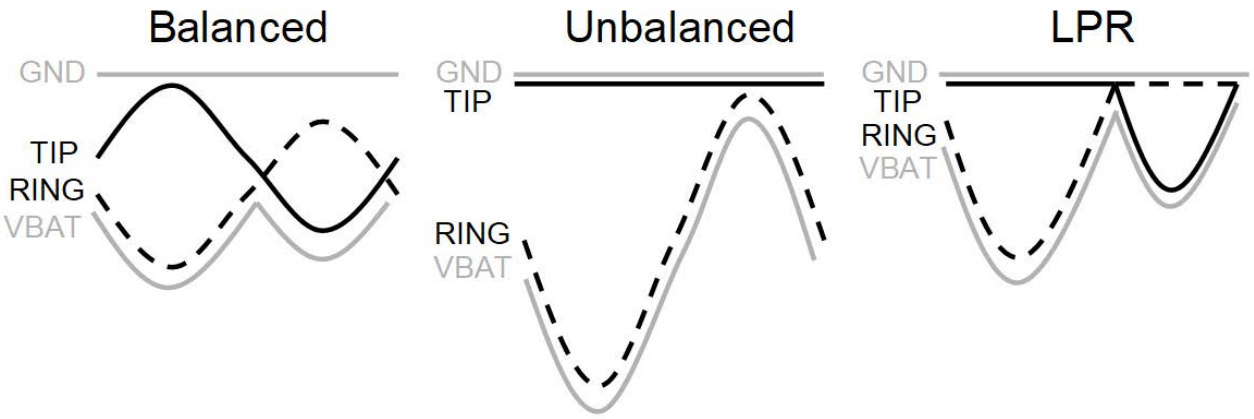

Figure 15. Ringing Mode

6.9. Polarity Reversal

The Si3218x supports polarity reversal for message waiting and various other signaling modes. The ramp rate can be programmed for a smooth or abrupt transition to accommodate different application requirements.

6.10. Two-Wire Impedance Synthesis

The ac two-wire impedance synthesis is generated on-chip using a DSP-based scheme to optimally match the output impedance of the Si3218x to the reference impedance. Most real or complex two-wire impedances can be generated with appropriate register coefficients.

6.11. Transhybrid Balance Figure

The transhybrid balance function is implemented on-chip using a DSP-based scheme to effectively cancel the reflected receive path signal from the transmit path.

6.12. Tone Generators

The Si3218x includes two digital tone generators that enable a wide variety of single- or dual-tone frequencies and amplitude combinations. Each tone generator has its own set of registers that hold the desired frequency, amplitude, and cadence to allow generation of DTMF and call progress tones for different requirements. The tones can be directed to either receive or transmit paths.

6.13. DTMF Detection (Si32185)

In DTMF, two tones generate a DTMF digit. One tone is chosen from four possible row tones, and one tone is chosen from four possible column tones. The sum of these tones constitutes one of 16 possible DTMF digits.

6.14. Pulse Metering

The pulse metering system for the Si3218x is designed to inject a 12 or 16 kHz billing tone into the audio path with maximum amplitude of 0.5 V_{RMS} at tip and ring into a 200 Ω ac load impedance. The tone is generated in the DSP via a table lookup that guarantees spectral purity by not allowing drift. The tone will ramp up until it reaches a host-programmed threshold, at which point it will maintain that level until instructed to ramp down, thus creating a trapezoidal envelope.

The amplitude is controlled by an automatic gain control circuit (AGC). While the tone is ramping up, the AGC circuit takes the feedback audio and applies it to a band pass filter, which is programmed for the 12 or 16 kHz frequency of interest. When the peak is detected, the ramp is stopped.

6.15. DC-to-DC Controller

The Si3218x integrates a dc-to-dc controller to control an external tracking dc-to-dc converter which generates the high voltage supply (V_{BAT}) to the SLIC. The tracking V_{BAT} voltage generated from a single positive dc input is optimized to minimize power consumption by closely tracking the SLIC state, and also tracking ringing waveforms.

The dc-to-dc controller output DCDRV is driven by an internal charge pump which allows it to connect directly to the gate of the MOSFET switch of the dc-to-dc converter. This eliminates the need for the MOSFET predrive circuit that is typically required when other SLICs are used with a MOSFET with VTH greater than VDD. See Table 10, “Switching Characteristics: General Inputs,” on page 9.

6.16. Wideband Audio

The Si3218x supports wideband audio (150 Hz to 6.8 kHz) compliant with PKT-SP-HDV-104-120823, and is configurable to support the full ITU-T-G.722-201209 bandwidth (50 Hz to 7 kHz). The wideband provides an expanded audio band at a 16-bit, 16 kHz sample rate for enhanced audio quality while maintaining standard telephony audio compatibility. Wideband audio samples are transmitted and received at an effective 16 kHz rate by using multiple timeslots in a single 8 kHz frame.

6.17. Test Functions

The Si3218x supports a rich set of metallic loop tests to diagnose external faults, as well as a set of inward self-tests to support diagnostics of the Si3218x-based voice port. Implementation of metallic loop tests require the ProSLIC MLT API, while the inward self-tests are included in the standard ProSLIC API.

Supported metallic loop tests include:

Voltages	Measures ac and dc voltages from T-R, T-G and R-G.
Receiver off-hook	Discriminates between a resistive fault and an off-hook terminating device.
REN	Measures ringer equivalence number.
REN capacitance	Measures T-R capacitance of on-hook load.
Capacitance	Measures three-terminal capacitance.
Resistance	Measures resistance from T-R, T-G or R-G.

Supported inward self-tests include:

PCM loopback	Configures Si3218x for 8 or 16-bit PCM loopback.
DC feed	Verifies dc feed I/V and loop closure using integrated test load.
Ringing and ringtrip	Verifies ringing voltage (ac and dc). Provides optional ringtrip check to support system level signaling verification.
Battery	Verifies V_{BAT}.
Audio gain	Measures gain of RX (host-to-line) and TX (line-to-host) paths without using an external load, test equipment, or requiring the host to provide audio samples.

In addition to these specific test suites, a variety of general test functions are available, including:

Monitor ADC	Provides tip/ring voltages (inside and outside overcurrent protection), tip/ring currents and V_{BAT} voltage.
Audio diagnostic filters	Three cascaded second order biquad filters with peak hold and averaging capabilities.
Loopback modes	Digital and analog loopback modes to isolate portions of the audio path.
Tone generators	Dual tone generators may be used as general purpose signal generators for test purposes.

7. System Interfaces

7.1. SPI Control Interface

The Si3218x SPI controller interface is a four-wire interface modeled after microcontroller and serial peripheral devices. The interface consists of a clock (SCLK), chip select (CSB), serial data input (SPI_MOSI), and serial data output (SPI_MISO). In addition, the ProSLIC devices feature a serial data through output (SPI_MOSI_THRU) to support operation of up to 32 channels using a single chip select line. The FXS port occupies one SPI channel. The device operates with both 8-bit and 16-bit SPI controllers.

7.2. PCM Interface and Companding

The Si3218x PCM interface is a flexible, programmable interface for the transmission and reception of digital PCM samples. PCM data transfer is controlled by the PCM clock (PCLK) and frame sync (FSYNC) inputs as well as the PCM mode select, PCM transmit start, and PCM receive start settings.

The interface can be configured to support from four to 128 8-bit time slots in each 125 µs frame, corresponding to a PCLK frequency range of 256 kHz to 8.192 MHz. 1.544 MHz is also supported.

The Si3218x supports both µ-255 Law (µ-Law) and A-law companding formats in addition to 16-bit linear data mode with no companding.

7.3. Input/Output Voltage Selection

The Si3218x digital host interface I/O (PCM/SPI) may directly interface to 1.8 V to 3.3 V devices. The I/O voltage selection is made by supplying the V_{DDIO} pin with the appropriate I/O supply voltage.

To avoid power supply sequencing issues, V_{DDIO} should be connected to the same supply as V_{DD} in 3.3 V interface designs. Other voltages between 1.8 V and 3.3 V can also be used for V_{DDIO} (for example 2.5 V), but steps must be taken to ensure that the V_{DDIO} supply comes up after the V_{DD} supply if V_{DDIO} is not connected to V_{DD} or V_{DDREG}.

8. Package Top Mark and Handling Information

Package marking for the Si3218x is shown below, followed by dimensions, and PCB land pattern.

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The Si3218x is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, PCB Design & SMT Assembly/Rework Guidelines for RFLGA Packages, document number 103147.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format or in trays.

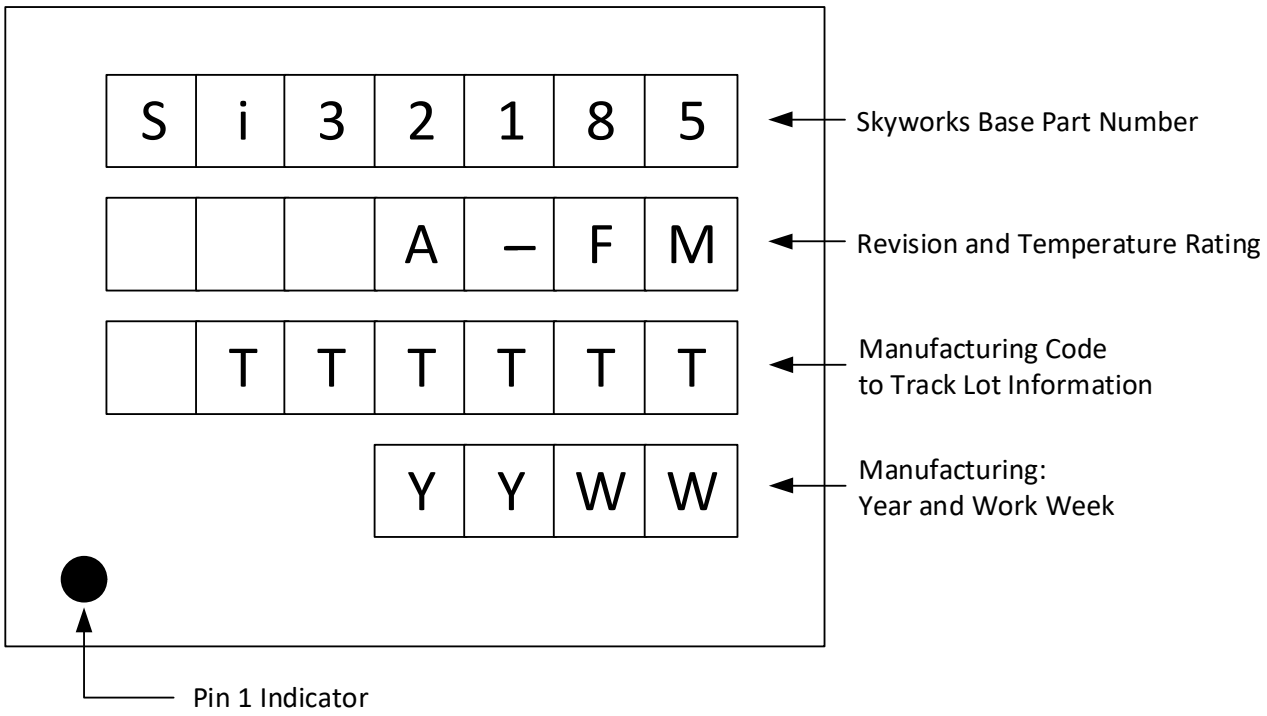

Figure 16. Typical Part Marking

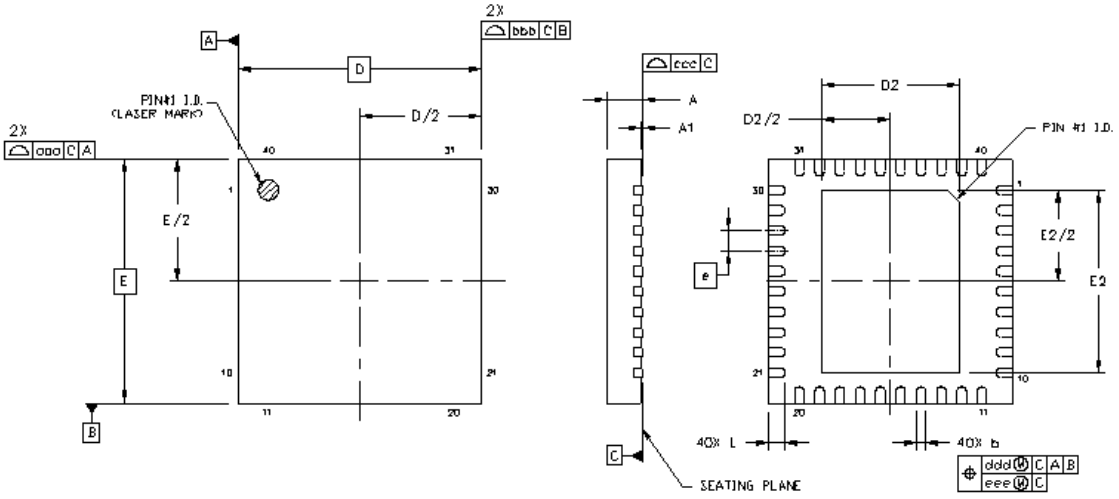

Figure 17. Package Dimensions

Table 14. Package Dimension Information[1, 2, 3, 4]

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		6.00 BSC	
D2	3.30	3.40	3.50
e		0.50 BSC	
E		6.00 BSC	
E2	4.40	4.50	4.60
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

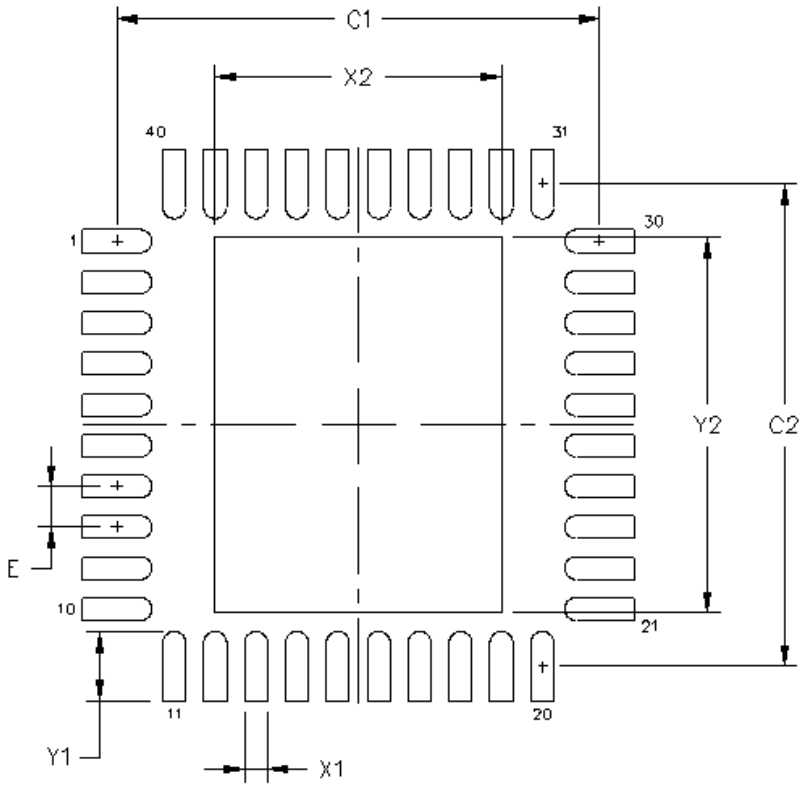

Figure 18. Land Pattern

Table 15. Land Pattern Dimensions

Dimension	mm	Notes
C1	5.90	**General** 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. This land pattern design is based on the IPC-7351 guidelines. 3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a fabrication allowance of 0.05 mm. **Solder Mask Design** 1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. **Stencil Design** 1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 2. The stencil thickness should be 0.125 mm (5 mils). 3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. 4. A 2×2 array of 1.10 x 1.10 mm openings on 1.30 mm pitch should be used for the center ground pad. **Card Assembly** 1. A No-Clean, Type-3 solder paste is recommended. 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components. **PCB Design** 1. High-Tg (glass transition temperature) PCB materials (Tg 170 °C is standard industry practice). 2. A minimum of eight thermal vias are required in each center pad. 3. The recommended via diameter is 0.20 to 0.30 mm (8 to 12 mils). 4. Thermal vias placed in the center pads must have a minimum spacing of 1.0 mm from the edge of the via to the closest pin pad metal (d 1.0mm). 5. Vias placed within the center pad areas must be either filled, or tented on the top side of the board, to prevent solder thieving from under the device.
C2	5.90	
E	0.50	
X1	0.30	
Y1	0.85	
X2	3.50	
Y2	4.60	

9. Ordering Information

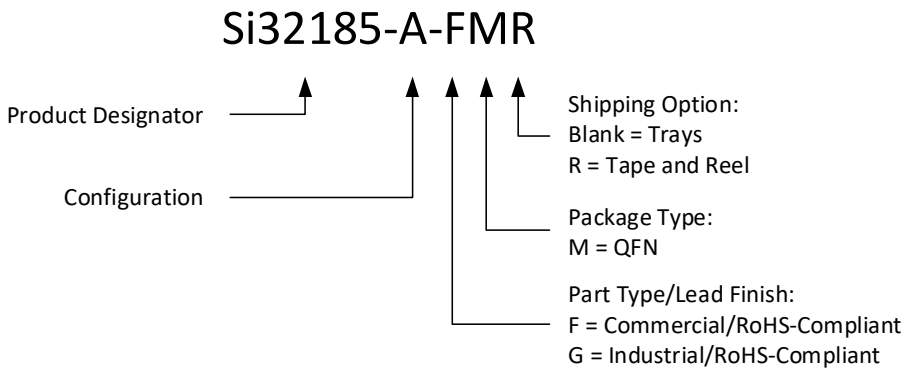

Figure 19. Ordering Information

Table 16. Ordering Guide[1]

Part Number	Description	Package Type	Max VBAT	Temperature
Si32184-A-FM	Wideband FXS, PCM interface, parametric MLT	QFN40[2]	–106 V	0 to 70 °C
Si32184-A-GM	Wideband FXS, PCM interface, parametric MLT	QFN40	–106 V	–40 to 85 °C
Si32185-A-FM	Wideband FXS, PCM interface, parametric MLT, DTMF detection	QFN40	–106 V	0 to 70 °C
Si32185-A-GM	Wideband FXS, PCM interface, parametric MLT, DTMF detection	QFN40	–106 V	–40 to 85 °C
Evaluation Kit				
Si32185ACB10SL0KIT	PCM interface, wideband FXS with DTMF detection low-cost capacitive boost dc-to-dc converter EVB.	QFN40	–100 V	NA
Si32185ACB10SL1KIT	PCM interface, wideband FXS with DTMF detection low-cost capacitive boost dc-to-dc converter EVB.	QFN40	–106 V	NA

1. Add an “R” at the end of the part number to denote tape and reel ordering option.
2. QFN: Quad Flat No-lead.

10. Revision History

Revision	Date	Description
A	September 2025	Initial internal release. Removed Si32182 and Si32183.