Mercury+ XU1 SoC Module

User Manual

Purpose

The purpose of this document is to present the characteristics of the Mercury+ XU1 SoC module to the user, and to provide the user with a comprehensive guide to understanding and using the Mercury+ XU1 SoC module.

Summary

This document first gives an overview of the Mercury+ XU1 SoC module followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Product Information	Code	Name
Product	ME-XU1	Mercury+ XU1 SoC Module

Document Information	Reference	Version	Date
Reference / Version / Date	D-0000-428-001	20	04-Jun-2026

Approval Information	Name	Position	Date
Written by	DIUN	Design Engineer	04-May-2016
Verified by	GLAC	Design Expert	12-May-2016
Approved by	IJOS	Manager, BU-SP	04-Jun-2026

Document History

Version	Date	Author	Comment
20	04-Jun-2026	MGOS	Fixed value of power consumption in Operating Conditions section.
19	26-Mar-2026	MGOS	Added EN-Number for additional product.
18	26-Nov-2025	MGOS	Added description of Enclustra Yocto BSP layer. Added section “Getting Started”. Re-structured section “Device Configuration”.
17	06-Dec-2024	MGOS	Updated for revision 5.1 modules. Specified LDO voltage change at revision 5.0.
16	04-Oct-2023	MGOS	Updated for revision 5.0 modules: added EN-numbers for all versions, corrected voltage supply input for VCC_BAT, improved terminology, content, and layout for better readability and consistency
15	29-Aug-2021	TKAU	Updated for revision 4.2 modules: added information on discontinuation of support for power converter switching frequency synchronization, changes on base board descriptions
14	16-Feb-2021	DIUN	Added information on Mercury heat sinks, added Mercury+ ST1 to accesories section, added information on FPGA fuses and warranty, on differential I/Os, on voltage monitoring outputs, removed 15 Gbps limitation on MGTs due to Hirose connector, other style updates
13	15-Aug-2019	DIUN	Added new product variant
12	25-Jul-2019	DIUN	Added information on new variants, on power supplies, corrected supported voltage range for VCC_BAT, corrected minimum MDIO clock frequency, other style updates
11	08-May-2019	DIUN	Corrected power synchronization frequency domain and duty cycle, added information on Linux how-to guide

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Version	Date	Author	Comment
10	05-Apr-2019	DIUN	Updated for revision 4 modules, added information on new product variants, other style updates
09	03-Jan-2019	DIUN	Added information on voltage monitoring, heat sink, and corrected power synchronization frequency domain
08	12-Sep-2018	DIUN	Updated assembly drawings for revision 3, other minor corrections
07	27-Aug-2018	DIUN	Updated for revision 3 modules, other style updates
06	20-Apr-2018	DIUN	Minor updates and corrections
05	13-Apr-2018	DIUN	Updated for revision 2 modules, updated DDR timing parameters
04	04-May-2017	DIUN	Updated EEPROM map, block diagram and footprint information
03	27-Dec-2016	DIUN	Updates, corrections and additions based on revision 1 modules
02	05-Jul-2016	DIUN	Version 02, preliminary, minor updates and corrections
01	06-Jun-2016	DIUN	Version 01, preliminary

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1 Overview

1.1 General

1.1.1 Introduction

The Mercury+ XU1 SoC module combines the AMD Zynq® UltraScale+ MPSoC (Multiprocessor System-on-Chip) device with DDR4, QSPI, and eMMC memories, as well as PCIe, USB 2.0/3.0, and Gigabit Ethernet interfaces. This module forms a complete and powerful embedded processing system, available in extended and industrial temperature ranges.

The use of the Mercury+ XU1 SoC module, in contrast to building a custom MPSoC hardware, significantly reduces development effort and redesign risk and improves time-to-market for the embedded system.

Together with Mercury+ base boards, the Mercury+ XU1 SoC module allows the user to quickly build a system prototype and start with application development.

1.1.2 Warranty

Refer to the General Business Conditions, available on the Enclustra website [1].

> **Tip**
>
> The warranty of Enclustra modules is void if the FPGA's one-time programmable eFuses are blown. This operation is irreversible. Enclustra cannot test the module in case of a product return.

NOTICE

Data loss or unusable product

The fuses of the FPGA can be blown to activate the user-defined Advanced Encryption Standard (AES). After blowing the fuses, only content encrypted using a specific key can be loaded on the FPGA. Your key is unique and cannot be retrieved in case of loss.

- Keep your key in a secure location.

1.1.3 RoHS

The Mercury+ XU1 SoC module is designed and produced according to the Restriction of Hazardous Substances (RoHS) Directives 2011/65/EU (RoHS 2) and 2015/863/EU (RoHS 3).

1.1.4 Disposal and WEEE

The Mercury+ XU1 SoC module must be properly disposed of at the end of its life.

The Mercury+ XU1 SoC module is not subject to the Waste Electrical and Electronic Equipment (WEEE) Directive (2012/19/EU).

1.1.5 Safety Recommendations and Warnings

Mercury+ modules are not designed to be "ready for operation" for the end-user. These can only be used in combination with suitable base boards. Proper configuration of the hardware before usage is required.

NOTICE

Damage by inserting or removing the module while under power

- Ensure that the power supply is disconnected from the base board before inserting/removing the Mercury+ XU1 SoC module, connecting/disconnecting interfaces, or connecting/disconnecting jumpers.

NOTICE

Damage by touching while under power

Touching the capacitors of the DC-DC converters can lead to voltage peaks and permanent damage.

- Do not touch the capacitors of the DC-DC converters while the power is applied.

1.1.6 Electrostatic Discharge

Electronic boards are sensitive to electrostatic discharge (ESD).

NOTICE

Damage due to electrostatic discharge

Electrostatic discharge (ESD) may damage the Mercury+ XU1 SoC module partially or completely.

- Follow the relevant guidelines for ESD-safe handling when operating or assembling electronic components.
- Ensure that the product is handled with care and only in an ESD-protected environment.

1.1.7 Electromagnetic Compatibility

The Mercury+ XU1 SoC module is a Class A product (as defined in IEC 61000-3-2 standard) and is not intended for use in domestic environments. The product may cause electromagnetic interference, for which appropriate measures must be taken.

1.2 Features

- AMD Zynq® UltraScale+™ MPSoC
  - XCZU6CG/XCZU6EG/XCZU9EG/XCZU15EG device
  - FFVC900 package
  - Dual-/Quad-core ARM® Cortex™-A53 MPCore™ up to 1.5 GHz
  - Dual-core ARM® Cortex™-R5 MPCore™ up to 600 MHz
  - Mali-400 MP2 GPU (not for CG variants)
  - AMD 16nm FinFET+ FPGA fabric
  - 14 ARM peripheral I/Os (SPI, SDIO, CAN, I2C, UART)
  - 200 FPGA I/Os
    - 152 HP I/Os
      - 148 I/Os[1] up to 1.8 V
      - 4 I/Os up to 3.3 V (routed via level shifters)

        - 48 HD I/Os (up to 3.3 V)
    - Up to 20 MGT transceivers
        - 12 GTH transceivers[1]
            - Speed grade 1 devices: 12.5 Gbit/s
            - Other devices: 16.375 Gbit/s
        - 4 GTR transceivers @ 6 Gbit/s
    - Up to 12 reference clock inputs
        - 6 GTH reference clock inputs[1]
        - 4 GTR reference clock inputs
    - PCIe Gen2 ×4 (AMD built-in PCIe hard block using GTR lanes)
- Up to 4 GB DDR4 SDRAM with ECC
- 64 MB quad SPI flash
- 16 GB eMMC flash
- 2 × Gigabit Ethernet PHYs (one PHY shared with one of the USB PHYs)
- 2 × USB 2.0 PHYs
    - PHY0 configured as host or device
    - PHY1 configured as host (shared with one of the Gigabit Ethernet PHYs)
- USB 3.0 (AMD built-in USB 3.0 hard block using GTR lanes)
- Real-time clock
- CAN, UART, SPI, I2C, SDIO/MMC
- Form factor: 76 × 54 mm
- 5 to 15 V supply voltage

1.3 Deliverables

- Mercury+ XU1 SoC module
- Mercury+ XU1 SoC module documentation, available via download:
    - Mercury+ XU1 SoC Module User Manual (this document)
    - Mercury+ XU1 SoC Module Reference Design [2]
    - Mercury+ XU1 SoC Module IO Net Length Excel Sheet [3]
    - Mercury+ XU1 SoC Module FPGA Pinout Excel Sheet [4]
    - Mercury+ XU1 SoC Module FPGA Pinout Assembly Variants Excel Sheet [5]
    - Mercury+ XU1 SoC Module User Schematic (PDF) [6]
    - Mercury+ XU1 SoC Module Known Issues and Changes [7]
    - Mercury+ XU1 SoC Module Footprint (Altium, Eagle, Orcad and PADS) [8]
    - Mercury+ XU1 SoC Module 3D Model (PDF) [9]
    - Mercury+ XU1 SoC Module 3D Model (STEP) [10]
    - Mercury Mars Module Pin Connection Guidelines [11]
    - Mercury Master Pinout [12]
    - Mercury Heat Sink Kits User Manual [22]
- Additional resources, available online:
    - Enclustra Build Environment [17] (Linux build environment; refer to Section 1.3.2 for details)
    - Enclustra Build Environment How-To Guide [18]
    - Petalinux BSP and Documentation [19]
    - Enclustra I2C Application Note [23]
    - Enclustra Gigabit Ethernet Application Note [24]
    - Enclustra ZynqMP Video Application Note [25]
    - Enclustra Secure Boot Reference Design for Zynq Ultrascale+ MPSoC [26]

[1] Starting with revision 3 modules, four additional GTH transceivers and two differential clock pairs may be routed to the module connector using the "G1" assembly variants. With this routing, 128 HP I/Os are available instead of 148 (up to 1.8 V). Refer to Section 3.8.2 for details on the assembly variants and MGT connectivity.

1.3.1 Reference Design

The Mercury+ XU1 SoC Module Reference Design [2] features an example configuration for the Zynq UltraScale+ MPSoC device, together with an example top level HDL file for the user logic.

A bare metal "hello world" application is provided in the reference design. The example shows how to initialize the peripheral controllers and how to access the external devices. Pre-compiled binaries are included in the archive, so that the user can easily check that the hardware is functional.

> **Tip**
>
> To get notified about updates to the Mercury+ XU1 SoC Module Reference Design, turn on the notifications from the Enclustra GitHub page [2].

1.3.2 Enclustra Build Environment

> The Enclustra Build Environment is deprecated. The latest release of the reference design is compatible with AMD tools release 2022.1.

The Enclustra Build Environment (EBE) [17] enables the user to quickly set up and run Linux on any Enclustra SoC module or system board. It allows the user to choose the desired target, and download all the required binaries, such as bitstream and FSBL. It downloads and compiles all required software, such as U-Boot, Linux, and BusyBox based root file system.

The Enclustra Build Environment features a graphical user interface (GUI) and a command line interface (CLI) that facilitates the automatic build flow.

The Enclustra Build Environment How-To Guide [18] describes in more detail how to use the EBE to customize the provided software for the user application. The document provides information on the configuration options for U-Boot, Linux kernel and Buildroot, debugging possibilities for Linux applications, customization of device trees and integration of existing or new kernel drivers.

1.3.3 Petalinux BSP

> The Enclustra Petalinux BSP is deprecated. For reference design releases starting at 2024.2, the Enclustra Yocto BSP layer is provided instead (see Section 1.3.4).

The Enclustra Petalinux BSPs enable the user to quickly set up a Petalinux project and to run Linux on the Enclustra SoC module or system board.

The documentation [19] describes the build process in detail and allows a user without Petalinux knowledge to build and run the desired design on the target hardware.

1.3.4 Yocto BSP Layer

The Enclustra Yocto BSP layer enables the user to quickly set up a Yocto project and to run Linux on the Enclustra SoC module.

The documentation [20] describes the build process in detail and allows a user without Yocto knowledge to build and run a Linux reference design on the target hardware.

1.4 Accessories

1.4.1 Enclustra Heat Sink

For Mercury modules an Enclustra heat sink is available for purchase along with the product. Refer to Section 3.10.6 for further information on the available cooling options.

1.4.2 Mercury+ PE1 Base Board

The Mercury+ PE1 [14] is a versatile PCIe® x4 base board equipped with a multitude of I/O interfaces for use with the Mercury/Mercury+ family of FPGA and SoC modules, providing a head start for building custom FPGA and SoC based hardware systems.

It is compatible with a multitude of FMC boards from different suppliers to use in data acquisition systems, motor control, display and camera interfaces, software defined radio and more. The board is equally well suited for rapid prototyping and for building FPGA systems without designing custom hardware.

The available features depend on the Mercury module type and on the selected base board variant.

1.4.3 Mercury+ PE3 Base Board

The Mercury+ PE3 [16] is a versatile PCIe® x8 base board equipped with a multitude of I/O interfaces for use with the Mercury/Mercury+ family of FPGA and SoC modules, providing a head start for building custom FPGA and SoC based hardware systems.

This high performance base board provides a versatile set of I/O connectivity options, specialized for high-speed communication and video applications, including SFP+, QSFP+, HDMI, USB Type-C and Firefly. The board is equally well suited for rapid prototyping and for building FPGA systems without designing custom hardware.

The available features depend on the Mercury module type and on the selected base board variant.

1.4.4 Mercury+ ST1 Base Board

The Mercury+ ST1 board [15] is a compact, low-cost base board equipped with a multitude of I/O interfaces for use with the Mercury/Mercury+ family of FPGA and SoC modules.

It provides a versatile set of I/O connectivity options, specialized for video applications, including DisplayPort, HDMI, MIPI, and SFP+. The board is equally well suited for rapid prototyping and for building FPGA systems without designing custom hardware.

The available features depend on the Mercury module type and on the selected base board variant.

1.5 AMD Tool Support

The MPSoC devices assembled on the Mercury+ XU1 SoC module are supported by the Vivado ML Enterprise Edition software for which a paid license is required. Contact AMD for further information.

2 Getting Started

This section contains essential information on using the Mercury+ XU1 SoC module.

NOTICE

Damage to the connectors

The connectors of the module and the base board can be damaged if the connectors are not properly aligned during installation.

- Align the connectors carefully before applying force on the module.
- Do not use excessive force to latch the module into the connectors on the base board.

NOTICE

Damage to the device when applying power

The Mercury module could physically be mounted the wrong way around on the base board. The module and the base board can be damaged if the device is powered on while it is connected the wrong way around.

- Ensure that the mounting holes on the base board are aligned with the mounting holes of the module.

NOTICE

Damage to the module by overtightening screws

- Do not use excessive force when tightening the screws.

NOTICE

Damage to the device by using metallic objects for removal

- Do not use metallic object, such as screwdrivers, to remove the module from the base board.
- Remove the module carefully using your fingers to avoid damage.
- If more force is required, always apply it evenly by hand to avoid damage.

2.1 Installing the Module

> **Tip**
>
> A small copper square on the bottom left corner of Enclustra modules is provided as landmark. The same landmark is provided on the Enclustra base boards to help orient the module in the right direction when connecting it.

1. **NOTICE: Damage due to electrostatic discharge (ESD).**
   Ensure that the product is handled in an ESD-protected environment.
2. **NOTICE: Damage by connecting or disconnecting under power.**
   Ensure that the power of the base board is disconnected.
3. **NOTICE: Damage to the device when applying power. The module could physically be mounted the wrong way around on the base board.**
   Identify the correct orientation and position of the module with respect to the base board.
4. **NOTICE: Damage to the connectors. Align the connectors carefully before applying force on the module. Do no use excessive force to latch the module into the connectors on the base board.**
   Align the connectors and press the module onto the base board.
5. **NOTICE: Damage to the module. Do not use excessive force when tightening the screws.**
   If required, use up to four M3 screws to mechanically fasten the module to the base board.

2.2 Removing the Module

1. **NOTICE: Damage due to electrostatic discharge (ESD).**
   Ensure that the product is handled in an ESD-protected environment.
2. **NOTICE: Damage by connecting or disconnecting under power.**
   Ensure that the power of the base board is disconnected.
3. **NOTICE: Damage to the device. Do not use any metallic object to remove the module from the base board.**
   Remove the module carefully using your fingers.

3 Module Description

3.1 Block Diagram

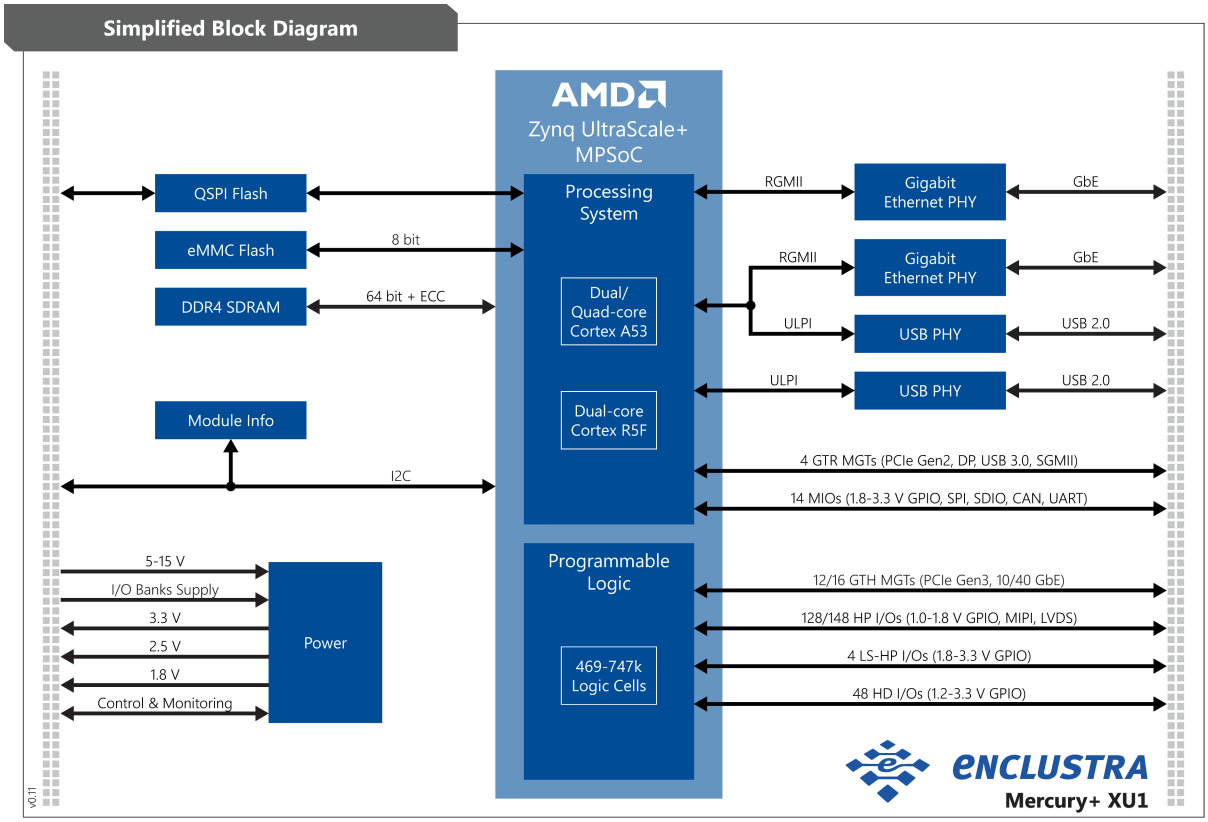

Figure 1: Hardware Block Diagram

The main component of the Mercury+ XU1 SoC module is the AMD Zynq UltraScale+ MPSoC device. Most of its I/O pins are connected to the Mercury+ module connector, making up to 214 regular user I/Os available to the user. Further, up to twenty MGT pairs are available on the module connector, making possible the implementation of several high-speed protocols such as PCIe Gen2 ×4 and USB 3.0 (simultaneous usage of all the interfaces is limited to the available hardware resources i.e. number of transceivers and lane mapping).

The "G1" module variants offer 16 GTH MGT transceivers on the module connector at the trade-off of having only 194 regular I/Os (instead of 214). Section> 3.8.2 describes in more detail the module assembly variants and routing options around the Processing System (PS) and Programmable Logic (PL) transceivers and I/Os.

The MPSoC device can boot from the on-board QSPI flash, from the eMMC flash or from an external SD card. For development purposes, a JTAG interface is connected to Mercury module connector.

The available standard configurations include a 16 GB eMMC flash, a 64 MB quad SPI flash and 2 GB or 4 GB DDR4 SDRAM.

Further, the module is equipped with two Gigabit Ethernet PHYs and two USB 2.0 PHYs, making it ideal for communication applications.

A real-time clock is available on the AMD Zynq UltraScale+ MPSoC device.

On-board clock generation is based on a 33.33 MHz crystal oscillator. In addition, two oscillators delivering 100 MHz and 27 MHz reference clocks for the MGT GTR transceivers are assembled on the module.

The module's internal supply voltages are generated from a single input supply of 5 to 15 V DC. Some of these voltages are available on the Mercury module connectors to supply circuits on the base board.

Five LEDs are connected to the MPSoC pins for status signaling.

3.2 Module Configuration and Product Models

Table 1 describes the available standard module configurations. The product model indicates the module type and main features. Figure 2 describes the fields within the product model. Custom configurations are available. Contact Enclustra for more information.

Product Model	MPSoC[2]	DDR4 SDRAM	DDR4 ECC	GTH MGTs	Temperature Range
ME-XU1-6CG-1E-D11E-G1	XC**ZU6**CG-1FFVC900E	2 GB	•	16	0 to +85°C
ME-XU1-6CG-1E-D11E	XC**ZU6**CG-1FFVC900E	2 GB	•	12	0 to +85°C
ME-XU1-6EG-1I-D11E	XC**ZU6**EG-1FFVC900I	2 GB	•	12	-40 to +85°C
ME-XU1-9EG-3E-D12E	XC**ZU9**EG-3FFVC900E	4 GB	•	12	0 to +85°C
ME-XU1-15EG-1E-D12E-G1	XC**ZU15**EG-1FFVC900E	4 GB	•	16	0 to +85°C
ME-XU1-15EG-2I-D12E	XC**ZU15**EG-2FFVC900I	4 GB	•	12	-40 to +85°C
ME-XU1-15EG-2I-D12E-G1	XC**ZU15**EG-2FFVC900I	4 GB	•	16	-40 to +85°C

Table 1: Standard Module Configurations

Starting with revision 3 modules, 4 additional GTH transceivers and 2 differential clock pairs may be routed to the module connector, by using the "G1" assembly variants. Refer to Section 3.8.2 for details on the assembly variants and MGT connectivity.

[2] The "device" is shown in bold.

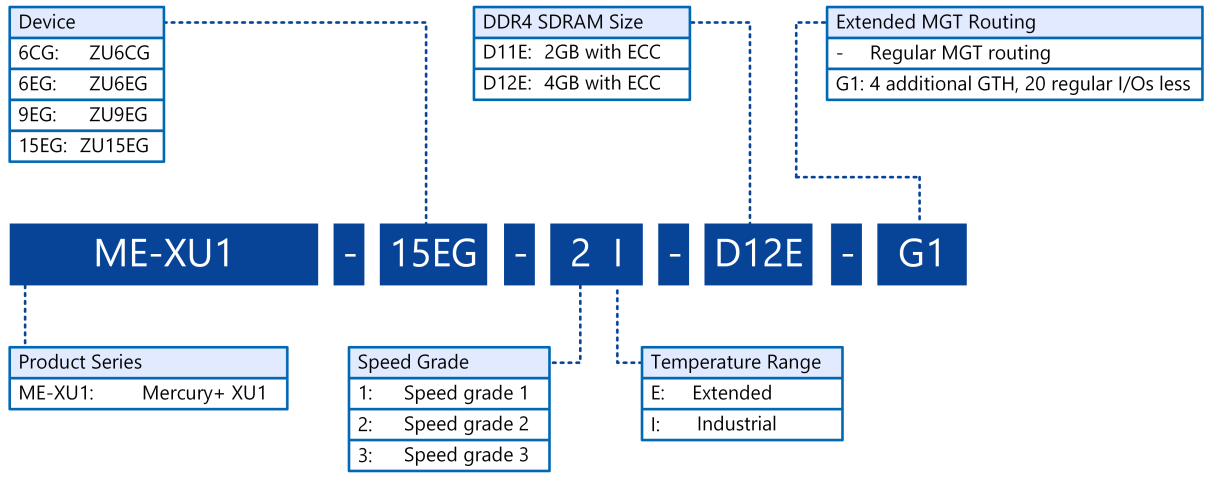

Figure 2: Product Model Fields

For the first revision modules or early access modules, the product model may not respect entirely this naming convention. Contact Enclustra for more information.

3.3 EN-Numbers and Product Models

Every product is uniquely labeled, showing the EN-number and serial number. An example is presented in Figure 3.

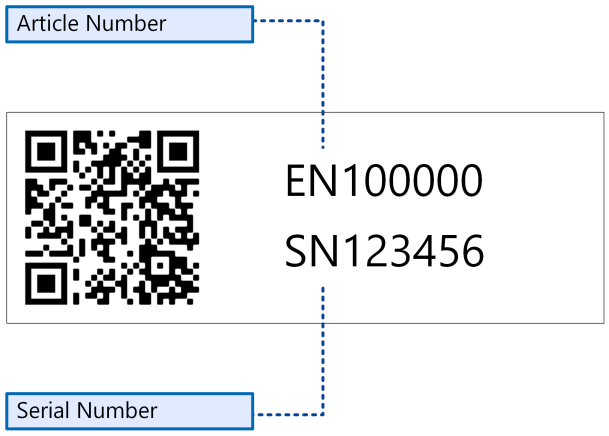

Figure 3: Product Label

The correspondence between EN-number and product model for each revision is shown in Table 2.

The known issues of the product and the changes between the revisions are described in the Mercury+ XU1 SoC Module Known Issues and Changes [7].

EN-Number	Part Name	Revision Number
EN107402	ME-XU1-6EG-1I-D12E-X2	R5.1
EN106107	ME-XU1-15EG-2I-D12E-G1	R5.1
EN106106	ME-XU1-15EG-2I-D12E	R5.1

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EN-Number	Part Name	Revision Number
EN106105	ME-XU1-15EG-1E-D12E-G1	R5.1
EN106104	ME-XU1-9EG-3E-D12E	R5.1
EN106099	ME-XU1-6EG-1I-D11E	R5.1
EN106098	ME-XU1-6CG-1E-D11E-G1	R5.1
EN106097	ME-XU1-6CG-1E-D11E	R5.1
EN105553	ME-XU1-6EG-2E-D11E	R5.0
EN105193	ME-XU1-9EG-3E-D12E	R5.0
EN105192	ME-XU1-9EG-2I-D12E	R5.0
EN105191	ME-XU1-9EG-2I-D12E-G1	R5.0
EN105190	ME-XU1-9EG-1E-D11E-G1	R5.0
EN105183	ME-XU1-6EG-1I-D11E	R5.0
EN105182	ME-XU1-6EG-1I-D11E-G1	R5.0
EN105181	ME-XU1-6CG-1E-D11E	R5.0
EN105180	ME-XU1-6CG-1E-D11E-G1	R5.0
EN105178	ME-XU1-15EG-2I-D12E	R5.0
EN105177	ME-XU1-15EG-2I-D12E-G1	R5.0
EN105176	ME-XU1-15EG-1E-D12E-G1	R5.0
EN105145	ME-XU1-9EG-3E-D12E	R4.2
EN105144	ME-XU1-9EG-2I-D12E	R4.2
EN105143	ME-XU1-9EG-2I-D12E-G1	R4.2
EN105142	ME-XU1-9EG-1E-D11E-G1	R4.2
EN105139	ME-XU1-6EG-1I-D11E	R4.2
EN105138	ME-XU1-6EG-1I-D11E-G1	R4.2
EN105137	ME-XU1-6CG-1E-D11E	R4.2
EN105136	ME-XU1-6CG-1E-D11E-G1	R4.2
EN105134	ME-XU1-15EG-2I-D12E	R4.2
EN105133	ME-XU1-15EG-2I-D12E-G1	R4.2

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EN-Number	Part Name	Revision Number
EN105132	ME-XU1-15EG-1E-D12E-G1	R4.2
EN102614	ME-XU1-6EG-1I-D11E-G1	R4.1
EN102604	ME-XU1-15EG-1E-D12E-G1	R4.1
EN102603	ME-XU1-9EG-2I-D12E-G1	R4.1
EN102602	ME-XU1-9EG-1E-D11E-G1	R4.1
EN102601	ME-XU1-6CG-1E-D11E	R4.1
EN102600	ME-XU1-6CG-1E-D11E-G1	R4.1
EN102376	ME-XU1-15EG-2I-D12E-G1	R4.1
EN102375	ME-XU1-15EG-2I-D12E	R4.1
EN102374	ME-XU1-9EG-3E-D12E	R4.1
EN102373	ME-XU1-9EG-2I-D12E	R4.1
EN102372	ME-XU1-6EG-1I-D11E	R4.1
EN102281	ME-XU1-15EG-2I-D12E	R4.0
EN102280	ME-XU1-9EG-3E-D12E	R4.0
EN102279	ME-XU1-9EG-2I-D12E	R4.0
EN102278	ME-XU1-6EG-1I-D11E	R4.0
EN102117	ME-XU1-15EG-2I-D12E	R3.0
EN102116	ME-XU1-9EG-3E-D12E	R3.0
EN102115	ME-XU1-9EG-2I-D12E	R3.0
EN102114	ME-XU1-6EG-1I-D11E	R3.0
EN102101	ME-XU1-9EG-3E-D12E	R2.0
EN101920	ME-XU1-15EG-2I-D12E	R2.0
EN101919	ME-XU1-9EG-2I-D12E	R2.0
EN101918	ME-XU1-6EG-1I-D11E	R2.0

Table 2: EN-Numbers and Part Names

3.4 Top and Bottom Views

Depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

3.4.1 Top View

Figure 4: Module Top View

3.4.2 Bottom View

Figure 5: Module Bottom View

3.5 Top and Bottom Assembly Drawings

Depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

3.5.1 Top Assembly Drawing

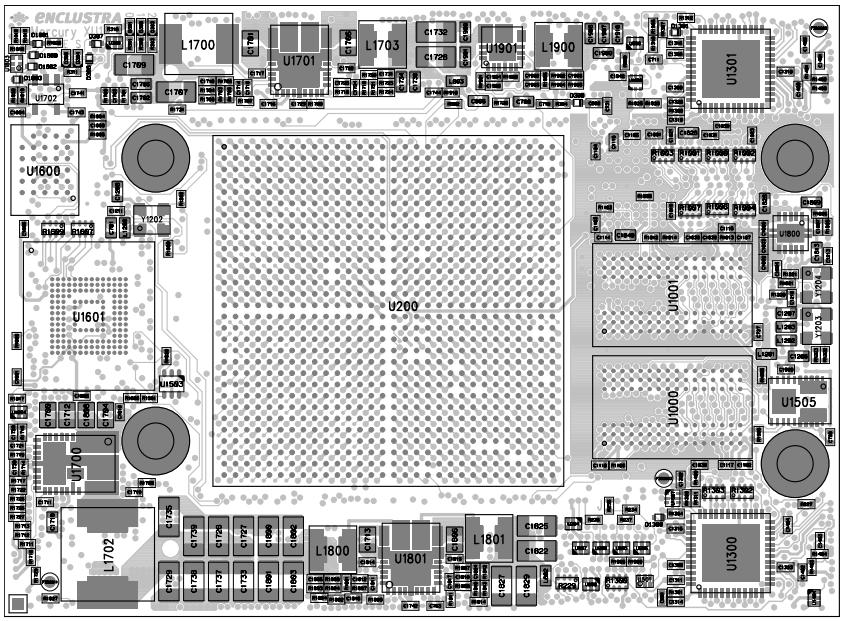

Figure 6: Module Top Assembly Drawing

3.5.2 Bottom Assembly Drawing

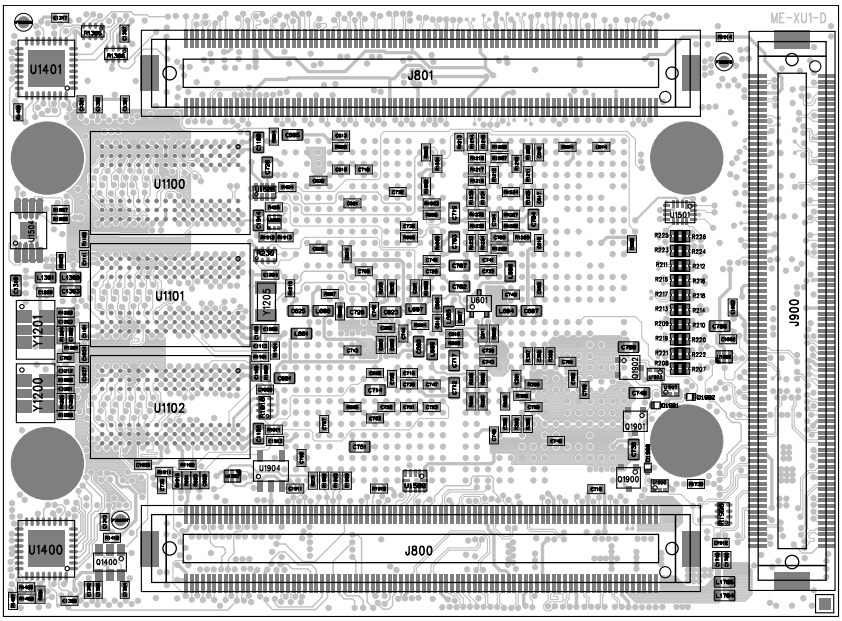

Figure 7: Module Bottom Assembly Drawing

3.6 Module Footprint and Mechanical Data

Figure 8 shows the dimensions of the module footprint on the base board.

Enclustra offers Mercury and Mercury+ modules of various geometries having widths of 56, 64, 65, 72 or 74 mm and having different topologies for the mounting holes. If different module types shall be fixed on the base board by screws, additional mounting holes may be required to accommodate different modules. The footprints of the module connectors for the base board design are available for different PCB design tools (Altium, PADS, Eagle, Orcad) [8] and include the required information on the module sizes and holes.

The maximum component height under the module is dependent on the connector type. Refer to Section 3.7 for detailed connector information.

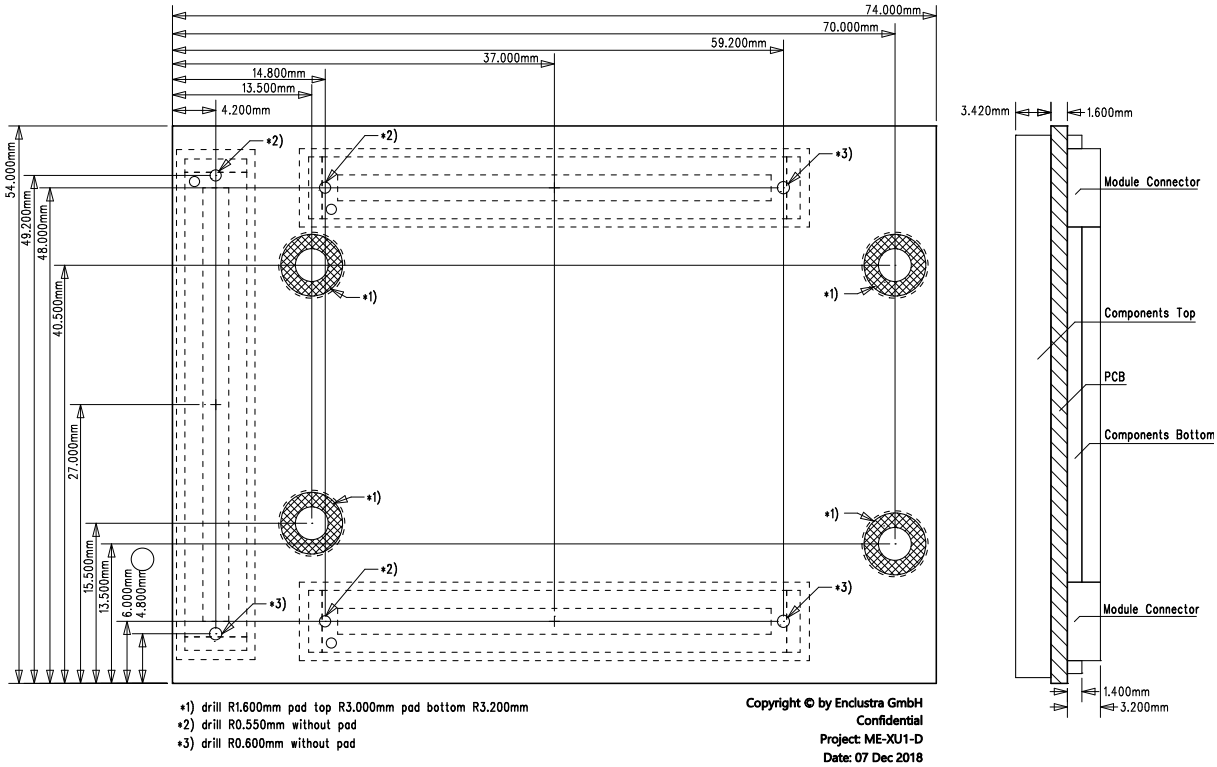

Figure 8: Module Footprint - Top View and Side View

Table 3 describes the mechanical characteristics of the Mercury+ XU1 SoC module. A 3D model (PDF) and a STEP 3D model are available [9], [10].

Parameter	Value
Size	74 × 54 mm
Component height top	3.42 mm
Component height bottom	1.4 mm
Weight	34 g

Table 3: Mechanical Data

3.7 Module Connector

Three Hirose FX10 168-pin 0.5 mm pitch headers with a total of 504 pins have to be integrated on the base board [13]. The pinout of the module connector is found in the Mercury Master Pinout [12]. The connector is available in different packaging options and different stacking heights. Some examples are presented in Table 4. Refer to the connector datasheet for more information.

Component	Part Number	Description
Mercury module connector	FX10A-168S-SV	Hirose FX10, 168-pin, 0.5 mm pitch
Base board connector	FX10A-168P-SV(71)	Hirose FX10, 168-pin, 0.5 mm pitch, 4 mm stacking height
Base board connector	FX10A-168P-SV1(71)	Hirose FX10, 168-pin, 0.5 mm pitch, 5 mm stacking height

Table 4: Module Connector Characteristics

Figure 9 indicates the pin numbering for the Mercury module connectors from the top view of the base board. The connector pins are numbered as follows:

- Connector A: from J800-1 to J800-168
- Connector B: from J801-1 to J801-168
- Connector C: from J900-1 to J900-168

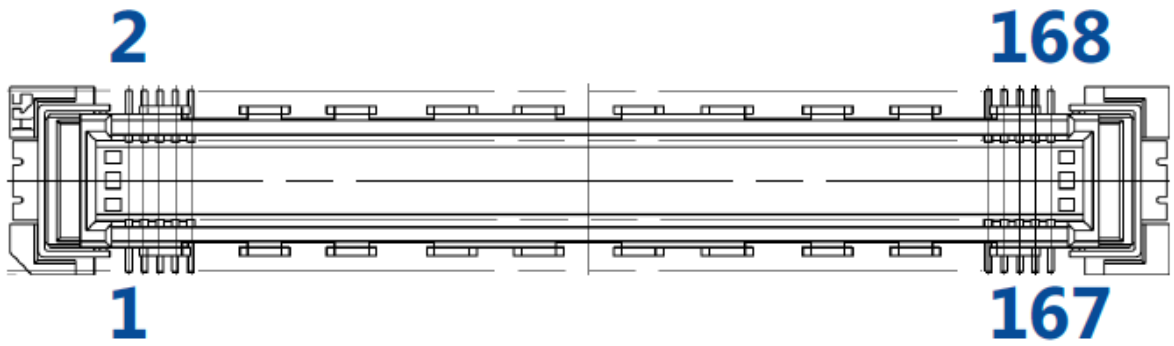

Figure 9: Pin Numbering for the Module Connector

3.8 User I/O

3.8.1 Pinout

Information on the Mercury+ XU1 SoC module pins can be found in the Mercury Master Pinout [12], and in the additional document Mercury Mars Module Pin Connection Guidelines [11].

> **Tip**
>
> The pin types on the schematic of the module connector and in the master pinout document are for reference only. On the Mercury+ XU1 SoC module, the connected pins might not have the targeted functions (such as primary clocks, differential pins, transceiver signals, etc).

Tip

The availability of certain pins might depend on the product model.

The naming convention for the user I/Os is:
IO_B<BANK>_L<PAIR_NUMBER>_<SPECIAL_FUNCTION>_<PACKAGE_PIN>_<POLARITY>.

For example, IO_B64_L18_AD2_AH4_P is located on pin AH4 of I/O bank 64, pair 18, it is a System Monitor differential auxiliary analog input capable pin and it has positive polarity, when used in a differential pair.

The global clock capable pins are marked with "GC" (HP I/O banks) or with "HDGC" (HD I/O banks) in the signal name. For details on their function and usage, refer to the AMD documentation.

Table 5 includes information related to the total number of I/Os available in each I/O bank and possible limitations.

Signal Name	Signals	Pairs	Differential	Single-ended	Bank	Bank Type[3]
IO_B64_<...>	52	24	In/Out	In/Out	64	HP
IO_B65_<...>	50	24	In/Out	In/Out	65	HP
IO_B66_<...>	50	24	In/Out	In/Out	66	HP
IO_B47_<...>	24	12	In/Out (no LVDS/LVPECL outputs supported; internal differential termination not supported) Refer to Section 3.8.3 for details.	In/Out	47	HD
IO_B48_<...>	24	12	In/Out (no LVDS/LVPECL outputs supported; internal differential termination not supported) Refer to Section 3.8.3 for details.	In/Out	48	HD
Total	**200**	**96**	–	–	–	–

Table 5: User I/Os

On the "G1" variants with 16 GTH transceivers, not all I/Os listed in Table 5 are available on the module connector. Certain user I/Os on the module connectors can be connected to various MPSoC I/Os, depending on the product variant. Section 3.8.2 lists and describes the connectivity for these pins for each assembly variant. The multi-use signals on the module connector are not named according to the naming convention described above.

The multi-gigabit transceiver (MGT) are described in Section 3.9.

[3] HD = high density pins, HP = high performance pins. Refer to the Zynq UltraScale+ MPSoC Data Sheet: Overview [32] for details.

3.8.2 I/O Pin Exceptions

The I/O pin exceptions are pins with special functions or restrictions (for example, when used in combination with certain Mercury boards they may have a specific role).

PCIe Reset Signal (PERST#)

Table 6 lists the I/O pin exceptions on the Mercury+ XU1 SoC module related to the PCIe reset connection.

I/O Name	Module Connector Pin	Description
PS_MIO42_PERST#	A104	Connected to ETH0_TXD3_PERST# and PL_PERST# via switches, series resistors, and a level shifter. Refer to the Mercury+ XU1 SoC Module User Schematic for details.

Table 6: I/O Pin Exceptions - PERST#

When the Mercury+ XU1 SoC module is used in combination with a Mercury+ PE1 base board as a PCIe device, the low value of the PERST# signal coming from the PCIe edge connector on the module connector pin A-104 (PS_MIO42_PERST#) pulls the ETH0_TXD3_PERST# (MIO[30]) to ground via a 1 kΩ resistor.

MIO[30] is the default pin used for the reset signal of the PCIe PS built-in block, therefore it was chosen for the reset implementation. The Ethernet controller 0 is disabled when the PCIe hard block is used. Any other valid position for PERST# would have resulted in having the Ethernet controller disabled.

In situations in which PCIe functionality is not required, PS_MIO42_PERST# pin can be used in the same manner as a regular MIO pin.

For root complex applications the PERST# signal can be placed on any unused MIO pin (the restriction on MIO[30,42] does not apply in this case).

I/O Pins with Level Shifter

There are four signals on the Mercury+ XU1 SoC module that are routed from the FPGA banks to the module connector via level shifters. These are presented in Table 7.

I/O Name	Module Connector Pin	Description
IO_B64_AG4_LS	A88	These pins have a level shifter from VCC_IO_B64 to VCC_CFG_MIO.
IO_B64_AJ1_LS	A90	
IO_B64_AH11_LS	A92	
IO_B64_AG9_LS	A94	

Table 7: I/O Pin Exceptions - Level Shifters

The level shifters used for the I/O pins mentioned in Table 7 are NXP NTB0104 and the maximum achievable data rate on these pins is 40 Mbit/s. The level shifter requires the VCC_IO_B64 to be greater or equal to 1.2 V. Refer to the level shifter datasheet for details. For VCC_IO_B64 voltages below 1.2 V, the level shifted signals are not operational.

Assembly Variants and Migration between Modules

Starting with revision 3 modules, four additional GTH transceivers and two differential clock pairs may be routed to the module connector, by using the "G1" assembly variants. This option may be useful when

the user application requires 16 GTH transceivers and less regular I/Os.

Table 8 presents the assembly variants for different product configurations. The signals on the module connector are routed to different types of I/Os, depending on the product variant. To find out where exactly these pins are routed, refer to the naming conventions for regular user I/Os (Section 3.8.1) and for MGT signals (Section 3.9). Table 8 is also available in a separate file, FPGA Pinout Assembly Variants Excel Sheet [5].

Figures 10 and 11 depict the assembly variants information. The default option is marked in bold.

Design support files such as the Mercury Master Pinout [12], Mercury+ XU1 SoC Module User Schematic [6], and Mercury+ XU1 SoC Module FPGA Pinout Assembly Variants Excel Sheet [5] offer additional information on assembly variants and migration guidelines. In the user schematic, this information is depicted in the "Component Assembly" section at the end of the PDF file (MGT_SEL).

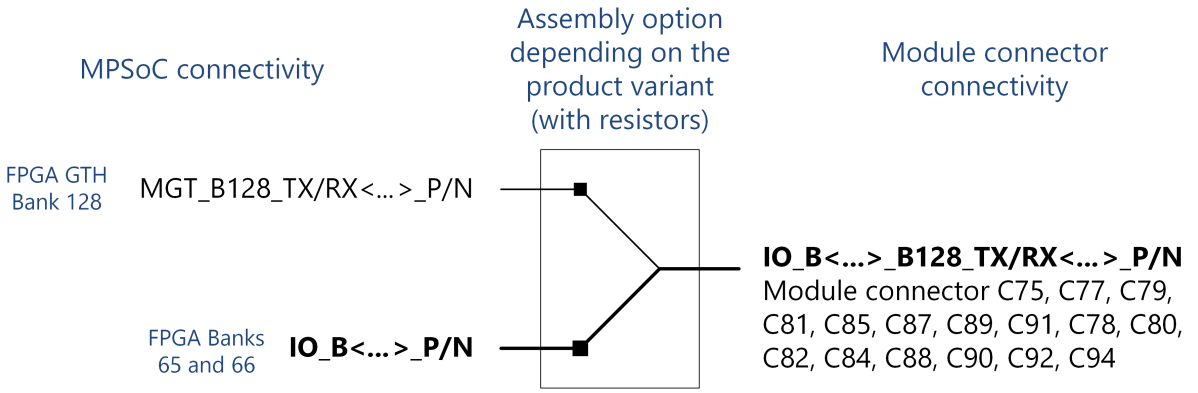

Figure 10: Assembly Options for MGT TX/RX Signals

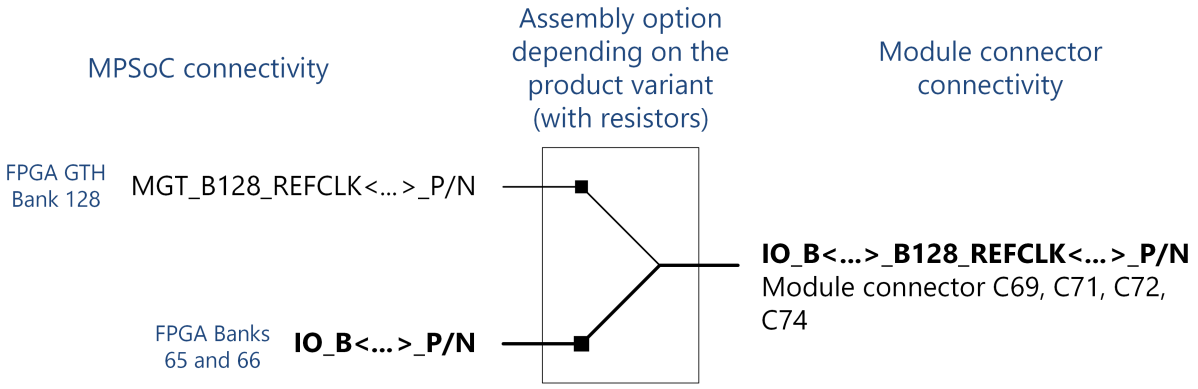

Figure 11: Assembly Options for MGT REFCLK Signals

Module Variant		**Default Assembly Variant**	**"G1" Assembly Variant**
Compatibility		**ME-XU1-R1/R2**	**ME-XU7/ME-XU8**
Signal Name	**Pin**	**MPSoC Pin Connectivity**	
IO_B66_Y10_B128_REFCLK0_F25_P	C69	IO_B66_Y10	MGT_B128_REFCLK0_F25_P
IO_B66_N11_B128_REFCLK0_F26_N	C71	IO_B66_N11	MGT_B128_REFCLK0_F26_N

Continued on next page...

Module Variant		Default Assembly Variant	"G1" Assembly Variant
Compatibility		ME-XU1-R1/R2	ME-XU7/ME-XU8
Signal Name	Pin	MPSoC Pin Connectivity	
IO_B66_L5_AD14_U2_B128_TX0_G27_P	C75	IO_B66_L5_AD14_U2_P	MGT_B128_TX0_G27_P
IO_B66_L5_AD14_U3_B128_TX0_G28_N	C77	IO_B66_L5_AD14_U3_N	MGT_B128_TX0_G28_N
IO_B66_L4_AD7_V2_B128_TX1_E27_P	C79	IO_B66_L4_AD7_V2_P	MGT_B128_TX1_E27_P
IO_B66_L4_AD7_V1_B128_TX1_E28_N	C81	IO_B66_L4_AD7_V1_N	MGT_B128_TX1_E28_N
IO_B66_L3_AD15_W2_B128_TX2_C27_P	C85	IO_B66_L3_AD15_W2_P	MGT_B128_TX2_C27_P
IO_B66_L3_AD15_W1_B128_TX2_C28_N	C87	IO_B66_L3_AD15_W1_N	MGT_B128_TX2_C28_N
IO_B66_L11_GC_V7_B128_TX3_A27_P	C89	IO_B66_L11_GC_V7_P	MGT_B128_TX3_A27_P
IO_B66_L11_GC_V6_B128_TX3_A28_N	C91	IO_B66_L11_GC_V6_N	MGT_B128_TX3_A28_N
IO_B65_AE7_B128_REFCLK1_D25_P	C72	IO_B65_AE7_P	MGT_B128_REFCLK1_D25_P
IO_B65_AE1_B128_REFCLK1_D26_N	C74	IO_B65_AE1_N	MGT_B128_REFCLK1_D26_N
IO_B65_L5_AD14_AA12_B128_RX0_H29_P	C78	IO_B65_L5_AD14_AA12_P	MGT_B128_RX0_H29_P
IO_B65_L5_AD14_AA11_B128_RX0_H30_N	C80	IO_B65_L5_AD14_AA11_N	MGT_B128_RX0_H30_N
IO_B65_L4_AD7_AC11_B128_RX1_F29_P	C82	IO_B65_L4_AD7_AC11_P	MGT_B128_RX1_F29_P
IO_B65_L4_AD7_AD11_B128_RX1_F30_N	C84	IO_B65_L4_AD7_AD11_N	MGT_B128_RX1_F30_N
IO_B65_L11_GC_AC7_B128_RX2_D29_P	C88	IO_B65_L11_GC_AC7_P	MGT_B128_RX2_D29_P
IO_B65_L11_GC_AD7_B128_RX2_D30_N	C90	IO_B65_L11_GC_AD7_N	MGT_B128_RX2_D30_N
IO_B65_L3_AD15_AD12_B128_RX3_B29_P	C92	IO_B65_L3_AD15_AD12_P	MGT_B128_RX3_B29_P
IO_B65_L3_AD15_AE12_B128_RX3_B30_N	C94	IO_B65_L3_AD15_AE12_N	MGT_B128_RX3_B30_N

Table 8: Assembly Options for MGT Signals and Migration Guidelines

3.8.3 Differential I/Os

When using differential pairs, a differential impedance of 100 Ω must be matched on the base board, and the two nets of a differential pair must have the same length.

The information regarding the length of the signal lines from the MPSoC device to the module connector is available in Mercury+ XU1 SoC Module IO Net Length Excel Sheet [3]. This enables the user to match the total length of the differential pairs on the base board if required by the application.

> **Tip**
>
> The trace length of various signals may change between revisions of the Mercury+ XU1 SoC module. Use the information provided in the Mercury+ XU1 SoC Module IO Net Length Excel Sheet [3] to check which signals are affected. The differential signals will also be routed differentially in subsequent product revisions.

The HD bank I/Os cannot be used as LVDS/LVPECL outputs, but they can still be used as LVDS/LVPECL differential inputs.

For information about signal terminations, refer to Section 3.8.6.

3.8.4 I/O Banks

Table 9 describes the main attributes of the Programmable Logic (PL) and Processing System (PS) I/O banks, and indicates which peripherals are connected to each I/O bank. All I/O pins within a particular I/O bank must use the same I/O voltage (VCC_IO) and reference voltage (VREF) .

Bank	Bank Type	Connectivity	VCC_IO	VREF
MGT Banks				
228	MGT	Module connector	0.9 V	–
229	MGT	Module connector	0.9 V	–
230	MGT	Module connector	0.9 V	–
128[4]	MGT	Module connector[4]	0.9 V	–
PL I/O Banks				
64	HP	Module connector	VCC_IO_B64, user selectable	½ × VCC_IO_B64
65	HP	Module connector[4]	VCC_IO_B65, user selectable	½ × VCC_IO_B65
66	HP	Module connector[4]	VCC_IO_B66, user selectable	½ × VCC_IO_B66
47	HD	Module connector	VCC_IO_B47, user selectable	–
48	HD	Module connector	VCC_IO_B48, user selectable	–
PS Banks				
500	PS MIO	eMMC and QSPI flash devices, I2C, LEDs	1.8 V	–
501	PS MIO	Module connector, Gigabit Ethernet PHY 0	VCC_CFG_MIO, user selectable	–
502	PS MIO	USB PHY 0, USB PHY 1 / Gigabit Ethernet PHY 1 (shared lines)	1.8 V	–
503	PS CONFIG	FPGA PS Configuration	VCC_CFG_MIO, user selectable	–
504	PS DDR	DDR4 SDRAM	1.2 V	–
505	PS GTR	Module connector, GTR oscillators	VCC_0V85	–

Table 9: I/O Banks

[4]The MGTs in bank 128 are available on the module connector only on "G1" assembly variants. On these variants, certain I/Os from banks 65 and 66 are not routed to the module connector. Check the assembly variants description in Section 3.8.2.

3.8.5 VCC_IO Usage

The VCC_IO voltages for the I/O banks located on the module connector are configurable by applying the required voltage to the VCC_IO_B[x], respectively VCC_CFG_MIO pins. All VCC_IO_B[x] or VCC_CFG_MIO pins in a given bank must be connected to the same voltage.

For compatibility with other Enclustra Mercury modules, it is recommended to use a single I/O voltage per module connector.

Signal Name	MPSoC Pins	Supported Voltages	Connector A Pins	Connector B Pins	Connector C Pins
VCC_CFG_MIO	VCCO_PSIO1_501, VCCO_PSIO3_503	1.8 V – 3.3 V ±5%	A74, A77	–	–
VCC_IO_B64	VCCO_64	1.0 V[5] – 1.8 V ±5%	–	–	C76, C116, C158
VCC_IO_B65	VCCO_65	1.0 V – 1.8 V ±5%	–	B64, B88, B140	–
VCC_IO_B66	VCCO_66	1.0 V[6] – 1.8 V ±5%	–	B67, B95, B143	–
VCC_IO_B47	VCCO_47	1.2 V – 3.3 V ±5%[7]	A41	–	–
VCC_IO_B48	VCCO_48	1.2 V – 3.3 V ±5%[7]	A38	–	–

Table 10: VCC_IO Pins

If the Mercury+ XU1 SoC module is used in combination with a base board having only two module connectors, the VCC_IO_B64 pin that powers I/O bank 64 is connected to the on-board generated 1.8 V supply voltage.

Figure 12 illustrates the requirements of the VCC_IO power sequence. Do not power the VCC_IO pins when PWR_GOOD and PWR_EN signals are not active. If the module is not powered, make sure that the VCC_IO voltages are disabled, for example, by using a switch that uses PWR_GOOD as enable signal on the base board.

[5] There are limitations on the I/Os from bank 64 routed via level shifters when VCC_IO_B64 is less than 1.2 V. Refer to Section 3.8.2 for details.

[6] When using voltages lower than 1.8 V for VCC_IO_B66, the I2C bus on FPGA bank 66 is not operational (I2C on PL side is available starting with revision 2).

[7] For voltages of 3.3 V for VCC_IO_B47 and VCC_IO_B48 the tolerance range is -5% to +3%.

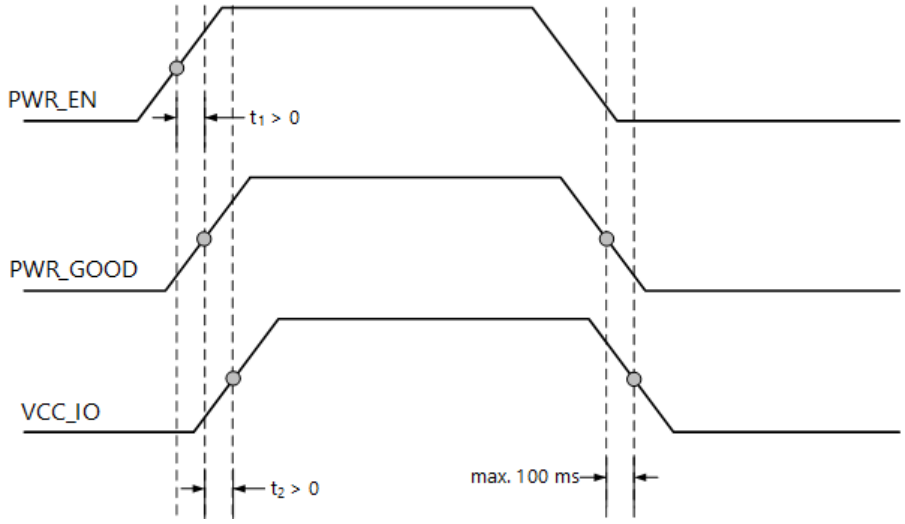

Figure 12: Power-Up Sequence - VCC_IO in Relation with PWR_GOOD and PWR_EN Signals

NOTICE

Damage to the device due to unsuitable voltage

Unsuitable voltages may damage the MPSoC device as well as other devices on the Mercury+ XU1 SoC module.

- Only use VCC_IO voltages compliant with the assembled MPSoC device.

NOTICE

Damage to the device due to floating VCC_IO pins

Floating VCC_IO pins reduce ESD protection.

- Do not leave any VCC_IO pin floating.

⚠ CAUTION

Injury due to uncontrolled device

If an I/O is connected to an external device, violating the power sequence or leaving the corresponding VCC_IO pin floating will leave the pin in an undefined state. This can lead to any behavior of the devices attached to this pin and, potentially, to damage or injuries.

- Follow the power sequence diagram shown in Figure 12. This ensures that the I/Os are tri-stated at power-on and power-off.
- Do not leave VCC_IO pins floating.

3.8.6 Signal Terminations

Differential Inputs

Internal differential termination is not supported for the HD pins (banks 47, 48). All differential signal pairs from both HD banks may optionally be equipped with 100 Ω differential termination resistors on

the module.

The resistor identifiers for each differential input pair can be retrieved from the Mercury+ XU1 SoC Module User Schematic [6].

Single-Ended Outputs

There are no series termination resistors on the Mercury+ XU1 SoC module for single-ended outputs. If required, series termination resistors may be assembled on the base board (close to the module pins).

3.8.7 Multiplexed I/O (MIO) Pins

Details on the MIO/EMIO terminology are available in the Zynq UltraScale+ Device Technical Reference Manual [27].

Some of the MIO pins on the Mercury+ XU1 SoC module are connected to on-board peripherals, while others are available as GPIOs. The suggested functions below are for reference only. Always verify your MIO pinout with the AMD device handbook.

Table 11 gives an overview over the MIO pin connections on the Mercury+ XU1 SoC module. Only the pins marked with "user functionality" are available on the module connector.

MIO Pins	Function(s)	Connection(s)
[0:5]	QSPI flash Trace interface	QSPI flash Debug connector[8]
[6]	QSPI feedback clock Trace interface (cont.)	–[9] Debug connector[8]
[7:9]	Trace interface (cont.)	Debug connector[8]
[10:11]	I2C	On-SoM I2C bus; connected to the PL HP Bank 66 and also exposed to the module connector (A111, A113) and debug connector[8] through a level shifter.
[12]	I2C interrupt PJTAG interface	On-board I2C bus Debug connector[8]
[13:15]	eMMC flash PJTAG interface (cont.)	eMMC flash Debug connector[8]
[16:22]	eMMC flash (cont.)	eMMC flash
[23]	USB PHY 1 reset	USB 2.0 PHY 1
[24]	LED0 Debug UART TX[10]	LED0 Debug connector[8]
[25]	LED1 Debug UART RX[10]	LED1 Debug connector[8]
[26:29,31:37]	Ethernet 0	Gigabit Ethernet PHY 0
[30]	Ethernet 0 (cont.) PS PCIe block PERST# signal[11]	Gigabit Ethernet PHY 0 Module connector via series resistor
[38]	UART RX[10]	Module connector

Continued on next page...

MIO Pins	Function(s)	Connection(s)
	User functionality	
[39]	UART TX[10] User functionality	Module connector
[40:41,43:44]	User functionality	Module connector
[42]	User functionality PS PCIe block PERST# signal[11]	Module connector
[45:51]	SD card User functionality	Module connector
[52:63]	USB 0	USB 2.0 PHY 0
[64:75]	Ethernet 1 USB 1	Gigabit Ethernet PHY 1 USB 2.0 PHY 1
[76:77]	Ethernet MDIO	Gigabit Ethernet PHY 1 and PHY 0 via level shifter

Table 11: MIO Pins Connections Overview

3.8.8 Analog Inputs

The Zynq UltraScale+ MPSoC devices contain a system monitor in the PL and an additional system monitor block in the PS. These are used to sample analog inputs and to collect information on the internal voltages and temperatures.

The system monitor block in the PL provides a 10-bit ADC, which supports up to 17 external analog lines (1 dedicated differential input, 16 auxiliary differential inputs). The auxiliary analog lines of the MPSoC device are available on the module connector. These I/Os have the abbreviation "AD" followed by the ADC channel in the signal name. The ADC lines are always used differentially. For single-ended applications, the *_N line must be connected to ground. The dedicated channel is not available on the module connector.

The analog input signals can be connected to any normal I/O FPGA bank, provided that all analog pins belong to the same bank. Note that the HD I/O banks have a limited number of analog inputs and they must be connected directly to the SYSMONE4 primitive instead of to the AMD System Management Wizard IP core.

For detailed information on the ADC and system monitor, refer to the UltraScale Architecture System Monitor document [29], Zynq UltraScale+ Device Technical Reference Manual [27] and System Management Wizard Product Guide [30].

Table 12 presents the ADC Parameters for the PL System Monitor (SYSMON). The PS System Monitor is only used for monitoring the on-chip power supply voltages and die temperature.

[8] Starting with revision 3, the PJTAG, TRACE, and debug UART interfaces to debug connector are not supported anymore. Refer to Section 3.24 for details.

[9] This pin is intentionally left unconnected to allow enabling the QSPI "Feedback Clk" and achieving QSPI transfer speeds greater than 40 MHz. Refer to the Zynq UltraScale+ Device Technical Reference Manual [27] for more information.

[10] UART RX is an MPSoC input; UART TX is an MPSoC output.

[11] Used for PCIe PERST# connection implementation. Refer to Section 3.8.2 for details.

Parameter	Value (PL SYSMON)
VCC_ADC	1.8 V
VREF_ADC	Internal
ADC Range	0-1 V
Sampling Rate per ADC	0.2 MSPS
Total number of channels available on the module connector	16 (only auxiliary inputs)

Table 12: System Monitor (PL) Parameters

3.9 Multi-Gigabit Transceiver (MGT)

There are two types of multi-gigabit transceivers available on the Mercury+ XU1 SoC module: GTH transceivers (connected to the PL) and GTR transceivers (connected to the PS).

Tip

For optimal performance of high-speed interfaces, for example, PCIe, use redrivers on the base board.

Tip

The maximum data rate on the transceivers on the Mercury+ XU1 SoC module depends on the routing path for these signals. When using transceivers at high performance rates, ensure adequate signal integrity over the full signal path.

NOTICE

Damage to the transceivers

No AC coupling capacitors are placed on the Mercury+ XU1 SoC module on the transceivers.

- If required by your application, ensure that capacitors are mounted on the base board, close to the module pins.

GTH Transceivers

There are 12 GTH MGTs available on the Mercury+ XU1 SoC module organized in three FPGA banks. Table 13 describes the connections.

The naming convention for the GTH MGT I/Os is:
MGT_B<BANK>_<FUNCTION>_<PACKAGE_PIN>_<POLARITY>.

For example, MGT_B228_TX2_M5_N is located on pin M5 of MGT I/O bank 228, it is a transmit pin and it has negative polarity.

Starting with revision 3 modules, 4 additional GTH transceivers and 2 differential clock pairs may be routed to the module connector, by using the "G1" assembly variants. Refer to Section 3.8.2 for details on the assembly variants and MGT connectivity.

Signal Name	Signal Description	Pairs	I/O Bank
MGT_B228_RX<...>	MGT receivers	4	228
MGT_B228_TX<...>	MGT transmitters	4	
MGT_B228_REFCLK<...>	MGT reference input clocks	2	
MGT_B229_RX<...>	MGT receivers	4	229
MGT_B229_TX<...>	MGT transmitters	4	
MGT_B229_REFCLK<...>	MGT reference input clocks	2	
MGT_B230_RX<...>	MGT receivers	4	230
MGT_B230_TX<...>	MGT transmitters	4	
MGT_B230_REFCLK<...>	MGT reference input clocks	2	
MGT_B128_RX<...>[12]	MGT receivers	4	128
MGT_B128_TX<...>[12]	MGT transmitters	4	
MGT_B128_REFCLK<...>[12]	MGT reference input clocks	2	
Total		**30 (40 on "G1" assembly variants)**	

Table 13: MGT Pairs

Eight of the GTH pairs and four corresponding clocks are routed to module connector C, while four GTH pairs and two reference input clock differential pairs are routed to module connector B. On "G1" assembly variant, four additional GTH pairs may be routed to module connector C. Refer to Section 3.8.2 for details.

The GTH MGTs on the MPSoC device support data rates of 12.5 Gbit/s on speed grade 1 devices and of 16.375 Gbit/s on the other devices. Hirose has removed the bandwidth limitation to 15 Gbit/s from the past, thefore the maximum MPSoC performance may be achieved.

GTR Transceivers

There are four GTR MGT pairs and two reference input clock differential pairs on the Mercury+ XU1 SoC module connected to I/O bank 505. These are routed to module connector B.

The naming convention for the GTR MGT I/Os is:
MGTPS_<FUNCTION>_<PACKAGE_PIN>_<POLARITY>.

For example, MGTPS_RX2_M30_N is located on pin M30 of PS GTR bank (bank 505), it is a receive pin and it has negative polarity.

All Mercury+ XU1 SoC module variants support the implementation of a PCIe Gen2 ×4 interface.

When the PCIe hard block is used, it is not possible to use the Ethernet 0 interface. Ethernet PHY 0 is connected to ETH 0 controller from the PS I/O bank 501. One of the Ethernet TX data signals is shared with the PCIe reset signal (PERST#). Refer to Sections 3.8.2 and 3.8.7 for details on the PERST# connection.

[12] "G1" assembly variant available starting with revision 3.

The GTR pairs support data rates of 6 Gbit/s and can be used for the implementation of several interfaces such as PCIe Gen2 ×4, USB 3.0, DisplayPort, SATA, or Ethernet SGMII. Refer to the Zynq UltraScale+ Device Technical Reference Manual [27] and to the Zynq UltraScale+ MPSoC Data Sheet: Overview [32] for details.

A 100 MHz LVDS oscillator and a 27 MHz CMOS oscillator provide reference clock inputs to the PS GTR bank 505. Refer to Section 3.11 for details.

3.10 Power

3.10.1 Power Generation Overview

The Mercury+ XU1 SoC module uses a 5 V to 15 V DC power input for generating the on-board supply voltages. The power output pins of the module are accessible on the module connector.

On revision 3, the Mercury+ XU1 SoC module underwent a major redesign of the power circuitry in order to support all MPSoC device speed grades, increase performance, and support power converter synchronization for noise-sensitive applications. The power converter synchronization is not supported anymore starting from revision 4.2 due to the usage of a new generation of power converters.

Table 14 describes the power supplies generated on the module.

Generated Supply Name	Voltage Value	Rated Current	Source Supply Name	Shut down via PWR_EN	Influences PWR_GOOD
VCC_INT	0.72 V[13]/0.85 V/0.9 V (PL core supply)	35 A[14]	VCC_MOD	Yes	Yes
VCC_PSINT	0.85 V/0.9 V (PS core supply)	6 A[14]	VCC_MOD	Yes	Yes
VCC_0V85[15]	0.85 V (GTR transceiver supply)	0.5 A	VCC_1V2	Yes	No
VCC_0V9	0.9 V	6 A[16]	VCC_MOD[16]	Yes	Yes
VCC_1V2	1.2 V	6 A[17]	VCC_MOD[17]	Yes	Yes
VCC_BAT_FPGA[18]	1.5 V[19]	10 mA	VCC_BAT	No	No
VCC_1V8	1.8 V	3 A[20]	VCC_MOD[20]	Yes	Yes
VCC_2V5	2.5 V	0.5 A	VCC_3V3	Yes[21]	No
VCC_3V3	3.3 V	6 A[22]	VCC_MOD	No	Yes
VCC_5V0	5.0 V	0.15 A	VCC_MOD	No	No

Table 14: Generated Power Supplies

In the standard configuration, the PL core supply is 0.85 V. For configurations in which a speed grade -3E MPSoC device is assembled, an assembly option is available to switch the PL core operating voltage to 0.9 V. Similarly, in situations in which a speed grade -2LE or -1LI device is used, an assembly option is available to switch the PL core operating voltage to 0.72 V.

In the standard configuration, the PS core supply is 0.85 V. For configurations in which a speed grade -3E MPSoC device is assembled, an assembly option is available to switch the PS core operating voltage to 0.9 V.

PS and PL operation at 0.9 V is not supported on modules revision 1 and 2. Refer to the Mercury+ XU1 SoC Module Known Issues and Changes [7] for details.

Refer to the Mercury Mars Module Pin Connection Guidelines [11] for general rules on the power pins.

Power Converter Synchronization

Starting with revision 4.2 modules, the switching converters used on the Mercury+ XU1 SoC module are upgraded to a newer version due to end of life of the original parts. They do not support synchronization of the switching frequency with any clock signal anymore.

Table 15 presents the control signals that were used for the power converter synchronization in revisions 3 to 4.1, and how they should be connected starting from revision 4.2.

Signal	MPSoC Pin	Package Pin	Description
PWR_SYNC_EN#	MIO[7]	A18	Reserved. This pin is equipped with a pull-up resistor to 1.8 V. Leave this pin floating or drive it high to use the default switching frequencies as specified in the schematic.
LED2#_PWR_SYNC	–	AE8	Multi-function FPGA pin. When PWR_SYNC_EN# is high (default configuration), this pin is connected to LED2#.

Table 15: Power Converter Synchronization

3.10.2 Power Enable / Power Good

The Mercury+ XU1 SoC module provides a power enable input on the module connector. This input may be used to shut down the module's internal supply voltages when required. The list of supply voltages that can be disabled via PWR_EN signal is provided in Section 3.10.1.

[13] Starting with revision 3, 0.72 V core voltage is supported.
[14] On modules revision 1 and 2, the PL and PS core supplies were combined in a single power rail rated 20 A.
[15] Starting with revision 3 modules, an LDO is used to generate the GTR transceiver supply, when a -1LI, -2LE, or -3E speed grade MPSoC device is used. For the other speed grades, VCC_INT is used.
[16] On modules revision 1 and 2 the VCC_0V9 supply is rated 2 A and is using VCC_3V3 as input.
[17] On modules revision 1 and 2 the 1.2 V supply required for the MPSoC device, DDR components and Gigabit Ethernet PHYs is separated into two separate power rails VCC_1V2 and VCC_1V2M both rated 2 A and using VCC_3V3 as voltage input.
[18] Starting with revision 2 modules, an LDO is used to generate the battery voltage for the built-in RTC.
[19] For modules of revision 2 to 4, the LDO voltage is 1.2 V.
[20] On modules revision 1 and 2 the VCC_1V8 supply is rated 2 A and is using VCC_3V3 as input.
[21] On revision 1 modules, the 2.5 V converter cannot be disabled via PWR_EN signal.
[22] On modules revision 1 and 2 the VCC_3V3 supply is rated 9 A.

The PWR_EN input is pulled to VCC_3V3 on the Mercury+ XU1 SoC module with a 10 kΩ resistor. The PWR_GOOD signal is pulled to VCC_3V3 on the Mercury+ XU1 SoC module with a 10 kΩ resistor.

PWR_GOOD is an open collector signal and must not be used to drive a load directly. This signal is pulled to ground if the onboard power converters fail or if the module is disabled via PWR_EN. The list of converters that influence the state of the PWR_GOOD signal is provided in Section 3.10.1.

The role of PWR_GOOD and PWR_EN on the VCC_IO power sequence is presented in Section 3.8.5.

NOTICE

Damage to the device due to unsuitable voltage

Appling unsuitable voltage to the power enable or power good pins can damage the Mercury+ XU1 SoC module.

- Do not actively drive the power enable or power good pins to anything other than ground.
- Do not pull these pins up to a voltage level higher than 3.3 V.

Pin Name	Module Connector Pin	Comment
PWR_EN	A10	Floating/3.3 V: Module power enabled Driven low: Module power disabled
PWR_GOOD	A12	0 V: Module supply not ok 3.3 V: Module supply ok

Table 16: Module Power Status and Control Pins

3.10.3 Voltage Supply Inputs

Table 17 describes the power supply inputs on the Mercury+ XU1 SoC module. The VCC voltages used as supplies for the I/O banks are described in Section 3.8.5.

Supply Name	Module Connector Pins	Voltage	Description
VCC_MOD	A1, A2, A3, A4, A5, A6, A7, A8, A9, A11	5 – 15 V	Supply for on-module generated power supplies. The 2.5 V supply is generated from the 3.3 V supply. The input current is rated at 3 A (0.3 A per connector pin).
VCC_BAT	A168	2.0 – 5.5 V	Supply for the battery voltage for MPSoC battery-backed RAM and battery-backed RTC.

Table 17: Voltage Supply Inputs

3.10.4 Voltage Supply Outputs

Table 18 presents the supply voltages generated on the Mercury+ XU1 SoC module, that are available on the module connector.

Supply Name	Module Connector Pins	Voltage	Typical Available Current[23]	Comment
VCC_3V3	A26, A29, A50, A86 B55, B79, B115, B127, B152, B155 C96, C103, C136, C143	3.3 V ±5%	4 A (max. 0.3 A per pin)	Always active
VCC_2V5	A53, A62, A65, A89	2.5 V ±5%	0.25 A	Controlled by PWR_EN[24]
VCC_1V8	B52, B76, B108, B128 C83, C123, C165	1.8 V ±5%	1 A	Controlled by PWR_EN

Table 18: Voltage Supply Outputs

NOTICE

Damage to the device due to unsuitable usage of the output pins

- Do not connect any power supply to the voltage supply outputs.
- Do not short circuit any of the voltage supply outputs to ground.

3.10.5 Power Consumption

The power consumption of any MPSoC device strongly depends on the application (on the configured bitstream and I/O activity).

To estimate the power consumption of your design, use the power estimation tool provided by AMD for the corresponding device family, available on the AMD website.

3.10.6 Heat Dissipation

High performance devices like the AMD Zynq UltraScale+ MPSoC need cooling in most applications. Always make sure the MPSoC is adequately cooled.

For Mercury modules an Enclustra heat sink kit is available for purchase along with the product. It represents an optimal solution to cool the Mercury+ XU1 SoC module. The heat sink body is low profile and usually covers the whole module surface. The kit comes with a gap pad for the MPSoC device, a fan and required mounting material to attach the heat sink to the module PCB and base board PCB. With additional user configured gap pads, it is possible to cool other components on the board as well.

Alternatively, if the Enclustra heat sink does not match the application requirements, a third-party heat sink body (ATS) and an additional gap pad (t-Global) may be used. The Enclustra heat sink kit already

[23] The maximum available output current depends on your design. See Sections 3.10.1 and 3.10.5 for details.
[24] On revision 1 modules, the 2.5 V converter cannot be disabled via PWR_EN signal.

contains all necessary items for cooling the module (heat sink body, gap pad, fan, mounting material).

Table 19 lists the heat sink and thermal gap pad part numbers that are compatible with the Mercury+ XU1 SoC module. Details on the Mercury heat sink kit can be found in the Mercury Heat Sink Kits User Manual [22].

Product Name	Package Name	Enclustra Heat Sink	ATS Heat Sink	t-Global Thermal Gap Pad
Mercury+ XU1	FFVC900 [28]	ACC-HS4-Set	ATS-52310G-C1-R0	TG-A6200-30-30-1

Table 19: Heat Sink Characteristics

Tip

Adhesive heat sinks are only recommended for prototyping purposes. When the module is used in environments subject to vibrations, additional mechanical fixation is recommended.

NOTICE

Damage to the device due to overheating

Depending on the user application, the Mercury+ XU1 SoC module may consume more power than can be dissipated without additional cooling measures.

- Ensure that the MPSoC is always adequately cooled by installing a heat sink and/or providing air flow.

3.10.7 Voltage Monitoring

Several pins on the module connector on the Mercury+ XU1 SoC module are marked as VMON. These are voltage monitoring outputs that are used in the production test for measuring some of the on-board voltages.

It is not allowed to draw power from the voltage monitoring outputs.

Tip

The voltage monitoring outputs are for Enclustra-use only. Pinout changes may be applied between revisions.

Table 20 presents the VMON pins on the Mercury+ XU1 SoC module.

Pin Name	Mod. Conn. Pin	Connection	Description
VMON_INT	A102	VCC_INT	PL core voltage
VMON_1V2_VBAT	B8	VCC_1V2	1.2 V on-board voltage (default assembly) MPSoC battery voltage (custom assembly)
VMON_PSINT	C8	VCC_PSINT	PS core voltage
VMON_0V9	B167	VCC_0V9	0.9 V on-board voltage
VMON_1V8	B168	VCC_1V8	1.8 V on-board voltage

Table 20: Voltage Monitoring Outputs

3.11 Clock Generation

A 33.33 MHz oscillator is used for the Mercury+ XU1 SoC module clock generation. The 33.33 MHz clock is fed to the PS.

A 100 MHz LVDS oscillator and a 27 MHz CMOS oscillator provide reference clock inputs to the PS GTR bank 505. A 24 MHz clock and a 25 MHz clock are used for the USB PHYs and Ethernet PHYs respectively. The crystal pads for the MPSoC RTC are connected to a 32.768 kHz oscillator on the Mercury+ XU1 SoC module.

Table 21 describes the clock connections to the MPSoC device.

Signal Name	Frequency	MPSoC Pin	MPSoC Pin Name
CLK33	33.33 MHz	P20	PS_REF_CLK
CLK27_GTR_P CLK27_GTR_N	27 MHz	H25 H26	PS_MGTREFCLK3P_505 PS_MGTREFCLK3N_505
CLK100_GTR_P CLK100_GTR_N	100 MHz	K25 K26	PS_MGTREFCLK2P_505 PS_MGTREFCLK2N_505
PS_PADI PS_PADO	32.768 kHz	R22 R23	PS_PADI (crystal pad input for MPSoC built-in RTC) PS_PADO (crystal pad output for MPSoC built-in RTC)

Table 21: Module Clock Resources

3.12 Reset

The power-on reset signal (POR) and the PS system reset signal (SRST) of the MPSoC device are available on the module connector.

Pulling PS_POR# low resets the MPSoC device, the Ethernet and the USB PHYs, and the QSPI and eMMC flash devices. Refer to the Mercury Mars Module Pin Connection Guidelines [11] for general rules regarding the connection of reset pins.

Pulling PS_SRST# low resets the MPSoC device and enables the connection between QSPI flash and module connector, allowing the flash to be programmed from an external SPI master.

For details on the functions of the PS_POR_B and PS_SRST_B signals, refer to the Zynq UltraScale+ Device Technical Reference Manual [27].

Table 22 presents the available reset signals. Both signals, PS_POR# and PS_SRST#, have on-board 10 kΩ pull-up resistors to VCC_CFG_MIO. For on-board devices using 1.8 V signaling, a PS_POR# low voltage variant is generated (PS_POR#_LV). PS_POR# is automatically asserted if PWR_GOOD is low.

Signal Name	Connector Pin	MPSoC Pin	MPSoC Pin Name	Description
PS_POR#	A132	U23	PS_POR_B	Power-on reset
PS_SRST#	A124	P19	PS_SRST_B	System reset

Table 22: Reset Resources

3.13 LEDs

There are three active-low user LEDs on the Mercury+ XU1 SoC module. Two of them are connected to the PS and one is connected to the PL. The PS LED signals are shared with the debug connector trace signals on modules revisions 1 and 2.

On revision 1 modules, LED1# is connected to both PS and PL, while LED2# is mapped to a different FPGA pin. Also, an additional LED signal, LED3#, is available on revision 1 modules on package pin Y7. For details, refer to the Mercury+ XU1 SoC Module Known Issues and Changes [7] and to the Mercury+ XU1 SoC Module User Schematic [6].

Signal Name (PS)	MPSoC Pin (PS)	MPSoC Pin Name (PS)	Signal Name (PL)	MPSoC Pin (PL)	Comment
PS_LED0#[25]	J16	MIO[24]	–	–	User function / active-low
PS_LED1#[25]	G16	MIO[25]	-[26]	-[26]	User function / active-low
–	–	–	LED2#[27, 28]	AE8[29]	User function / active-low

Table 23: User LEDs

The module is also equipped with two status LEDs, which offer details on the configuration process for debugging purposes.

Signal Name (PS)	MPSoC Pin (PS)	Pin Name (PS)	Comment
PS_ERROR	P21	PS_ERROR_OUT	Refer to Zynq UltraScale+ Device Technical Reference Manual [27]
PS_STATUS	P22	PS_ERROR_STATUS	Refer to Zynq UltraScale+ Device Technical Reference Manual [27]

Table 24: Status LEDs

On revision 1 modules, the PS_STATUS LED is active-low. Starting with revision 2, the polarity for the PS_STATUS LED has been inverted, as the PS_ERROR_STATUS signal is active-high in the MPSoC device.

3.14 DDR4 SDRAM

There is a single DDR4 SDRAM channel on the Mercury+ XU1 SoC module attached directly to the PS side and is available only as a shared resource to the PL side.

The DDR4 SDRAM is connected to PS I/O bank 504. The memory configuration on the Mercury+ XU1 SoC module supports ECC error detection and correction. The correction code type used is single bit error correction and double bit error detection (SEC-DED).

Five 16-bit memory chips are used to build an 72-bit wide memory (8 bits are unused): 64 bits for data and 8 bits for ECC.

The maximum memory bandwidth on the Mercury+ XU1 SoC module is:
2'400 Mbit/s × 64 bit = 19'200 MB/s

3.14.1 DDR4 SDRAM Characteristics

Table 25 describes the memory availability and configuration on the Mercury+ XU1 SoC module.

Module	Density	Configuration
ME-XU1-D11E	4 Gbit	256 M × 16 bit
ME-XU1-D12E	8 Gbit	512 M × 16 bit

Table 25: DDR4 SDRAM Characteristics

In custom configurations, up to 8 GB of SDRAM memory may be assembled on the module.

[25] Shared with debug UART interface on modules revision 1 and 2 (signals PS_LED0#_UA1TX and PS_LED1#_UA1RX)
[26] Shared with LED1# signal on revision 1 modules, mapped to package pin AE8.
[27] On revision 3 to 4.1 modules: May be used as LED signal or as clock for power converter synchronization. Refer to Section 3.10.1 for details.
[28] On revision 5, the signal name was changed from LED2#_PWR_SYNC to LED2#.
[29] Mapped to package pin V3 on revision 1 modules.

3.14.2 Signal Description

Refer to the Mercury+ XU1 SoC Module FPGA Pinout Excel Sheet [4] for detailed information on the DDR4 SDRAM connections.

3.14.3 Termination

> **Tip**
>
> No external termination is implemented for the data signals on the Mercury+ XU1 SoC module. Enclustra strongly recommends enabling the on-die termination (ODT) feature of the assembled device.

3.14.4 Parameters

Table 26 shows the parameters of the PS DDR4 SDRAM to be set in the Vivado project such that it corresponds to the reference design [2] of the Mercury+ XU1 SoC module.

Parameter	Value
Requested device frequency	1’200 MHz
Memory type	DDR4
Effective DRAM bus width	64 bit
ECC	Enabled
Speed bin	DDR4 2400T
CAS latency	17 cycles
RAS to CAS delay	17 cycles
Precharge time	17 cycles
CAS write latency	12 cycles
tRC	46.16 ns
tRASmin	32 ns
tFAW	30 ns
Additive latency	0 cycles
DRAM IC bus width	16 bits
DRAM device capacity (per die)	4’096 or 8’192 Mbit
Bank group address count	1 bit
Rank address count	0 bit
Bank address count	2 bit
Row address count	15-16 bit
Column address count	10 bit

Table 26: DDR4 SDRAM Parameters

3.15 QSPI Flash

The QSPI flash can be used to boot the PS, and to store the FPGA bitstream, ARM application code and other user data.

3.15.1 QSPI Flash Characteristics

Table 27 describes the memory availability and configuration on the Mercury+ XU1 SoC module.

As there is one QSPI flash chip assembled on the Mercury+ XU1 SoC module, type “single” must be selected when programming the flash from Vivado tools.

Part Number	Density	Manufacturer
S25FL512S	512 Mbit	Infineon (Spansion)

Table 27: QSPI Flash Characteristics

> **Tip**
>
> Different flash memory devices may be assembled in future revisions of the Mercury+ XU1 SoC module. Any flash memory with a different speed and temperature range fulfilling the requirements of the module variant may be used.

3.15.2 Signal Description

The QSPI flash is connected to the PS MIO pins 0 to 5. Some of these signals are available on the module connector, allowing the user to program the QSPI flash from an external source.

The reset of the QSPI flash is connected to the PS_POR#_LV power-on reset signal (note that modules revision 1 use PS_POR# signal).

Refer to Section 4 for details on programming the flash memory.

> **Tip**
>
> For optimal signal integrity, avoid long traces when when connecting the QSPI flash signals on the base board. Long traces or high capacitance may disturb the data communication between the MPSoC and the flash device.

3.15.3 Configuration

The QSPI flash supports up to 50 MHz operation for standard read. For fast, dual and quad read speed values, refer to the flash device datasheet. The "Feedback Clk" option on pin MIO[6] must be enabled in the Zynq configuration for clock rates higher than 40 MHz.

Refer to Zynq UltraScale+ Device Technical Reference Manual [27] for details on booting from the QSPI flash.

Using the Write Register (WWR) command can corrupt the QSPI flash. This issue is described in more details in the Mercury+ XU1 SoC Module Known Issues and Changes [7].

3.16 eMMC Flash

The eMMC flash can be used to boot the PS, and to store the FPGA bitstream, ARM application code and other user data.

3.16.1 eMMC Flash Characteristics

Table 28 describes the memory availability and configuration on the Mercury+ XU1 SoC module.

Module	Revision	Density
ME-XU1	R1	8 GB
ME-XU1	R2 and newer	16 GB

Table 28: eMMC Flash Characteristics

> **Tip**
>
> Different flash memory devices may be assembled in future revisions of the Mercury+ XU1 SoC module. Any flash memory with a different speed and temperature range fulfilling the requirements of the module variant may be used.

3.16.2 Signal Description

The eMMC flash signals are connected to the MIO pins 13 to 22 for 8-bit data transfer mode. Some of these signals are shared with the PJTAG interface (Refer to Section 4.1.3 for details). The command signal has a 4.7 kΩ pull-up resistor to 1.8 V and the data lines have 47 kΩ pull-up resistors to 1.8 V.

3.17 SD Card

An SD card can be connected to the PS MIO pins 45 to 51. The corresponding MIO pins are available on the module connector. Information on SD card boot mode is available in Section 4.6.5.

External pull-ups are needed for SD card operation. Depending on the selected voltage for VCC_CFG_MIO, a level shifter to 3.3 V may be required (some level shifters also have built-in pull-ups).

For booting from an Ultra High Speed (UHS) SD card, an SD 3.0 compliant level shifter is required on the base board and VCC_CFG_MIO must be set to 1.8 V. This boot mode has not been tested, but it may be supported in the future.

3.18 Dual Gigabit Ethernet

Two 10/100/1000 Mbit Ethernet PHYs are available on the Mercury+ XU1 SoC module, both connected to the PS via RGMII interfaces.

3.18.1 Ethernet PHY Characteristics

Table 29 describes the Ethernet PHY devices assembled on the Mercury+ XU1 SoC module.

Part Number	Manufacturer	Description
KSZ9031RNX	Microchip (Micrel)	10/100/1000 Mbit

Table 29: Gigabit Ethernet PHYs Characteristics

3.18.2 Signal Description

PHY 0 is connected to ETH 0 controller from the PS I/O bank 501. One of the Ethernet TX data signals is shared with the PCIe reset signal (PERST#). If the application requires a hard PCIe block, the ETH 0 interface is not available. Refer to Section 3.8.2 for details on the PERST# connection.

Tip

Remember that the Gigabit Ethernet 0 interface is not available when the PCIe endpoint in the PS is used, because of the PERST# connection.

PHY 1 is connected to ETH 3 controller from the PS bank 502. The corresponding MIO signals (64 to 75) are shared between Ethernet PHY 1 and USB PHY 1, therefore only one of them can be used. By default the Ethernet connection is enabled.

Tip

Remember that the USB 1 and Gigabit Ethernet 1 interfaces cannot be used simultaneously.

USB1_RST#_ETH1_RST is pulled to ground via a 1 kΩ resistor. To release the USB PHY from reset, this signal must be driven high from MIO[23]. ETH1_RST# is pulled to 1.8 V via a 10 kΩ resistor. If USB1_RST#_ETH1_RST signal is driven high from the PS, the Ethernet reset is connected to ground.

Both reset signals (for Ethernet and USB) are pulled to ground if the PS_POR# is active. Table 30 describes the behavior of the USB1/ETH1 selection circuit. The default selection is marked in bold.

Condition		Function	
PS_POR#	**USB1_RST#_ETH1_RST (MIO[23])**	**USB PHY 1**	**Ethernet PHY 1**
0	–	In reset	In reset
1	**0**	**In reset**	**Active**
1	1	Active	In reset

Table 30: USB1/ETH1 Selection

The two Gigabit Ethernet PHYs have a shared MDIO interface and a shared interrupt line. The interrupt output of the Ethernet PHYs is connected to the I2C interrupt line, available on MIO pin 12.

3.18.3 External Connectivity

The Ethernet signal lines can be connected directly to the magnetics. Refer to the Mercury Mars Module Pin Connection Guidelines [11] for details regarding the connection of Ethernet signals.

3.18.4 MDIO Address

The MDIO interface is shared between the two Gigabit Ethernet PHYs. These can be configured using the corresponding address. The MDIO address assigned to PHY 0 is 3 and to PHY 1 is 7.

The MDIO signals are mapped to MIO pins 76 to 77 and they are routed directly to PHY 1 and via a level shifter to PHY 0.

3.18.5 PHY Configuration

The configuration of the Ethernet PHYs is bootstrapped when the PHYs are released from reset. Make sure all I/Os on the RGMII interface are initialized and all pull-up or pull-down resistors are disabled at that moment.

The bootstrap options of the Ethernet PHYs are set as indicated in Table 31.

Strap Input	Signal Value	Description
MODE[3:0]	1110	RGMII mode: advertise all capabilities (10/100/1000, half/full duplex) except 1000Base-T half duplex.
PHYAD[2:0]	011 111	PHY0: MDIO address 3 PHY1: MDIO address 7
CLK125_EN	0	125 MHz clock output disabled
LED_MODE	1	Single LED mode

Table 31: Gigabit Ethernet PHYs Configuration - Bootstraps

For the Ethernet PHY configuration via the MDIO interface, the MDC clock frequency must not exceed 2 MHz.

The PHY is configured in single LED mode with active-low LEDs 1 and 2.

3.18.6 RGMII Delays Configuration

The two Ethernet PHYs are connected directly to hard MAC controllers present in the MPSoC device. In order to achieve the best sampling eye for the RX and TX data, it is recommended to adjust the pad skew delays as specified in Table 32. These values have been successfully tested on Enclustra side.

The delays can be adjusted by programming the RGMII pad skew registers of the Ethernet PHY. Refer to the PHY datasheet for details.

PHY Register Name	Register Value [binary]	Delay Value
RXD0-RXD3	0111	0 ps
RX_DV	0111	0 ps
RX_CLK	01111	0 ps
TXD0-TXD3	0111	0 ps
TX_EN	0111	0 ps
GTX_CLK	11110	900 ps

Table 32: Gigabit Ethernet PHY (PS) Configuration for KSZ9031 - RGMII Delays

For RX_CLK, the PHY itself uses an additional default delay of 1.2 ns.

3.19 USB 2.0

Two USB 2.0 PHYs are available on the Mercury+ XU1 SoC module, both connected to the PS to I/O bank 502. USB PHY 0 can be configured as host or device and USB PHY 1 can be used only as host.

3.19.1 USB PHY Characteristics

Table 33 describes the USB PHYs device type assembled on the Mercury+ XU1 SoC module.

Part Number	Manufacturer	Description
USB3320C	Microchip (Atmel)	USB 2.0 PHY

Table 33: USB 2.0 PHY Characteristics

3.19.2 Signal Description

The ULPI interface for the PHY 0 is connected to MIO pins 52 to 63 for use with the integrated USB controller.

The ULPI interface for the PHY 1 is connected to MIO pins 64 to 75. The MIO signals are shared between Ethernet PHY 1 and USB PHY 1, therefore only one of them can be used. By default the Ethernet connection is enabled. Refer to Section 3.18.2 for details on how to select Ethernet or USB mode.

> **Tip**
>
> Remember that the USB 1 and Gigabit Ethernet 1 interfaces cannot be used simultaneously.

3.20 USB 3.0

AMD Zynq UltraScale+ devices feature two built-in USB 3.0 controllers and PHYs, configurable as host or device. The PHY interface used by the USB 3.0 controller is PIPE3, supporting a 5 Gbit/s data rate in host or device modes. The interface of each USB 3.0 controller uses one of the PS GTR lanes.

A 100 MHz differential clock is available on the module and connected to PS_MGTREFCLK2 pins, to be used as a reference clock for the USB 3.0 interface. It is also possible to provide another reference clock from the base board to the MGTPS_REFCLK* pins.

Details on the built-in USB 2.0/3.0 controller and on the usage of the PS GTR lanes are available in the Zynq UltraScale+ Device Technical Reference Manual [27] and in the Zynq UltraScale+ MPSoC Data Sheet: Overview [32].

Figure 13 shows an example of a USB 3.0 implementation using the built-in AMD USB 3.0 interface and the USB 2.0 signals from the PHY, all routed to a USB 3.0 connector on the base board.

> **Tip**
>
> The USB 3.0 interface on the Mercury+ XU1 SoC module uses the GTR signal lines (MGTPS signals on module connector B), and not the USB_SSRX_P/N and USB_SSTX_P/N signal lines on module connector A.

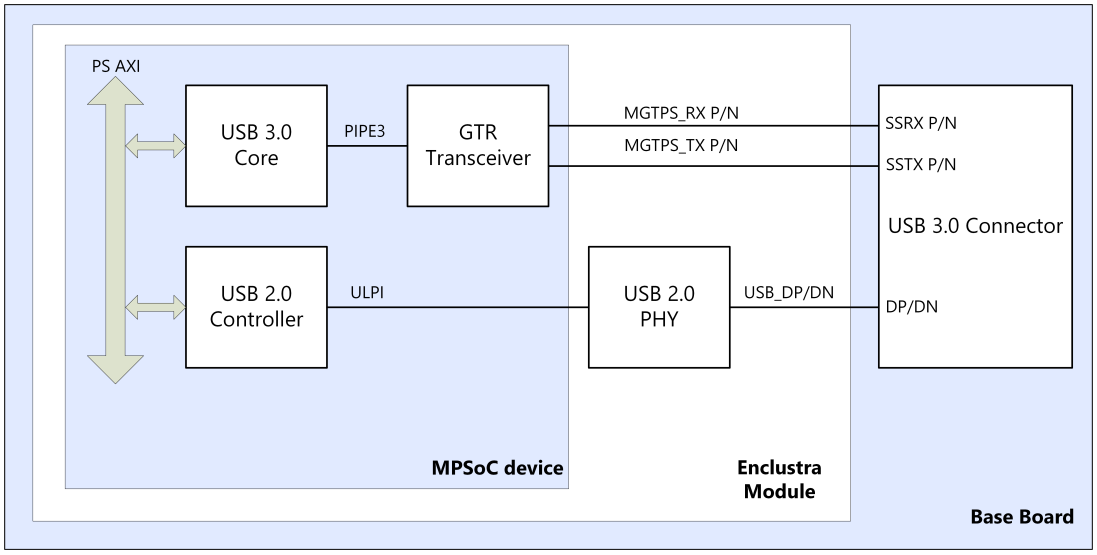

Figure 13: USB 3.0 Implementation Example

3.21 DisplayPort

AMD Zynq UltraScale+ devices feature two built-in DisplayPort controllers and PHYs, supporting up to two lanes at a 5.4 Gbit/s line rate. Each lane is represented by one of the PS GTR lines, available on the module connector.

A 27 MHz differential clock is available on the module and connected to PS_MGTREFCLK3 pins, to be used as a reference clock for the DisplayPort interface. It is also possible to provide another reference clock from the base board to the MGTPS_REFCLK* pins.

Details on the built-in DisplayPort controller and on the usage of the PS GTR lanes is available in the Zynq UltraScale+ Device Technical Reference Manual [27] and in the Zynq UltraScale+ MPSoC Data Sheet: Overview [32].

3.22 Real-Time Clock (RTC)

Zynq UltraScale+ devices include an internal real-time clock. The internal RTC can be accessed by the platform management unit (PMU). More information on the PMU is available in the Zynq UltraScale+ Device Technical Reference Manual [27].

The RTC crystal pad input and crystal pad output are connected on the Mercury+ XU1 SoC module to a 32.768 kHz oscillator.

Starting with revision 2 modules, an LDO[30] is used to generate the battery voltage for the built-in RTC (supplied to VCC_PSBATT pin), based on the VCC_BAT voltage mapped to the module connector. This pin can be connected directly to a 3 V battery on the base board.

On revision 1 modules, the battery voltage is generated using a voltage divider.

An external RTC (separate chip, not within the MPSoC) may be assembled optionally on the Mercury+ XU1 SoC module.

[30] For modules with revision 5.0 and higher, the LDO voltage is 1.5 V. For modules of revision 2 to 4, the LDO voltage is 1.2 V.

3.23 Secure EEPROM

The secure EEPROM is used to store the module type and serial number, as well as the Ethernet MAC address and other information. It is connected to the I2C bus.

The secure EEPROM must not be used to store user data.

Refer to Section 5.4 for details on the content of the EEPROM.

3.23.1 EEPROM Characteristics

Table 34 describes the EEPROM device assembled on the Mercury+ XU1 SoC module.

Part Number	Manufacturer	Assembly variant
ATSHA204A-MAHDA-T	Atmel	Default
DS28CN01	Maxim	Custom

Table 34: EEPROM Characteristics

An example demonstrating how to read data from the EEPROM is included in the Mercury+ XU1 SoC Module Reference Design [2].

3.24 Debug Connector

For revisions 1 and 2, the Mercury+ XU1 SoC module may optionally be equipped with a debug connector that allows the user to perform debug operations using JTAG or TRACE signals connected to the ARM DAP, to monitor and control FPGA configuration signals and to have access to the I2C bus and UART.

Starting with revision 3, the debug connector is not offered as an optional feature anymore. The related circuitry has been completely removed, including the MIO pin mappings for PJTAG, TRACE, and debug UART interfaces. PJTAG boot mode is also no longer supported. The signals that were mapped to the debug connector have been renamed to reflect the changes.

Part Number	Manufacturer
DF40C-30DP-0.4V(51)	Hirose

Table 35: Debug Connector Characteristics

NOTICE

Damage to the device

The Hirose debug connector on the Mercury+ XU1 SoC module is not polarized. Connecting an external board the wrong way around on the debug connector may damage the equipped MPSoC device, as well as other devices on the Mercury+ XU1 SoC module.

- Ensure that the debug connector is connected the right way around.

Table 36 describes the signals routed to the debug connector (valid only for modules revision 1 and 2).

Pin Number	Signal Name	Description
1	EMMC_IO2_PJTAG_TMS	PJTAG TMS
3	I2C_INT#_PJTAG_TCK	PJTAG TCK
7	EMMC_IO0_JTAG_TDI	PJTAG TDI
9	EMMC_IO1_PJTAG_TDO	PJTAG TDO
2	PJTAG_EN#	PJTAG enable (enable PJTAG boot mode)
5, 20, 31, 32, 33, 34	GND	Ground
10	VCC_3V3	
11	VCC_CFG_MIO	
21	VCC_ 1V8	
4	PS_SRST#	PS system reset
6	PS_PROG#	Configuration block reset (Refer to Zynq UltraScale+ Device Technical Reference Manual [27])
8	PS_INIT#	Initialization completed (Refer to Zynq UltraScale+ Device Technical Reference Manual [27])
12	PS_ERROR	PS_ERROR_OUT status signal (Refer to Zynq UltraScale+ Device Technical Reference Manual [27])
14	PS_STATUS	PS_ERROR_STATUS (Refer to Zynq UltraScale+ Device Technical Reference Manual [27])
13	I2C_SCL	I2C bus signals
15	I2C_SDA	
17	PS_LED1#_UA1RX	Debug UART signals, LED signals
19	PS_LED0#_UA1TX	
16	TRACE_EN#	Trace interface enable signal
18	TRACE_CLK	Debug trace interface (Refer to Zynq UltraScale+ Device Technical Reference Manual [27])
22	TRACE_CTL	
23	TRACE_DQ0	
24	TRACE_DQ4	
25	TRACE_DQ1	
26	TRACE_DQ5	
27	TRACE_DQ2	
28	TRACE_DQ6	
29	TRACE_DQ3	
30	TRACE_DQ7	

Table 36: Debug Connector Interface - Revision 1 and 2 Modules

The trace signals can be used to debug the processor running at full speed, allowing the user to collect information on the CPU instruction execution and data transfers.

In order to enable the trace interface, TRACE_EN# signal must be pulled low from the debug connector, and MIO pins 0 to 9 must be assigned to TRACE controller in the PS settings of the Vivado project. Additionally, starting with revision 2 modules, the trace clock multiplexer must be assembled. Refer to the Mercury+ XU1 SoC Module User Schematic [6] for details.

4 Device Configuration

4.1 JTAG

The Zynq UltraScale+ devices include two separate JTAG controllers: the Zynq UltraScale+ TAP and the ARM DAP. The first one uses the PS dedicated JTAG pins and has access to both PS and PL and the second one uses the PS PJTAG pins and is used for loading programs, system test, and PS debug.

Details on JTAG and on system test and debug are available in the Zynq UltraScale+ Device Technical Reference Manual [27].

On modules equipped with ES1 (engineering samples 1) MPSoC devices, PJTAG boot mode is required in order to program the FPGA and download a program to one of the ARM processors via JTAG.

Certain AMD tool versions support QSPI flash programming via JTAG only when JTAG boot mode is used (unavailable in the standard configurations of the Mercury+ XU1 SoC module). Alternatively, the QSPI flash can be programmed in u-boot or Linux by the SPI controller in the PS or from an SPI external master.

4.1.1 JTAG on Module Connector

The PL and the PS JTAG interfaces are connected into one single chain available on the module connector. The PS_JTAG pins are used by the Zynq UltraScale+ TAP controller. The controller has full functionality only after the PS boot is complete. In order to enable the ARM DAP controller, special commands must be sent to the Zynq UltraScale+ TAP.

The MPSoC device and the flash devices can be configured via JTAG from AMD Vivado Hardware Manager or AMD Vitis. For this operation, the ARM DAP must be enabled.

Signal Name	Module Connector Pin	PS Dedicated Pin	Comment
JTAG_TCK	A123	PS_JTAG_TCK	10 kΩ pull-up to VCC_CFG_MIO
JTAG_TMS	A119	PS_JTAG_TMS	10 kΩ pull-up to VCC_CFG_MIO
JTAG_TDI	A117	PS_JTAG_TDI	10 kΩ pull-up to VCC_CFG_MIO
JTAG_TDO	A121	PS_JTAG_TDO	10 kΩ pull-up to VCC_CFG_MIO

Table 37: JTAG Interface - PL and PS Access and Debug

4.1.2 External Connectivity

The JTAG signals can be connected to a JTAG connector on the base board. No pull-up/pull-down resistors are necessary. The VREF pin of the programmer must be connected to VCC_CFG_MIO.

It is recommended to add series termination resistors between the module and the JTAG header, close to the source. Enclustra also recommends adding a transient-voltage-suppression diode close to the JTAG connector to protect the MPSoC from damage due to ESD (Electrostatic Discharge). Refer to the Mercury Mars Module Pin Connection Guidelines [11] for details on JTAG interface.

4.1.3 PJTAG on Debug Connector

The JTAG pins available on the debug connector are used by the ARM DAP for debugging the PS. These pins can be used when the ARM DAP is not on the JTAG chain.

Signal Name	Pin on Debug Connector	PS Pin	Comment
I2C_INT#_PJTAG_TCK	3	MIO[12]	51.7 kΩ pull-up to VCC_3V3
EMMC_IO2_PJTAG_TMS	1	MIO[15]	47 kΩ pull-up to VCC_1V8
EMMC_IO0_PJTAG_TDI	7	MIO[13]	47 kΩ pull-up to VCC_1V8
EMMC_IO1_PJTAG_TDO	9	MIO[14]	47 kΩ pull-up to VCC_1V8

Table 38: JTAG Interface - ARM DAP Access via PJTAG Signals (valid only for modules revision 1 and 2)

In the standard configuration, PJTAG boot mode is not supported. In order to enable the PJTAG boot mode via MIO pins 12 to 15 (PJTAG1 pins), PJTAG_EN# must be driven low from pin 2 of the optional debug connector.

Note that starting with revision 3, the debug connector is not offered as an optional feature anymore. The related circuitry has been completely removed, including the MIO pin mappings for PJTAG, TRACE, and debug UART interfaces. PJTAG boot mode is also not supported any longer. The signals that were mapped to the debug connector have been renamed to reflect these changes.

4.2 Configuration Signals

The PS of the MPSoC needs to be configured before the PL can be used. AMD Zynq devices need special boot images to boot from QSPI flash, eMMC flash or SD card. For more information, refer to the Zynq UltraScale+ Device Technical Reference Manual [27].

Table 39 describes the most important configuration pins and their location on the module connector. These signals allow the MPSoC to boot from QSPI flash, eMMC flash or SD card, and can be used to program the QSPI flash from an external master. Refer to Section 4.7.3 for details.

Signal Name	MPSoC Pin Type	Mod. Conn. Pin	Description	Comment
PS_DONE	PS_DONE	A130	MPSoC device configuration done	1 kΩ pull-up to VCC_CFG_MIO
PS_POR}	PS_POR_B	A132	MPSoC power-on reset	10 kΩ pull-up to VCC_CFG_MIO
PS_SRST#	PS_SRST_B	A124	MPSoC system reset	10 kΩ pull-up to VCC_CFG_MIO
BOOT_MODE0	–	A126	Boot mode selection	10 kΩ pull-up to VCC_CFG_MIO
BOOT_MODE1	–	A112	Boot mode selection	10 kΩ pull-up to VCC_CFG_MIO

Table 39: MPSoC Configuration Pins

NOTICE

Damage to the device

- Only allow the signals PS_POR# and PS_SRST# to be driven low.
- Do not drive PS_POR# or PS_SRST# to a logic high level.
- Do not drive onto the PS_DONE pin on the base board.

4.3 Module Connector C Detection

Signal C_PRSNT# (pin C-167) must be connected to ground on the base board if the designed base board has three connectors. Depending on the value of this pin, the FPGA banks routed to module connector C are supplied with the voltages provided by the user (when C_PRSNT# is low) or with a default voltage of 1.8 V (when C_PRSNT# is unconnected).

C_PRSNT# is equipped with a 4.7 kΩ pull-up resistor on the module.

4.4 Pull-Up During Configuration

The Pull-Up During Configuration signal (PUDC) is pulled to ground on the module. As PUDC is an active-low signal, all FPGA I/Os will have the internal pull-up resistors enabled during device configuration.

If the application requires the pull-up during configuration to be disabled, this can be achieved by removing R201 component and by mounting R228. In this configuration the PUDC pin is connected to 1.8 V.

Figure 14 illustrates the configuration of the I/O signals during power-up. Figure 15 indicates the location of the pull-up/pull-down resistors on the module PCB. Lower right part on the bottom view drawing.

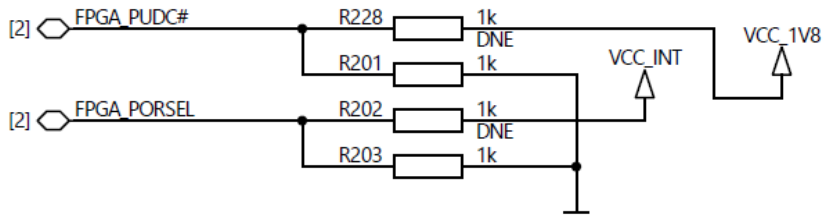

Figure 14: Pull-Up During Configuration (PUDC) and Power-on Reset Delay Override (PORSEL) - Revision 4 Modules

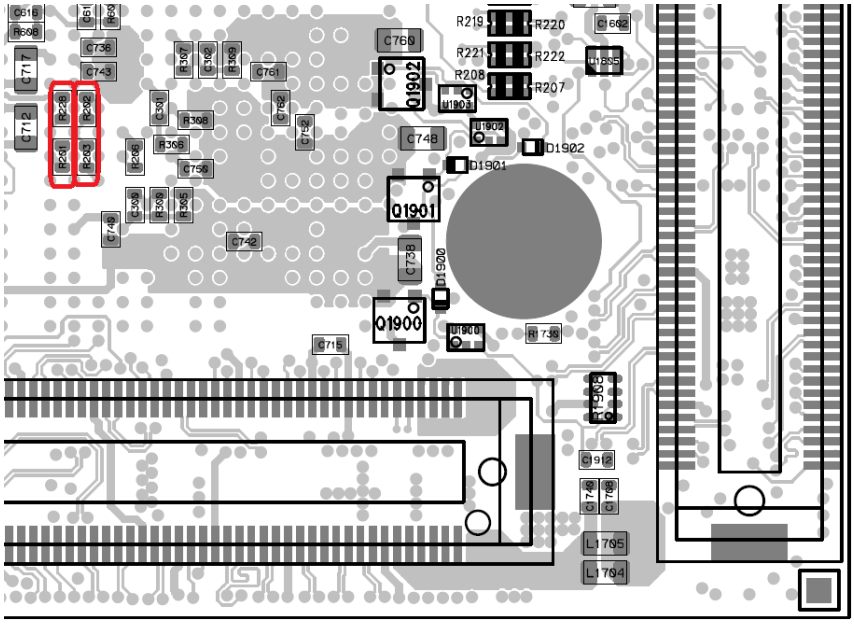

Figure 15: Pull-Up During Configuration (PUDC) and Power-on Reset Delay Override (PORSEL) Resistors - Assembly Drawing Bottom View (lower right part) for Revision 4 Modules

For details on the PUDC signal, refer to the Zynq UltraScale+ Device Technical Reference Manual [27].

4.5 Power-on Reset Delay Override

The power-on reset delay override MPSoC signal (POR_OVERRIDE) is pulled to ground on the module, setting the PL power-on delay time to the default standard time.

If the application requires faster PL power-on delay time, this can be achieved by removing R203 component and by mounting R202.

Figure 14 illustrates the configuration of the POR_OVERRIDE signal. Figure 15 indicates the location of the pull-up/pull-down resistors on the module PCB, lower right part on the bottom view drawing.

For details on the POR_OVERRIDE signal, refer to the Zynq UltraScale+ Device Technical Reference Manual [27].

4.6 Boot Mode

4.6.1 Boot Mode Selection

The boot mode can be selected via two signals available on the module connector and a signal available on the debug connector.

Table 40 describes the available boot modes on the Mercury+ XU1 SoC module. PJTAG_EN# signal is only available on the optional debug connector. It has a 10 kΩ pull-up resistor to VCC_CFG_MIO, therefore it may be left unconnected.

Note that starting with revision 3, the debug connector is not offered as an optional feature anymore. The related circuitry has been completely removed and the PJTAG boot mode is not supported any longer.

Starting with revision 4, JTAG boot mode has been introduced to increase the usability with AMD tools, which may report issues when programming the on-board QSPI flash or when loading the FPGA bitstream in a non-JTAG boot mode.

BOOT MODE1	BOOT MODE0	PJTAG_EN#	Mode Straps [3:0]	Description	Comment
0	0	1	0110	Boot from eMMC flash	–
0	1	1	1110	Boot from SD card (with an external SD 3.0 compliant level shifter; only available when VCC_CFG_MIO is 1.8 V)	Not supported (may be supported in the future)
1	0	1	0010	Boot from QSPI flash	–
1	1	1	0101	Boot from SD card (default mode)	–
1	1	0	1001	PJTAG boot mode[31]	Not supported in the standard configuration[31]
1	0	–	0000	JTAG boot mode	Available only starting with revision 4 modules in certain conditions (refer to Section 4.6.2 for details).

Table 40: Boot Modes

4.6.2 JTAG Boot Mode

Starting with revision 4, support for JTAG boot mode has been added to increase the usability of the module with AMD tools, for example for QSPI flash programming or FPGA bitstream loading.

> **Tip**
>
> JTAG boot mode is used explicitly for initial booting and is not required for the general JTAG mode used for programming, debugging, and in-system testing.

The following steps are required in order to boot the module in JTAG boot mode:

1. Set the boot mode selection signals for QSPI boot
2. Short-circuit R235 (see Figure 16) while powering-up the module (in order to sample the MPSoC boot selection pins correctly for JTAG boot mode)

[31] Starting with revision 3, PJTAG boot mode is not supported anymore on any configuration.

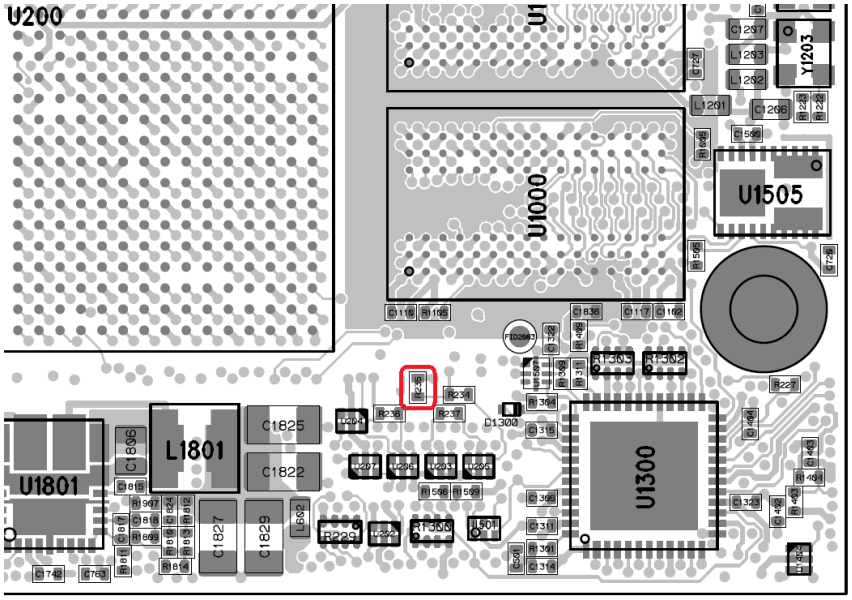

Figure 16: JTAG Boot Mode Resistor - Assembly Drawing Top View (lower right part) for Revision 4 Modules

4.6.3 eMMC Boot Mode

In the eMMC boot mode, the PS boots from the eMMC flash located on the module. The flash device is connected to the PS MIO pins 13 to 22 for 8-bit data transfer mode.

4.6.4 QSPI Boot Mode

In the QSPI boot mode, the PS boots from the QSPI flash located on the module. The flash device is connected to the PS MIO pins 0 to 5.

4.6.5 SD Card Boot Mode

In the SD card boot mode, the PS boots from the SD card located on the base board. There are two SD card boot modes available on the Mercury+ XU1 SoC module, as described in Table 40. The SD boot mode with level shifter is currently not supported.

The SD boot mode with level shifter is used with Ultra High Speed (UHS) SD cards. The controller will start the communication at 3.3 V and afterwards it will command the card to drop from 3.3 V operation to 1.8 V operation. For this mode, an external SD 3.0 compliant level shifter is required. This boot mode may be supported in the future by Enclustra modules and base boards.

For the SD card boot mode, the following requirements must be met:

- The SD card must be connected to MIO pins 45 to 51.
- A Zynq boot image must be generated from an MPSoC design having the SDIO controller enabled.
- The boot image must be named “boot.bin” and then copied to the SD card.
- The SDIO controller must be fed with a reasonable clock frequency. Refer to the reference design for guidelines on SDIO settings.

For details on SD card boot, refer to the Zynq UltraScale+ Device Technical Reference Manual [27].

4.7 Flash Programming

4.7.1 eMMC Flash Programming

The eMMC flash can be formatted and/or programmed in u-boot or Linux, like a regular SD card. The boot image or independent partition files can be transmitted via Ethernet or copied from another storage device.

Certain AMD tool versions support eMMC flash programming via JTAG.

4.7.2 QSPI Flash Programming via JTAG

The AMD Vivado and SDK software offer QSPI flash programming support via JTAG.

Certain AMD tools versions support QSPI flash programming via JTAG only when JTAG boot mode is used (unavailable in the standard configurations of the Mercury+ XU1 SoC module). For more information, refer to Zynq UltraScale+ Device Technical Reference Manual [27]. Alternatively, the QSPI flash can be programmed in u-boot or Linux by the SPI controller in the PS or from an SPI external master.

4.7.3 QSPI Flash Programming from an External SPI Master

The signals of the QSPI flash are directly connected to the module connector for flash access, as shown in Table 41. As the flash signals are connected to the MPSoC device as well, the MPSoC device pins must be tri-stated while accessing the QSPI flash directly from an external device. This is ensured by pulling the PS_SRST# signal to ground followed by a pulse on PS_POR#, which puts the MPSoC device into reset state and tri-states all I/O pins. PS_SRST# must be low when PS_POR# is released and kept low until the flash programming has finished. Afterwards, all SPI lines and PS_SRST# must be tri-stated and another reset impulse must be applied to PS_POR#.

Signal Name	MPSoC Pin	Mod. Conn. Pin	Description	Comment
FLASH_CLK	MIO[0]	A118	SPI CLK	10 kΩ pull-up to VCC_CFG_MIO
FLASH_DO	MIO[1]	A122	SPI MISO	–
FLASH_DI	MIO[4]	A114	SPI MOSI	10 kΩ pull-up to VCC_CFG_MIO
FLASH_CS#	MIO[5]	A116	SPI CS#	10 kΩ pull-up to VCC_CFG_MIO

Table 41: QSPI Flash Signals for External Access

Figure 17 shows the signal diagrams corresponding to flash programming from an external master.

In addition, a non-QSPI boot mode must be used during QSPI flash programming, otherwise the MPSoC device will attempt to boot from the flash and will disturb the clock.

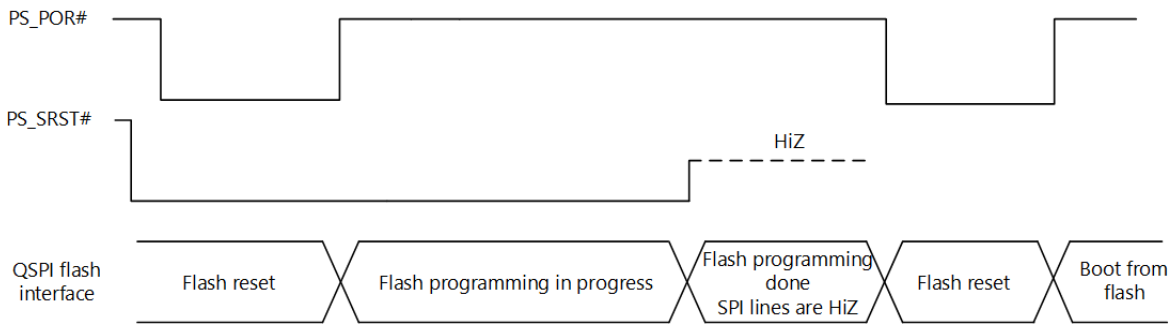

Figure 17: QSPI Flash Programming from an External SPI Master - Signal Diagrams

NOTICE

Damage to the device

The module can be damaged if the QSPI flash signals are driven simultaneously by the module and the base board.

- While accessing the QSPI flash from the module connector, put the MPSoC device into reset and select a non-QSPI boot mode.

4.8 Enclustra Module Configuration Tool

In combination with an Enclustra base board, the QSPI flash can be programmed using Enclustra Module Configuration Tool (MCT) [21]. For this method, a non-QSPI boot mode must be used during QSPI flash programming. The entire procedure is described in the reference design documentation, and is only available starting with revision 2 modules.

The AMD Zynq devices do not support slave serial configuration, therefore only flash programming is supported by the Enclustra MCT for the Mercury+ XU1 SoC module.

5 I2C Communication

5.1 Overview

The I2C bus on the Mercury+ XU1 SoC module is connected to the MPSoC device and to the EEPROM, and is available on the module and debug connectors. This allows external devices to read the module type and to connect more devices to the I2C bus.

The I2C clock frequency should not exceed 400 kHz.

> **Tip**
>
> Maximum I2C speed may be limited by the routing path and additional loads on the base board.

> **Tip**
>
> If the I2C traces on the base board are very long, 100 Ω series resistors should be added between the module and the I2C device on the base board.

5.2 Signal Description

Table 42 describes the signals of the I2C interface. The pins are connected to the PS. All signals have on-board pull-up resistors to VCC_3V3.

All signals must be connected to open collector outputs and must not be driven high from any source. I2C_INT# is an input to the MPSoC and must not be driven from the MPSoC device.

Starting with revision 2 modules, the I2C bus is connected to both PS and PL sides (and not only to the PS), to offer extra flexibility and help on future development. I2C on PL side is functional only when the VCC_IO_B66 voltage is 1.8 V.

Level shifters are used between the I2C bus and MPSoC pins, as I/O banks 500 and 66 are supplied with 1.8 V. Make sure that all pins are configured correctly and no pull-down resistors are enabled.

Signal Name	PS Pin	PL Package Pin	Connector Pin	Comment
I2C_SDA	MIO[11]	Y7	A113	2.2 kΩ pull-up to VCC_3V3
I2C_SCL	MIO[10]	V3	A111	2.2 kΩ pull-up to VCC_3V3
I2C_INT#	MIO[12]	–	A115	4.7 kΩ pull-up to VCC_3V3

Table 42: I2C Signal Description

5.3 I2C Address Map

Table 43 describes the addresses for several devices connected on I2C bus. For details on the EEPROM characteristics, refer to Section 3.23.

Address (7-bit)	Description	Assembly Variant
0x5C	Secure EEPROM	Custom
0x64	Secure EEPROM	Default

Table 43: I2C Addresses

5.4 Secure EEPROM

The secure EEPROM is used to store the module serial number and configuration. An example demonstrating how to read the module information from the EEPROM memory is included in the Mercury+ XU1 SoC module reference design.

> **Tip**
>
> Any attempt to write data to the secure EEPROM causes the warranty to be rendered void.

5.4.1 Memory Map

Address	Length (bits)	Description
0x00	32	Module serial number
0x04	32	Module product information
0x08	40	Module configuration
0x0D	24	Reserved
0x10	48	Ethernet MAC address
0x16	48	Reserved
0x1C	32	Checksum (only for DS28CN01 EEPROM type)

Table 44: EEPROM Sector 0 Memory Map

Module Serial Number

The module serial number is a unique 32-bit number that identifies the module. It is stored using big-endian byte order (MSB on the lowest address).

Module Product Information

This field indicates the type of module and hardware revision.

Module	Product Series	Reserved	Revision	Product Information
Mercury+ XU1 SoC module	0x032F	0x[XX]	0x[YY]	0x032F [XX][YY]

Table 45: Product Information

Module Configuration

Addr.	Bits	Description	Min. Value	Max. Value	Comment
0x08	[7:4]	MPSoC type	0	4	See Table 47
	[3:0]	MPSoC device speed grade	1	3	–
0x09	[7:6]	Temperature range	0	2	See Table 48
	[5]	Power grade	0 (Normal)	1 (Low power)	–
	[4:3]	Gigabit Ethernet port count	0	2	–
	[2]	RTC equipped	0	1	–
	[1]	Extended MGT routing[32]	0 (No)	1 (Yes)	–
	[0]	Reserved	–	–	–
0x0A	[7:2]	Reserved	–	–	–
	[1:0]	USB 2.0 port count	0	2	–
0x0B	[7:4]	DDR4 ECC RAM size (GB)	0 (0 GB)	4 (8 GB)	Resolution = 1 GB
	[3:0]	QSPI flash memory size (MB)	0 (0 MB)	7 (64 MB)	Resolution = 1 MB
0x0C	[7:4]	eMMC flash size (GB)	0 (0 GB)	5 (16 GB)	Resolution = 1 GB
	[3:0]	Reserved	–	–	–

Table 46: Module Configuration

.The memory sizes are defined as Resolution$\times 2^{(Value-1)}$, for example:

- DRAM = 0: none
- DRAM = 1: 1 GB
- DRAM = 2: 2 GB
- DRAM = 3: 4 GB

Table 47 shows the available MPSoC types.

[32] Property introduced starting with revision 3. For the "G1" module variants with 16 GTH transceivers on the module connector, a value of 1 (Yes) is programmed to the EEPROM. For the standard module variants, a value of 0 (No) is programmed to the EEPROM. The new EEPROM map definition is backward compatible.

Value	MPSoC Device Type
0	XCZU9EG ES
1	XCZU6EG
2	XCZU9EG
3	XCZU15EG
4	XCZU6CG

Table 47: MPSoC Device Types

Table 48 shows the available temperature ranges.

Value	Module Temperature Range
0	Commercial
1	Extended
2	Industrial

Table 48: Module Temperature Range

Ethernet MAC Address

The Ethernet MAC address is stored using big-endian byte order (MSB on the lowest address). Each module is assigned two sequential MAC addresses. Only the lower one is stored in the EEPROM.

6 Operating Conditions

6.1 Absolute Maximum Ratings

Table 49 indicates the absolute maximum ratings for Mercury+ XU1 SoC module. The values given are for reference only. For details, refer to the Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics [31].

Parameter	Description	Min.	Max.	Unit
VCC_MOD	Supply voltage relative to ground	-0.5	16.0	V
VCC_BAT	Supply voltage for MPSoC battery-backed RAM and battery-backed RTC	0.0	6.0	V
VCC_IO_B47 VCC_IO_B48	I/O bank supply voltage relative to ground (V_{CCO})	-0.5	3.4	V
VCC_CFG_MIO	I/O bank supply voltage relative to ground (V_{CCO_PSIO})	-0.5	3.63	V
VCC_IO_B64 VCC_IO_B65 VCC_IO_B66	I/O bank supply voltage relative to ground (V_{CCO})	-0.5	2.0	V
IO_B[x]_<...>	I/O input voltage relative to ground (V_{IN})	-0.5	V_{CCO} +0.5	V
PS_MIO[x]_<...>	I/O input voltage relative to ground (V_{PSIN})	-0.5	V_{CCO_PSIO} +0.55	V

Table 49: Absolute Maximum Ratings

6.2 Recommended Operating Conditions

Table 50 indicates the recommended operating conditions for Mercury+ XU1 SoC module. The values given are for reference only. For details, refer to the Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics [31].

Parameter	Description	Min.	Typ.	Max.	Unit
VCC_MOD	Supply voltage relative to ground	4.75	5.0 – 15.0	15.75	V
VCC_BAT	Supply voltage for MPSoC battery-backed RAM and battery-backed RTC	2.0	–	5.5	V
VCC_IO_B[x]	Output drivers supply voltage relative to ground (V_{CCO})	Refer to Section 3.8.5			
VCC_CFG_MIO	Output drivers supply voltage relative to ground (V_{CCO_PSIO})				
IO_B[x]_<...>	I/O input voltage relative to ground (V_{IN})	-0.2	–	V_{CCO}+0.2	V
PS_MIO[x]_<...>	I/O input voltage relative to ground (V_{PSIN})	-0.2	–	V_{CCO_PSIO}+0.2	V
Power	Maximum module power consumption[33]	–	–	45	W
Temperature[34]	Temperature range for extended temperature modules (E)	0	–	+85	°C
	Temperature range for industrial modules (I)	-40	–	+85	°C

Table 50: Recommended Operating Conditions

NOTICE

Damage to the device due to overheating

Depending on the user application, the Mercury+ XU1 SoC module may consume more power than can be dissipated without additional cooling measures.

- Ensure that the MPSoC is always adequately cooled by installing a heat sink and/or providing air flow.

[33] Sum of all power inputs at maximum rated current

[34] The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.

7 Ordering and Support

7.1 Ordering

Use the Enclustra online request/order form for ordering or requesting information:
http://www.enclustra.com/en/order/

7.2 Support

Follow the instructions on the Enclustra online support site:
http://www.enclustra.com/en/support/

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References

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