Mercury XU5 SoC Module

User Manual

Purpose

The purpose of this document is to present the characteristics of the Mercury XU5 SoC module to the user, and to provide the user with a comprehensive guide to understanding and using the Mercury XU5 SoC module.

Summary

This document first gives an overview of the Mercury XU5 SoC module followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Product Information	Code	Name
Product	ME-XU5	Mercury XU5 SoC Module

Document Information	Reference	Version	Date
Reference / Version / Date	D-0000-445-001	10	10-Jul-2026

Approval Information	Name	Position	Date
Written by	DIUN	Design Engineer	08-Jun-2018
Verified by	GKOE, GLAC	Design Expert	22-Jun-2018
Approved by	IJOS	Manager, BU-SP	10-Jul-2026

Document History

Version	Date	Author	Comment
10	10-Jul-2026	MGOS	Fixed value of power consumption in Operating Conditions section. Simplified the table about MGT and MIO signals per assembly option and grouped the figures per assembly option. Replaced the name “EEPROM” by “persistent storage element”, which is more representative of the device.
09	26-Mar-2025	MGOS	Improved terminology, content, and layout for better readability and consistency. Added R1.3 and R1.4 product models. Added section ”Getting Started”. Re-structured section ”Device Configuration”.
08	16-Feb-2021	DIUN	Added information on Mercury heat sinks, added Mercury+ ST1 to accesories section, added information on FPGA fuses and warranty, on differential I/Os, on voltage monitoring outputs, other style updates
07	25-Jul-2019	DIUN	Added information on new variants, on power supplies, corrected supported voltage range for VCC_BAT, corrected minimum MDIO clock frequency, other style updates
06	17-May-2019	DIUN	Added information on new variants, updated EEPROM map accordingly, added information on RGMII delays, added information on Linux how-to guide
05	18-Jan-2019	DIUN	Minor correction in the block diagrams
04	16-Jan-2019	DIUN	Added information on voltage monitoring and heat sink, updated information on assembly variants
03	12-Sep-2018	DIUN	Updated EEPROM map, other minor corrections
02	22-Aug-2018	DIUN	Updates, corrections and additions based on revision 1 modules
01	26-Jun-2018	DIUN	Version 01, preliminary

Table of Contents

1 Overview

1.1 General

1.1.1 Introduction

The Mercury XU5 SoC module combines the AMD Zynq® UltraScale+ MPSoC (Multiprocessor System-on-Chip) device with USB 3.0, PCIe® Gen3 $\times 4$, PCIe® Gen2 $\times 4$, two USB 2.0 PHYs, two Gigabit Ethernet PHYs, DDR4 SDRAM with Error Correction Code (ECC), eMMC flash, multi-gigabit transceivers, high-speed LVDS I/O, and is available in industrial temperature range, forming a complete and powerful embedded processing system.

The use of the Mercury XU5 SoC module, in contrast to building a custom MPSoC hardware, significantly reduces development effort and redesign risk and improves time-to-market for the embedded system.

Together with Mercury base boards, the Mercury XU5 SoC module allows the user to quickly build a system prototype and start with application development.

1.1.2 Warranty

Refer to the General Business Conditions, available on the Enclustra website [1].

> **Tip**
>
> The warranty of Enclustra modules is void if the FPGA's one-time programmable eFuses are blown. This operation is irreversible. Enclustra cannot test the module in case of a product return.

NOTICE

Data loss or unusable product

The fuses of the FPGA can be blown to activate the user-defined Advanced Encryption Standard (AES). After blowing the fuses, only content encrypted using a specific key can be loaded on the FPGA. Your key is unique and cannot be retrieved in case of loss.

- Keep your key in a secure location.

1.1.3 RoHS

The Mercury XU5 SoC module is designed and produced according to the Restriction of Hazardous Substances (RoHS) Directives 2011/65/EU (RoHS 2) and 2015/863/EU (RoHS 3).

1.1.4 Disposal and WEEE

The Mercury XU5 SoC module must be properly disposed of at the end of its life.

The Mercury XU5 SoC module is not subject to the Waste Electrical and Electronic Equipment (WEEE) Directive (2012/19/EU).

1.1.5 Safety Recommendations and Warnings

Mercury modules are not designed to be "ready for operation" for the end-user. These can only be used in combination with suitable base boards. Proper configuration of the hardware before usage is required.

NOTICE

Damage by inserting or removing the module while under power

- Ensure that the power supply is disconnected from the base board before inserting/removing the Mercury XU5 SoC module, connecting/disconnecting interfaces, or connecting/disconnecting jumpers.

NOTICE

Damage by touching while under power

Touching the capacitors of the DC-DC converters can lead to voltage peaks and permanent damage.

- Do not touch the capacitors of the DC-DC converters while the power is applied.

1.1.6 Electrostatic Discharge

Electronic boards are sensitive to electrostatic discharge (ESD).

NOTICE

Damage due to electrostatic discharge

Electrostatic discharge (ESD) may damage the Mercury XU5 SoC module partially or completely.

- Follow the relevant guidelines for ESD-safe handling when operating or assembling electronic components.
- Ensure that the product is handled with care and only in an ESD-protected environment.

1.1.7 Electromagnetic Compatibility

The Mercury XU5 SoC module is a Class A product (as defined in IEC 61000-3-2 standard) and is not intended for use in domestic environments. The product may cause electromagnetic interference, for which appropriate measures must be taken.

1.2 Features

- AMD Zynq® UltraScale+™ MPSoC
  - XCZU2CG/XCZU2EG/XCZU3EG/XCZU4CG/XCZU4EV/XCZU5EV device
  - SFVC784 package
  - Dual-/Quad-core ARM® Cortex™-A53 MPCore™ up to 1’500 GHz
  - Dual-core ARM® Cortex™-R5 MPCore™ up to 600 MHz
  - Mali-400 MP2 GPU (not for CG variants)
  - H.264 / H.265 Video Codec (only for EV variants)
  - AMD 16nm FinFET+ FPGA fabric
  - **ZU2CG/ZU2EG/ZU3EG**
    - 12 ARM peripheral I/Os (SPI, SDIO, CAN, I2C, UART)
    - 146 FPGA I/Os
      - 92 HP I/Os (up to 1.8 V)

- 54 HD I/Os (up to 3.3 V)
- 4 MGT transceivers
  - 4 GTR transceivers @ 6 Gbit/s
- 2 reference clock inputs
  - 2 GTR reference clock inputs
- **ZU4CG/ZU4EV/ZU5EV, with standard MGT routing**
  - 14 ARM peripheral I/Os (SPI, SDIO, CAN, I2C, UART)
  - 124 FPGA I/Os
    - 72 HP I/Os (up to 1.8 V)
    - 52 HD I/Os (up to 3.3 V)
  - 8 MGT transceivers
    - 4 GTH transceivers @ 12.5 Gbit/s
    - 4 GTR transceivers @ 6 Gbit/s
  - 4 reference clock inputs
    - 2 GTH reference clock inputs
    - 2 GTR reference clock inputs
  - PCIe Gen3 $\times$4 (AMD built-in PCIe integrated block using GTH lanes)
- **ZU4CG/ZU4EV/ZU5EV, with alternative MGT routing (G1 assembly variants)**
  - 12 ARM peripheral I/Os (SPI, SDIO, CAN, I2C, UART)
  - 146 FPGA I/Os
    - 92 HP I/Os (up to 1.8 V)
    - 54 HD I/Os (up to 3.3 V)
  - 4 MGT transceivers
    - 4 GTH transceivers @ 12.5 Gbit/s
  - 2 reference clock inputs
    - 2 GTH reference clock inputs
  - PCIe Gen3 $\times$4 (AMD built-in PCIe integrated block using GTH lanes)
- PCIe Gen2 $\times$4 (AMD built-in PCIe hard block using GTR lanes)

- Up to 8 GB DDR4 SDRAM with ECC on PS side
- Up to 2 GB DDR4 SDRAM on PL side
- 64 MB quad SPI flash
- 16 GB eMMC flash
- 2 $\times$ Gigabit Ethernet PHYs
- 2 $\times$ USB 2.0 PHYs (host and host/device)
- USB 3.0 (AMD built-in USB 3.0 hard block using GTR lanes)
- CAN, UART, SPI, I2C, SDIO/MMC
- Real-time clock
- Form factor: 56 $\times$ 54 mm
- 5 to 15 V supply voltage

1.3 Deliverables

- Mercury XU5 SoC module
- Mercury XU5 SoC module documentation, available via download:
  - Mercury XU5 SoC Module User Manual (this document)
  - Mercury XU5 SoC Module Reference Design [2]
  - Mercury XU5 SoC Module IO Net Length Excel Sheet [3]
  - Mercury XU5 SoC Module FPGA Pinout Excel Sheet [4]
  - Mercury XU5 SoC Module FPGA Pinout Assembly Variants Excel Sheet [5]
  - Mercury XU5 SoC Module User Schematic (PDF) [6]
  - Mercury XU5 SoC Module Known Issues and Changes [7]
  - Mercury XU5 SoC Module Footprint (Altium, Eagle, Orcad and PADS) [8]

    - Mercury XU5 SoC Module 3D Model (PDF) [9]
    - Mercury XU5 SoC Module 3D Model (STEP) [10]
    - Mercury Mars Module Pin Connection Guidelines [11]
    - Mercury Master Pinout [12]
    - Mercury Heat Sink Kits User Manual [22]
- Additional resources, available online:
    - Enclustra Build Environment [17] (Linux build environment; refer to Section 1.3.2 for details)
    - Enclustra Build Environment How-To Guide [18]
    - Petalinux BSP and Documentation [19]
    - Enclustra I2C Application Note [23]
    - Enclustra Gigabit Ethernet Application Note [24]
    - Enclustra ZynqMP Video Application Note [25]
    - Enclustra Secure Boot Reference Design for Zynq Ultrascale+ MPSoC [26]

1.3.1 Reference Design

The Mercury XU5 SoC Module Reference Design [2] features an example configuration for the Zynq UltraScale+ MPSoC device, together with an example top level HDL file for the user logic.

A bare metal "hello world" application is provided in the reference design. The example shows how to initialize the peripheral controllers and how to access the external devices. Pre-compiled binaries are included in the archive, so that the user can easily check that the hardware is functional.

> **Tip**
>
> To get notified about updates to the Mercury XU5 SoC Module Reference Design, turn on the notifications from the Enclustra GitHub page [2].

1.3.2 Enclustra Build Environment

> The Enclustra Build Environment is deprecated. The latest release of the reference design is compatible with AMD tools release 2022.1.

The Enclustra Build Environment (EBE) [17] enables the user to quickly set up and run Linux on any Enclustra SoC module or system board. It allows the user to choose the desired target, and download all the required binaries, such as bitstream and FSBL. It downloads and compiles all required software, such as U-Boot, Linux, and BusyBox based root file system.

The Enclustra Build Environment features a graphical user interface (GUI) and a command line interface (CLI) that facilitates the automatic build flow.

The Enclustra Build Environment How-To Guide [18] describes in more detail how to use the EBE to customize the provided software for the user application. The document provides information on the configuration options for U-Boot, Linux kernel and Buildroot, debugging possibilities for Linux applications, customization of device trees and integration of existing or new kernel drivers.

1.3.3 Petalinux BSP

> The Enclustra Petalinux BSP is deprecated. For reference design releases starting at 2024.2, the Enclustra Yocto BSP layer is provided instead (see Section 1.3.4).

The Enclustra Petalinux BSPs enable the user to quickly set up a Petalinux project and to run Linux on the Enclustra SoC module or system board.

The documentation [19] describes the build process in detail and allows a user without Petalinux knowledge to build and run the desired design on the target hardware.

1.3.4 Yocto BSP Layer

The Enclustra Yocto BSP layer enables the user to quickly set up a Yocto project and to run Linux on the Enclustra SoC module.

The documentation [20] describes the build process in detail and allows a user without Yocto knowledge to build and run a Linux reference design on the target hardware.

1.4 Accessories

1.4.1 Enclustra Heat Sink

For Mercury modules an Enclustra heat sink is available for purchase along with the product. Refer to Section 3.10.6 for further information on the available cooling options.

1.4.2 Mercury+ PE1 Base Board

The Mercury+ PE1 [14] is a versatile PCIe® x4 base board equipped with a multitude of I/O interfaces for use with the Mercury/Mercury+ family of FPGA and SoC modules, providing a head start for building custom FPGA- and SoC-based hardware systems.

It is compatible with a multitude of FMC boards from different suppliers to use in data acquisition systems, motor control, display and camera interfaces, software defined radio and more. The board is equally well suited for rapid prototyping and for building FPGA systems without designing custom hardware.

The available features depend on the Mercury module type and on the selected base board variant.

1.4.3 Mercury+ PE3 Base Board

The Mercury+ PE3 [16] is a versatile PCIe® x8 base board equipped with a multitude of I/O interfaces for use with the Mercury/Mercury+ family of FPGA and SoC modules, providing a head start for building custom FPGA- and SoC-based hardware systems.

This high performance base board provides a versatile set of I/O connectivity options, specialized for high-speed communication and video applications, including SFP+, QSFP+, HDMI, USB Type-C and Firefly. The board is equally well suited for rapid prototyping and for building FPGA systems without designing custom hardware.

The available features depend on the Mercury module type and on the selected base board variant.

1.4.4 Mercury+ ST1 Base Board

The Mercury+ ST1 board [15] is a compact, low-cost base board equipped with a multitude of I/O interfaces for use with the Mercury/Mercury+ family of FPGA and SoC modules.

It provides a versatile set of I/O connectivity options, specialized for video applications, including DisplayPort, HDMI, MIPI, and SFP+. The board is equally well suited for rapid prototyping and for building FPGA systems without designing custom hardware.

The available features depend on the Mercury module type and on the selected base board variant.

1.5 AMD Tool Support

The MPSoC devices assembled on the Mercury XU5 SoC module are supported by the Vivado ML Standard Edition software, which is available free of charge. Contact AMD for further information.

2 Getting Started

This section contains essential information on using the Mercury XU5 SoC module.

NOTICE

Damage to the connectors

The connectors of the module and the base board can be damaged if the connectors are not properly aligned during installation.

- Align the connectors carefully before applying force on the module.
- Do not use excessive force to latch the module into the connectors on the base board.

NOTICE

Damage to the device when applying power

The Mercury module could physically be mounted the wrong way around on the base board. The module and the base board can be damaged if the device is powered on while it is connected the wrong way around.

- Ensure that the mounting holes on the base board are aligned with the mounting holes of the module.

NOTICE

Damage to the module by overtightening screws

- Do not use excessive force when tightening the screws.

NOTICE

Damage to the device by using metallic objects for removal

- Do not use metallic object, such as screwdrivers, to remove the module from the base board.
- Remove the module carefully using your fingers to avoid damage.
- If more force is required, always apply it evenly by hand to avoid damage.

2.1 Installing the Module

Tip

A small copper square on the bottom left corner of Enclustra modules is provided as landmark. The same landmark is provided on the Enclustra base boards to help orient the module in the right direction when connecting it.

1. **NOTICE: Damage due to electrostatic discharge (ESD).**
   Ensure that the product is handled in an ESD-protected environment.
2. **NOTICE: Damage by connecting or disconnecting under power.**
   Ensure that the power of the base board is disconnected.
3. **NOTICE: Damage to the device when applying power. The module could physically be mounted the wrong way around on the base board.**
   Identify the correct orientation and position of the module with respect to the base board.
4. **NOTICE: Damage to the connectors. Align the connectors carefully before applying force on the module. Do no use excessive force to latch the module into the connectors on the base board.**
   Align the connectors and press the module onto the base board.
5. **NOTICE: Damage to the module. Do not use excessive force when tightening the screws.**
   If required, use up to four M3 screws to mechanically fasten the module to the base board.

2.2 Removing the Module

1. **NOTICE: Damage due to electrostatic discharge (ESD).**
   Ensure that the product is handled in an ESD-protected environment.
2. **NOTICE: Damage by connecting or disconnecting under power.**
   Ensure that the power of the base board is disconnected.
3. **NOTICE: Damage to the device. Do not use any metallic object to remove the module from the base board.**
   Remove the module carefully using your fingers.

3 Module Description

3.1 Block Diagram

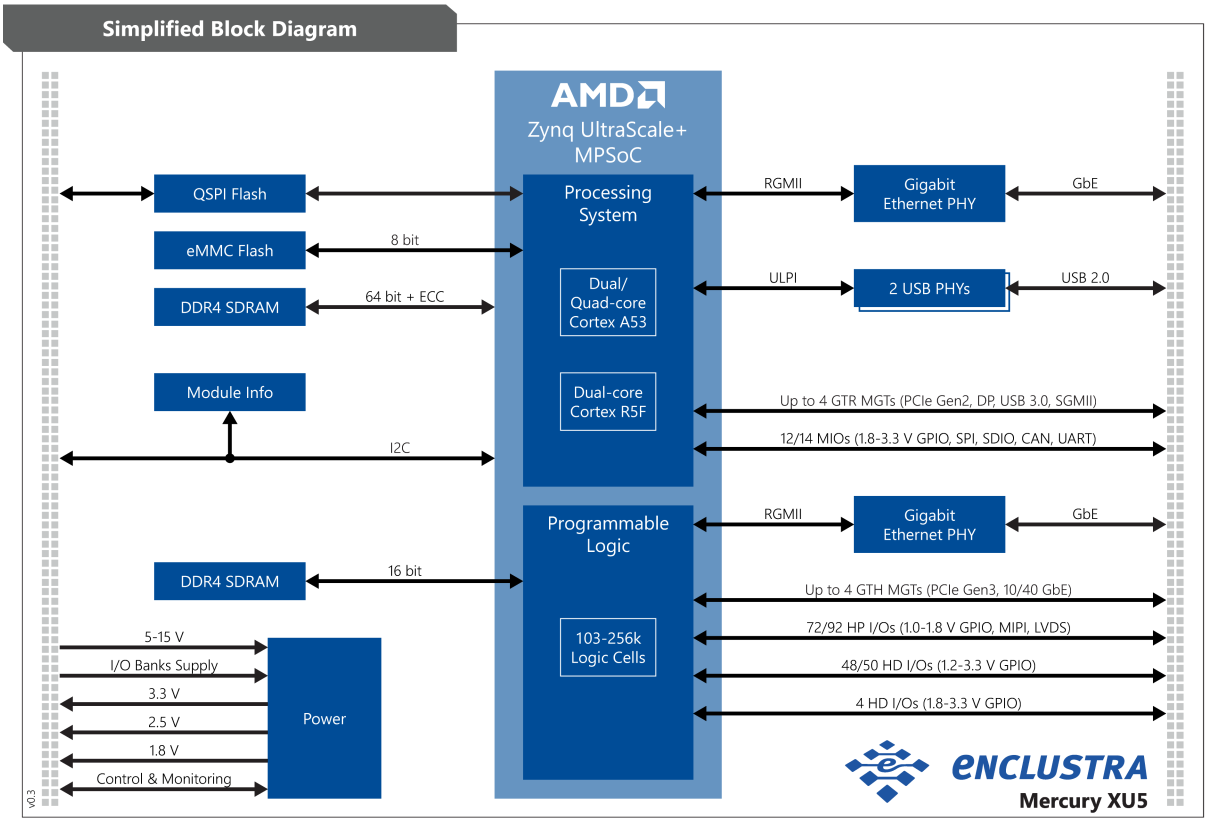

Figure 1: Hardware Block Diagram

The main component of the Mercury XU5 SoC module is the AMD Zynq UltraScale+ MPSoC device. Most of its I/O pins are connected to the Mercury module connector, making up to 158 regular user I/Os available to the user. Further, up to 8 MGT lanes are available on the module connector, making possible the implementation of several high-speed protocols such as PCIe Gen3/Gen2 $\times 4$ and USB 3.0 (simultaneous usage of all the interfaces is limited to the available hardware resources i.e. number of transceivers and lane mapping).

The "G1" module variants offer 158 regular I/Os and 4 GTH MGT lanes on the module connector at the trade-off of no GTR transceivers available. Section 3.8.2 describes in more detail the module assembly variants and routing options around the Processing System (PS) and Programmable Logic (PL) transceivers and I/Os.

The MPSoC device can boot from the on-board QSPI flash, from the eMMC flash or from an external SD card. For development purposes, a JTAG interface is connected to Mercury module connector.

The available standard configurations include a 16 GB eMMC flash, a 64 MB quad SPI flash, up to 8 GB DDR4 SDRAM with ECC connected to the Processing System (PS) and up to 2 GB DDR4 SDRAM connected to the Programmable Logic (PL). The DDR configuration on the smallest module variant (ME-XU5-2CG-1E-D10H) does not support ECC and has only half of the DDR4 bandwidth (32-bit interface instead of 64-bit).

The module is equipped with two Gigabit Ethernet PHYs and two USB 2.0 PHYs, making it ideal for communication applications.

A real-time clock is available on the AMD Zynq UltraScale+ MPSoC device.

On-board clock generation is based on a 33.33 MHz crystal oscillator and a 100 MHz LVDS oscillator for the PL. In addition, two oscillators delivering 100 MHz and 27 MHz reference clocks for the MGT GTR lanes, are assembled on the module.

The module's internal supply voltages are generated from a single input supply of 5 to 15 V DC. Some of these voltages are available on the Mercury module connectors to supply circuits on the base board.

Six LEDs are connected to the MPSoC pins for status signaling.

3.2 Module Configuration and Product Models

Table 1 describes the available standard module configurations. The product model indicates the module type and main features. Figure 2 describes the fields within the product model. Custom configurations are available. Contact Enclustra for more information.

Product Model	MPSoC[1]	DDR4 (PS) SDRAM	DDR4 (PS) ECC	DDR4 (PL) SDRAM	Temperature Range
ME-XU5-2CG-1E-D10H[2]	XC**ZU2**CG-1SFVC784E	1 GB	–	512 MB	0 to +85°C
ME-XU5-2EG-1I-D11E	XC**ZU2**EG-1SFVC784I	2 GB	•	512 MB	-40 to +85°C
ME-XU5-3EG-2I-D11E	XC**ZU3**EG-2SFVC784I	2 GB	•	512 MB	-40 to +85°C
ME-XU5-4EV-1I-D11E	XC**ZU4**EV-1SFVC784I	2 GB	•	512 MB	-40 to +85°C
ME-XU5-4EV-1I-D11E-G1[3]	XC**ZU4**EV-1SFVC784I	2 GB	•	512 MB	-40 to +85°C
ME-XU5-5EV-2I-D12E	XC**ZU5**EV-2SFVC784I	4 GB	•	1 GB	-40 to +85°C
ME-XU5-5EV-2I-D12E-G1[3]	XC**ZU5**EV-2SFVC784I	4 GB	•	1 GB	-40 to +85°C

Table 1: Standard Module Configurations

[1] The "device" is shown in bold.

[2] This variant supports only half of the DDR4 bandwidth on the PS side (32-bit interface instead of 64-bit). Refer to Section 3.14 for details.

[3] G1 assembly variants offered for migration purposes or for cases where the end application does not require GTR transceivers, but instead more regular I/Os. It can be used when porting an existing design from Mercury ZX1 or ZX5 to Mercury XU5 SoC module. Refer to Section 3.8.2 for details on assembly options and migration guidelines. This variant was referred to as "X1" variant in previous user manual versions.

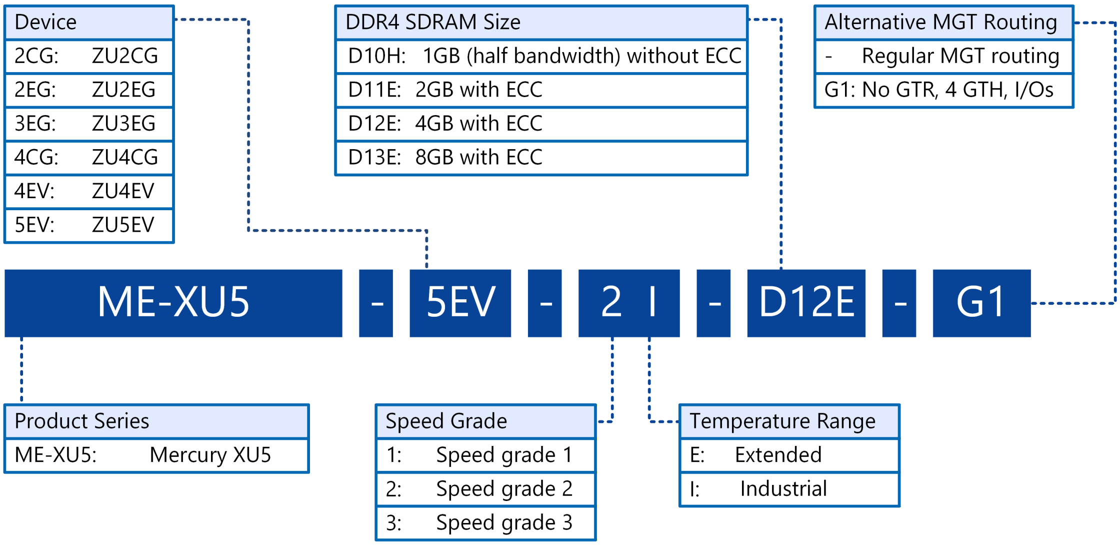

Figure 2: Product Model Fields

For the first revision modules or early access modules, the product model may not respect entirely this naming convention. Contact Enclustra for more information.

3.3 EN-Numbers and Product Models

Every product is uniquely labeled, showing the EN-number and serial number. An example is presented in Figure 3.

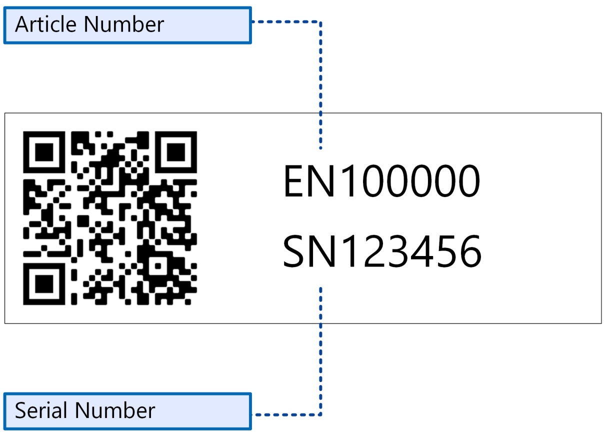

Figure 3: Product Label

The correspondence between EN-number and product model for each revision is shown in Table 2.

The known issues of the product and the changes between the revisions are described in the Mercury XU5 SoC Module Known Issues and Changes [7].

EN-Number	Product Models	Product Revision
EN107148	ME-XU5-5EV-2I-D12E-G1	R1.4

Continued on next page...

EN-Number	Product Models	Product Revision
EN107144	ME-XU5-4EV-1I-D11E	R1.4
EN107143	ME-XU5-4EV-1I-D11E-G1	R1.4
EN107139	ME-XU5-3EG-2I-D11E	R1.4
EN107135	ME-XU5-2EG-1I-D11E	R1.4
EN107116	ME-XU5-2CG-1E-D10H	R1.4
EN107027	ME-XU5-5EV-2I-D12E	R1.4
EN106119	ME-XU5-2CG-1E-D10H	R1.3
EN106118	ME-XU5-4EV-1I-D11E-G1	R1.3
EN106117	ME-XU5-5EV-2I-D12E-G1	R1.3
EN106116	ME-XU5-4EV-1I-D11E	R1.3
EN106114	ME-XU5-3EG-2I-D11E	R1.3
EN106113	ME-XU5-2EG-1I-D11E	R1.3
EN106094	ME-XU5-5EV-2I-D12E	R1.3
EN102599	ME-XU5-5EV-1E-D11E	R1.2
EN102598	ME-XU5-4CG-1E-D11E-G1	R1.2
EN102596	ME-XU5-2CG-1E-D10H	R1.2
EN102285	ME-XU5-4EV-1I-D11E-G1	R1.2
EN102229	ME-XU5-5EV-2I-D12E-G1	R1.2
EN102228	ME-XU5-5EV-3E-D13E	R1.2
EN102227	ME-XU5-5EV-2I-D12E	R1.2
EN102226	ME-XU5-4EV-1I-D11E	R1.2
EN102225	ME-XU5-3EG-2I-D11E	R1.2
EN102224	ME-XU5-2EG-1I-D11E	R1.2
EN102060	ME-XU5-5EV-2I-D12E-G1	R1.0
EN102028	ME-XU5-5EV-3E-D13E	R1.0
EN102027	ME-XU5-5EV-2I-D12E	R1.0
EN102026	ME-XU5-4EV-1I-D11E	R1.0

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EN-Number	Product Models	Product Revision
EN102025	ME-XU5-3EG-2I-D11E	R1.0
EN101970	ME-XU5-2EG-1I-D11E	R1.0

Table 2: EN-Numbers and Product Models

3.4 Top and Bottom Views

Depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

3.4.1 Top View

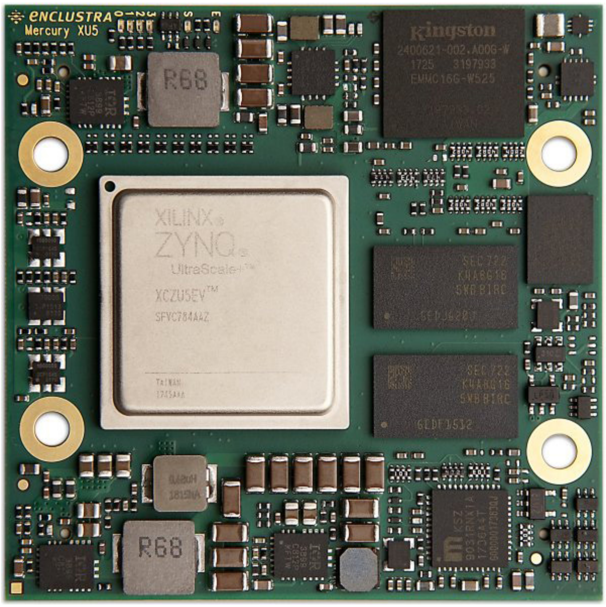

Figure 4: Module Top View

3.4.2 Bottom View

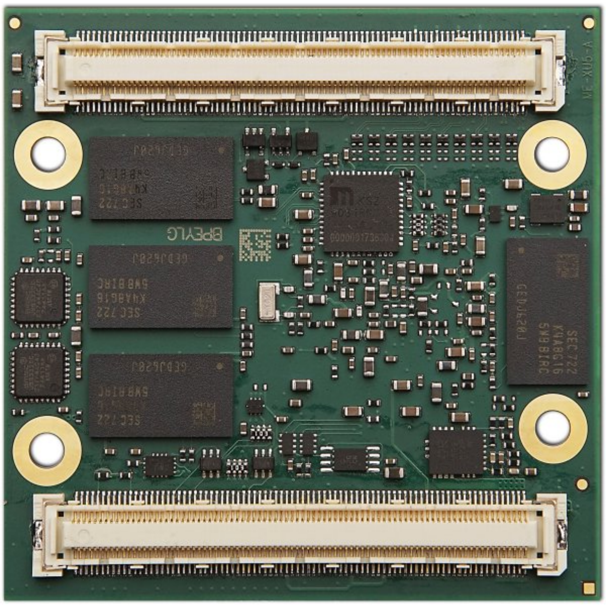

Figure 5: Module Bottom View

3.5 Top and Bottom Assembly Drawings

Depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

3.5.1 Top Assembly Drawing

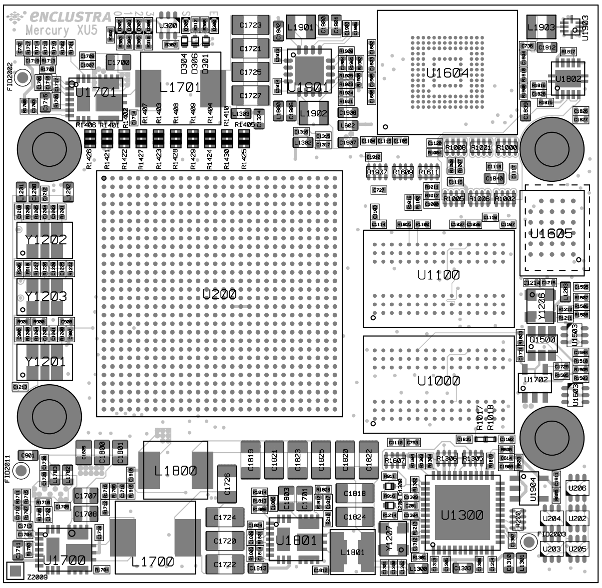

Figure 6: Module Top Assembly Drawing

3.5.2 Bottom Assembly Drawing

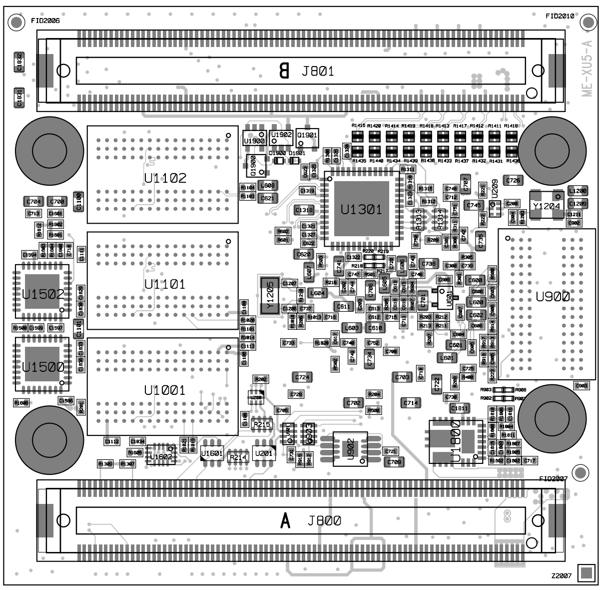

Figure 7: Module Bottom Assembly Drawing

3.6 Module Footprint and Mechanical Data

Figure 8 shows the dimensions of the module footprint on the base board.

Enclustra offers Mercury and Mercury+ modules of various geometries having widths of 56, 64, 65, 72 or 74 mm and having different topologies for the mounting holes. If different module types shall be fixed on the base board by screws, additional mounting holes may be required to accommodate different modules. The footprints of the module connectors for the base board design are available for different PCB design tools (Altium, PADS, Eagle, Orcad) [8] and include the required information on the module sizes and holes.

The maximum component height under the module is dependent on the connector type. Refer to Section 3.7 for detailed connector information.

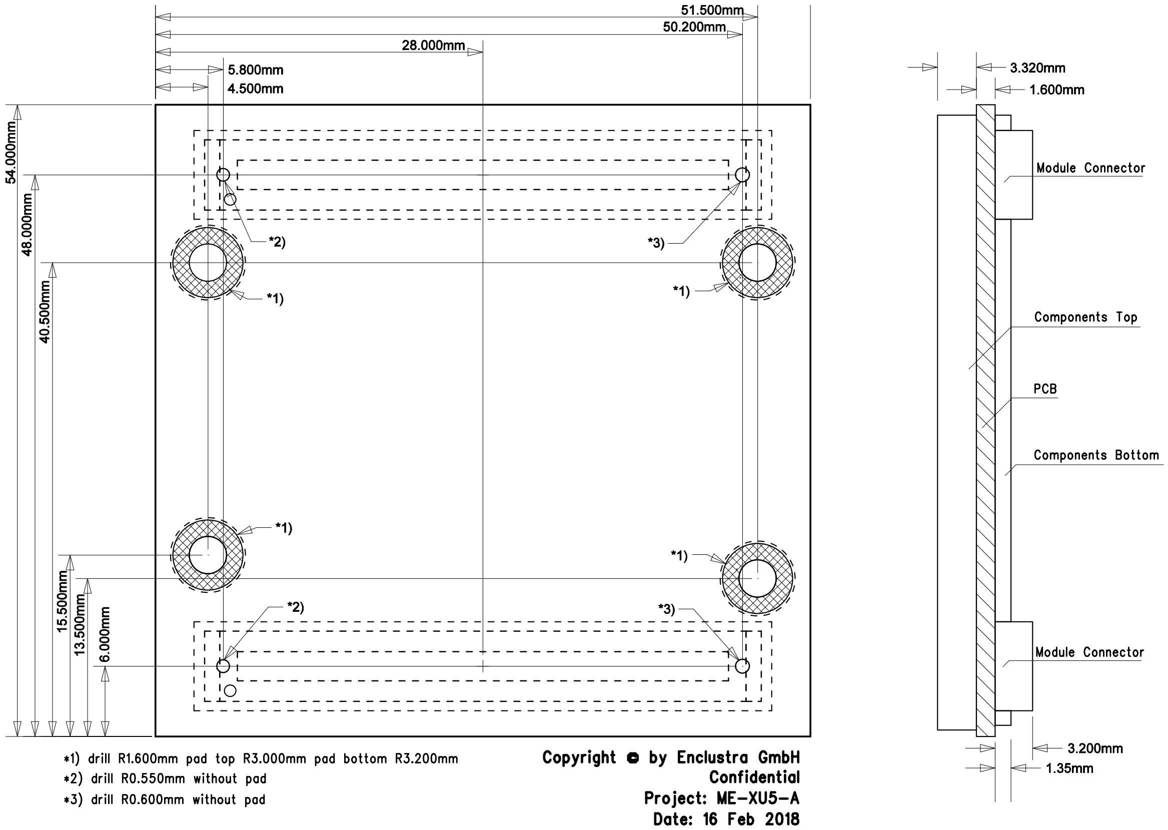

Figure 8: Model Footprint and Dimensions, Top View and Side View

Table 3 describes the mechanical characteristics of the Mercury XU5 SoC module. A 3D model (PDF) and a STEP 3D model are available [9], [10].

Parameter	Value
Size	56 × 54 mm
Component height top	3.32 mm
Component height bottom	1.9 mm[4]
Weight	26 g

Table 3: Mechanical Data

3.7 Module Connector

Two Hirose FX10 168-pin 0.5 mm pitch headers with a total of 336 pins have to be integrated on the base board [13]. The pinout of the module connector is found in the Mercury Master Pinout [12]. The connector is available in different packaging options and different stacking heights. Some examples are presented in Table 4. Refer to the connector datasheet for more information.

Component	Part Number	Description
Mercury module connector	FX10A-168S-SV	Hirose FX10, 168-pin, 0.5 mm pitch
Base board connector	FX10A-168P-SV(71)	Hirose FX10, 168-pin, 0.5 mm pitch, 4 mm stacking height
Base board connector	FX10A-168P-SV1(71)	Hirose FX10, 168-pin, 0.5 mm pitch, 5 mm stacking height

Table 4: Module Connector Characteristics

Figure 9 indicates the pin numbering for the Mercury module connectors from the top view of the base board. The connector pins are numbered as follows:

- Connector A: from J800-1 to J800-168
- Connector B: from J801-1 to J801-168

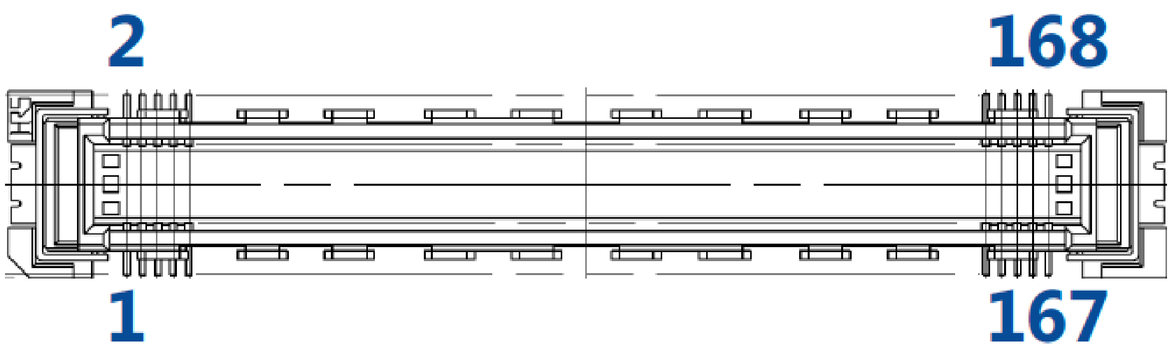

Figure 9: Pin Numbering for the Module Connector

[4]For revisions prior to R1.4, the top component height is 1.35 mm.

3.8 User I/O

3.8.1 Pinout

Information on the Mercury XU5 SoC module pins can be found in the Mercury Master Pinout [12], and in the additional document Mercury Mars Module Pin Connection Guidelines [11].

Tip

The pin types on the schematic of the module connector and in the master pinout document are for reference only. On the Mercury XU5 SoC module, the connected pins might not have the targeted functions (such as primary clocks, differential pins, transceiver signals, etc).

The naming convention for the user I/Os located in HP banks is:
IO_B<BANK>_L<PAIR_NUMBER>_<SPECIAL_FUNCTION>_<PACKAGE_PIN>_<POLARITY>.

For example, IO_B66_L4_AD7_G3_P is located on pin G3 of I/O bank 66, pair 4, it is a System Monitor differential auxiliary analog input capable pin and it has positive polarity, when used in a differential pair.

The HD banks are numbered differently depending on the MPSoC device assembled on the module. Table 5 presents the mapping between the generic bank letters and the device-specific bank numbers.

Device	Bank			
	E	F	N	O
ZU2 ZU3	25	26	24	44
ZU4 ZU5	45	46	44	43

Table 5: Mapping Between the Generic I/O Bank Letters and the Device-Specific I/O Bank Numbers

The naming convention for the user I/Os located in HD banks is:
IO_B<BANK_LETTER>_L<PAIR_NUMBER><_SPECIAL_FUNCTION>_<PACKAGE_PIN>_<POLARITY>

For example, IO_BO_L6_HDGC_AD6_AD12_N is located on pin AD12 of I/O bank O, pair 6, it is a System Monitor differential auxiliary analog input capable pin and also a clock capable pin and it has negative polarity, when used in a differential pair.

The global clock capable pins are marked with “GC” (HP I/O banks) or with “HDGC” (HD I/O banks) in the signal name. For details on their function and usage, refer to the AMD documentation.

Table 6 includes information related to the total number of I/Os available in each I/O bank and possible limitations.

Signal Name	Sign.	Pairs	Differential	Single-ended	Bank	Bank Type[5]
IO_B65_<...>	44	22	In/Out	In/Out	65	HP
IO_B66_<...>	48	24	In/Out	In/Out	66	HP
IO_BE_<...>	4	2	In/Out (no LVDS/LVPECL outputs supported; internal differential termination not supported) Refer to Section 3.8.3 for details.	In/Out	E	HD
IO_BF_<...>	2	1	In/Out (no LVDS/LVPECL outputs supported; internal differential termination not supported) Refer to Section 3.8.3 for details.	In/Out	F	HD
IO_BN_<...>	24	12	In/Out (no LVDS/LVPECL outputs supported; internal differential termination not supported) Refer to Section 3.8.3 for details.	In/Out	N	HD
IO_BO_<...>	24	12	In/Out (no LVDS/LVPECL outputs supported; internal differential termination not supported) Refer to Section 3.8.3 for details.	In/Out	O	HD
Total	**146**	**73**	–	–	–	–

Table 6: User I/Os

Not all I/Os listed in Table 6 are available on the module connector. Certain user I/Os on the module connectors can be connected to various MPSoC I/Os, depending on the assembly variant. Section 3.8.2 lists and describes the connectivity for these pins for each assembly variant. The multi-use signals on the module connector are not named according to the naming convention described above.

The multi-gigabit transceiver (MGT) are described in Section 3.9.

3.8.2 I/O Pin Exceptions

The I/O pin exceptions are pins with special functions or restrictions (for example, when used in combination with certain Mercury boards they may have a specific role).

PCIe Reset Signal (PERST#)

Table 7 lists the I/O pin exceptions on the Mercury XU5 SoC module related to the PCIe reset connection.

[5] HD = high density pins, HP = high performance pins. Refer to the Zynq UltraScale+ MPSoC Data Sheet: Overview [32] for details.

I/O Name	Module Connector Pin	Description
PS_MIO42_PERST#	A-104	When the pin has a low value, its value is routed via a 1 kΩ resistors to ETH0_TXD3_PERST# pin (MIO[30]) and via a 47 kΩ resistor to IO_B65_L24_PERSTN_H8_N (module pin B-126) for PCIe PERST# connection implementation.

Table 7: I/O Pin Exceptions - PERST#

When the Mercury XU5 SoC module is used in combination with a Mercury+ PE1 base board as a PCIe device, the PERST# signal coming from the PCIe edge connector on the module connector pin A-104 (PS_MIO42_PERST#) is driven further to IO_B65_L24_PERSTN_H8_N and to ETH0_TXD3_PERST# (MIO[30]) when its value is low.

When a PCIe block on the PL side is used, the PERST# signal is connected to the FPGA pin IO_B65_L24_PERSTN_H8_N via a 47 kΩ resistor. In situations in which a custom board is used or PCIe functionality on the PL side is not required, this FPGA pin can be used in the same manner as a regular I/O pin.

When a PCIe block on the PS side is used, the PERST# signal is routed via a 1 kΩ resistor to MIO[30]. This is the default MIO pin used for the reset signal of the PCIe PS built-in block, therefore it was chosen for the reset implementation. The Ethernet controller 0 is disabled when the PCIe hard block is used. Any other valid position for PERST# would have resulted in having the Ethernet controller disabled.

Using a PCIe block in the PL simultaneously with Gigabit Ethernet 0 interface on the PS side is possible. Simultaneous usage of two PCIe endpoints on the PL and PS sides is not supported and was not tested on Enclustra side.

In situations in which PCIe functionality is not required, PS_MIO42_PERST# pin can be used in the same manner as a regular MIO pin.

For root complex applications the PERST# signal can be placed on any unused MIO pin (the restriction on MIO[30] and MIO[42] does not apply in this case).

Assembly Options and Migration between Modules

Depending on the assembled MPSoC device on the Mercury XU5 SoC module, the type and number of user I/Os available on the module connector may differ.

On the Mercury XU5 SoC modules equipped with bigger MPSoC devices (ZU4/ZU5) there are four GTH MGT lanes and two differential clock inputs available, in addition to the GTR MGT lanes and clocks located on the PS side. The location of the PL MGT lanes differs between G1 and non-G1 variants.

On the modules equipped with smaller MPSoC devices (ZU2/ZU3), the signals on the module connector are routed to regular I/Os instead of GTH MGTs.

Table 8 presents which resistors are mounted for each assembly option. The corresponding connections are presented in Table 9 and depicted in Figures 10, 11 and 12. The signals on the module connector are routed to different types of I/Os, depending on the assembly option. To find out where exactly these pins are routed, refer to the naming conventions for regular user I/Os (Section 3.8.1) and for MGT signals (Section 3.9).

The assembly options affect the MGT connections on connector B (depending mainly on the MPSoC device's capabilities) and two pins on connector A, which can be routed to MIO pins (PS side) or to FPGA pins (PL side).

For migration from the Zynq-7000 family modules, Mercury ZX1-30 and Mercury ZX5, to the Zynq UltraScale+ family, the additional "G1" module variants with ZU4 or ZU5 devices can be used. These variants offer MGT and MIO/FPGA pins (A-82, A-84) compatibility. For ZX1 modules having 8 MGT lanes (ZX1-35/ZX1-45 variants), only partial pinout compatibility can be achieved.

The "G1" assembly variants can be also be useful in cases where the end application does not require GTR transceivers, but instead more regular I/Os.

Design support files such as the Mercury Master Pinout [12], Mercury XU5 SoC Module User Schematics [6], and Mercury XU5 SoC Module FPGA Pinout Assembly Variants Excel Sheet [5] offer additional information on assembly options and migration guidelines. In the User Schematic, this information is depicted in the "Assembly Variants" section at the end of the PDF file (MGT_A, MGT_B, MGT_C).

Custom assembly variants are also available. Contact Enclustra support if none of the standard options fulfills your system requirements.

Assembly Option	Status	Mounted Resistors	2CG/2EG/3EG	4CG/4EV/5EV	4CG/4EV/5EV-G1	Comment
MGT_A	Equipped	R1412 – R1420	•	•	–	Figure 10
#MGT_A#	DNE	R1402 – R1410	–	–	•	
MGT_B	Equipped	R217, R219, R1431 – R1440	–	•	–	Figure 11
#MGT_B#	DNE	R218, R220, R1421 – R1430	•	–	•	
MGT_C	Equipped	R1411	–	•	•	Figure 12
#MGT_C#	DNE	R1401	•	–	–	

Table 8: Definition of MGT and I/O Signals Assembly Options

Assembly Option	Mod. Conn. Pin	2CG/2EG/3EG	4CG/4EV/5EV	4CG/4EV/5EV-G1
MGT_A	B-4, B-6	GTR Bank 505	GTR Bank 505	GTH Bank 224
	B-13:44	GTR Bank 505	GTR Bank 505	GTH Bank 224
MGT_B	A-82, A-84	Bank F	Bank 501	Bank F
	B-3, B-5	HP Bank 66	GTH Bank 224	HP Bank 66
	B-7, B-9	HP Bank 66	GTR Bank 505	HP Bank 66
	B-45:71	HP Bank 66	GTH Bank 224	HP Bank 66
MGT_C	B-10, B-12	GTR Bank 505	GTH Bank 224	GTH Bank 224

Table 9: Connections of MGT and I/O Signals per Product Model

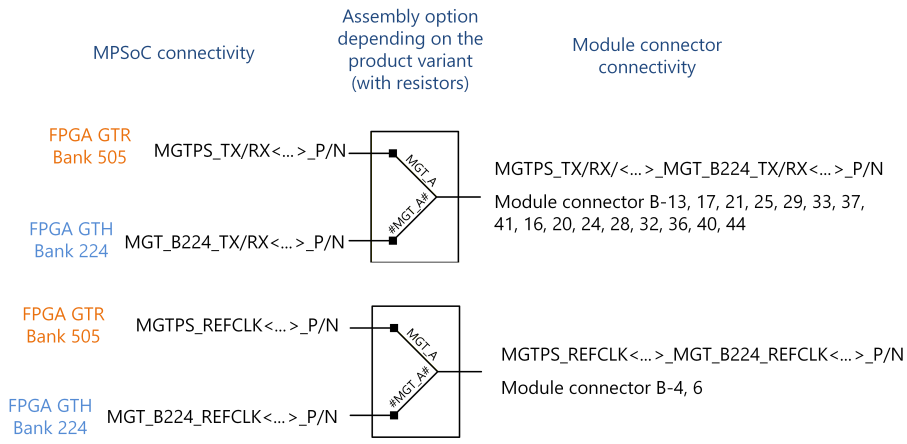

Figure 10: Connections of the MGT_A Assembly Option

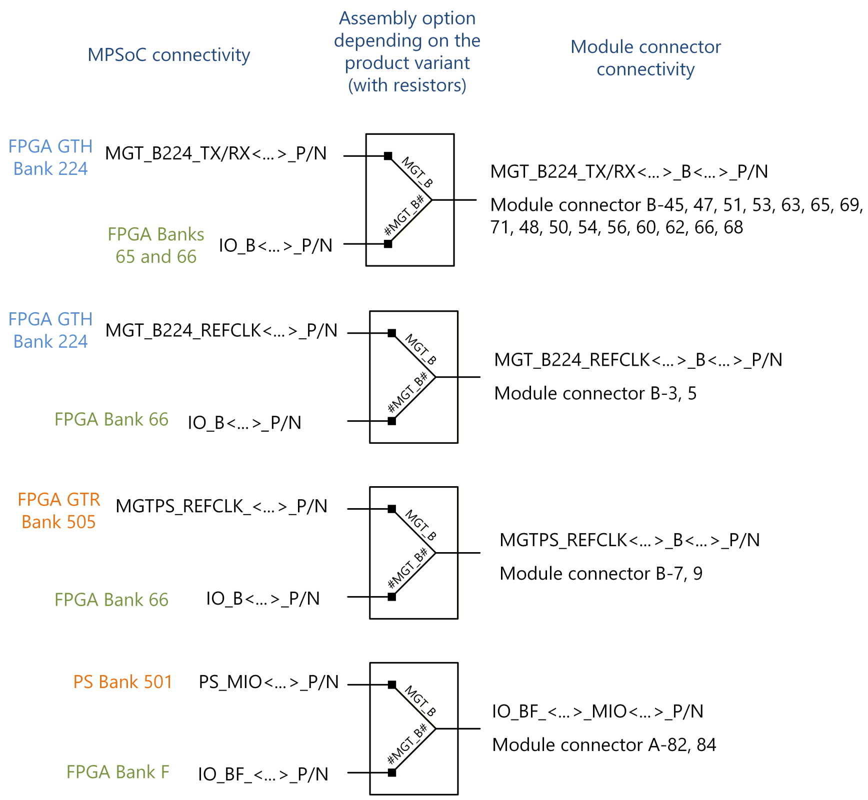

Figure 11: Connections of the MGT_B Assembly Option

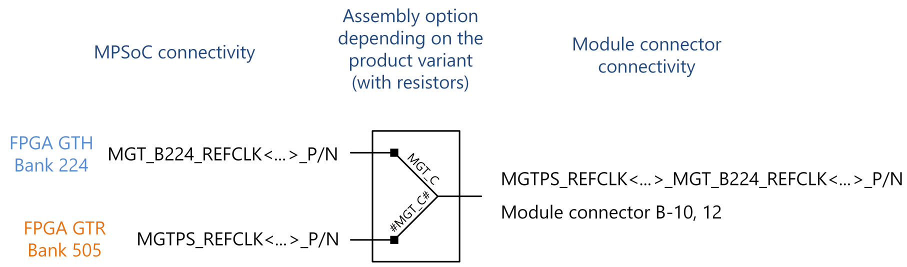

Figure 12: Connections of the MGT_C Assembly Option

3.8.3 Differential I/Os

When using differential pairs, a differential impedance of 100 Ω must be matched on the base board, and the two nets of a differential pair must have the same length.

The information regarding the length of the signal lines from the MPSoC device to the module connector is available in Mercury XU5 SoC Module IO Net Length Excel Sheet [3]. This enables the user to match the total length of the differential pairs on the base board if required by the application.

> **Tip**
>
> The trace length of various signals may change between revisions of the Mercury XU5 SoC module. Use the information provided in the Mercury XU5 SoC Module IO Net Length Excel Sheet [3] to check which signals are affected. The differential signals will also be routed differentially in subsequent product revisions.

The HD bank I/Os cannot be used as LVDS/LVPECL outputs, but they can still be used as LVDS/LVPECL differential inputs.

For information about signal terminations, refer to Section 3.8.6.

3.8.4 I/O Banks

Table 10 describes the main attributes of the Programmable Logic (PL) and Processing System (PS) I/O banks, and indicates which peripherals are connected to each I/O bank. All I/O pins within a particular I/O bank must use the same supply voltage (VCC_IO) and reference voltage (VREF).

Bank	Bank Type	Connectivity	Supply Voltage	Ref. Voltage
PL MGT Banks				
224[6]	GTH	Module connector[7]	0.9 V	–
PL I/O Banks				
64	HP	PL DDR4 SDRAM, clock oscillator	1.2 V	0.6 V
65	HP	Module connector[7], LEDs	VCC_IO_B65, user selectable	½ × VCC_IO_B65
66	HP	Module connector[7]	VCC_IO_B66, user selectable	½ × VCC_IO_B66

Continued on next page...

Bank	Bank Type	Connectivity	Supply Voltage	Ref. Voltage
E	HD	Gigabit Ethernet PHY 1, I2C, module connector	VCC_CFG_MIO, user selectable	–
F	HD	Module connector[7]	VCC_IO_BN, user selectable	–
N	HD	Module connector	VCC_IO_BN, user selectable	–
O	HD	Module connector	VCC_IO_BO, user selectable	–
PS Banks				
500	PS	eMMC and QSPI flash devices, I2C, LEDs	1.8 V	–
501	PS	Gigabit Ethernet PHY 0, module connector	VCC_CFG_MIO, user selectable	–
502	PS	USB PHY 0, USB PHY 1	1.8 V	–
503	PS	FPGA PS configuration	VCC_CFG_MIO, user selectable	–
504	PS DDR	DDR4 SDRAM	1.2 V	–
505	PS GTR	Module connector[7], GTR oscillators	VCC_PSINT	–

Table 10: I/O Banks

3.8.5 VCC_IO Usage

The voltages for the I/O banks located on the module connector are configurable by applying the required voltage to the VCC_IO_B[x], respectively VCC_CFG_[x] pins. All VCC_IO_B[x] or VCC_CFG_[x] pins in a given bank must be connected to the same voltage. Details on connectivity in I/O banks having generic names (for example O or N) are presented in Section 3.8.4.

For compatibility with other Enclustra Mercury modules, it is recommended to use a single I/O voltage per module connector.

[6] This bank is only available on ZU4 and ZU5 devices.
[7] Not all I/Os are available on the module connector. Check the assembly variants description in Section 3.8.2.

Signal Name	MPSoC Pins	Supported Voltages[8]	Connector A Pins	Connector B Pins
VCC_CFG_MIO	VCCO_PSIO1_501, VCCO_PSIO3_503, VCCO_BE[9]	1.8 V – 3.3 V ±5%	74, 77	–
VCC_IO_BO	VCCO_BO[9]	1.2 V – 3.3 V ±5%[10]	41	–
VCC_IO_BN	VCCO_BN[9], VCCO_BF[9]	1.2 V – 3.3 V ±5%[10]	38	–
VCC_IO_B65	VCCO_65	1.0 V – 1.8 V ±5%	–	64, 88, 140
VCC_IO_B66	VCCO_66	1.0 V – 1.8 V ±5%	–	67, 95, 143

Table 11: VCC_IO Pins

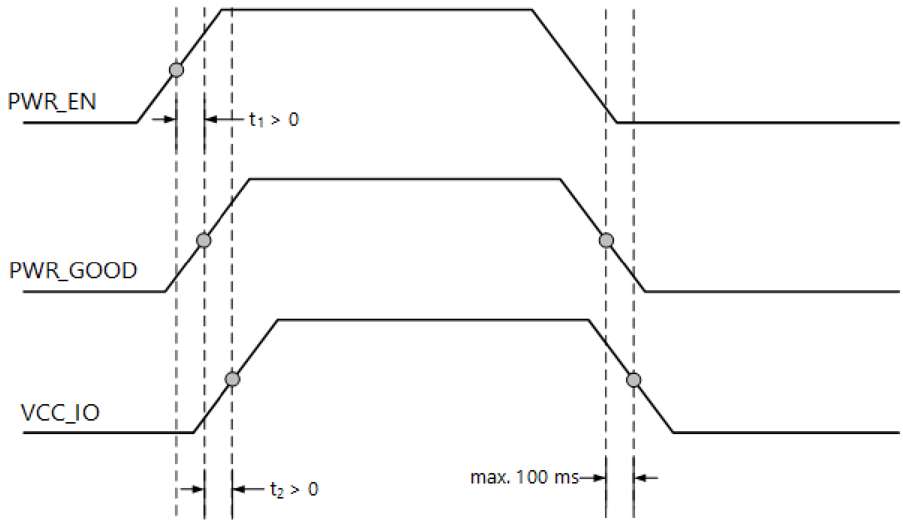

Figure 13: Power-Up Sequence, VCC_IO in Relation with PWR_GOOD and PWR_EN Signals

NOTICE

Damage to the device due to unsuitable voltage

Unsuitable voltages may damage the MPSoC device as well as other devices on the Mercury XU5 SoC module.

- Only use VCC_IO voltages compliant with the assembled MPSoC device.

[8] Only discrete values are allowed. Refer to Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics [31] for details.
[9] For HD I/O banks generic supply names are used. Refer to Section 3.8.4 for details on I/O banks connectivity and supplies.
[10] For voltages of 3.3 V for VCC_IO_BO and VCC_IO_BN the tolerance range is -5% to +3%.

NOTICE

Damage to the device due to floating VCC_IO pins

Floating VCC_IO pins reduce ESD protection.

- Do not leave any VCC_IO pin floating.

CAUTION

Injury due to uncontrolled device

If an I/O is connected to an external device, violating the power sequence or leaving the corresponding VCC_IO pin floating will leave the pin in an undefined state. This can lead to any behavior of the devices attached to this pin and, potentially, to damage or injuries.

- Follow the power sequence diagram shown in Figure 13. This ensures that the I/Os are tri-stated at power-on and power-off.
- Do not leave VCC_IO pins floating.

3.8.6 Signal Terminations

Differential Inputs

Internal differential termination is not supported for the HD pins. Differential input pairs on the module connector may be terminated by external termination resistors on the base board (close to the module pins).

Single-Ended Outputs

There are no series termination resistors on the Mercury XU5 SoC module for single-ended outputs. If required, series termination resistors may be assembled on the base board (close to the module pins).

3.8.7 Multiplexed I/O (MIO) Pins

Details on the MIO/EMIO terminology are available in the Zynq UltraScale+ Device Technical Reference Manual [27].

Some of the MIO pins on the Mercury XU5 SoC module are connected to on-board peripherals, while others are available as GPIOs. The suggested functions below are for reference only. Always verify your MIO pinout with the AMD device handbook.

Table 12 gives an overview over the MIO pin connections on the Mercury XU5 SoC module. Only the pins marked with “user functionality” are available on the module connector.

MIO Pins	Function(s)	Connection(s)
[0:5]	QSPI flash	QSPI flash
[6]	QSPI feedback clock	–[11]
[7:9]	Unused	–
[10:11]	I2C	On-board I2C bus and module connector via level shifter
[12]	I2C interrupt	On-board I2C bus
[13:22]	eMMC flash	eMMC flash
[23]	Unused	–
[24:25]	LED0#, LED1#	On-board LEDs
[26:29,31:37]	Ethernet	Gigabit Ethernet PHY 0
[30]	Ethernet PCIe block PERST# signal	Gigabit Ethernet PHY 0 Module connector via series resistor
[38]	UART RX[12] User functionality	Module connector
[39]	UART TX[12] User functionality	Module connector
[40:41]	User functionality	Module connector
[42]	PCIe block PERST# signal[13] User functionality	Module connector
[43:44]	User functionality	Module connector
[45:51]	SD card User functionality	Module connector
[52:63]	USB	USB 2.0 PHY 0
[64:75]	USB	USB 2.0 PHY 1
[76:77]	Ethernet MDIO	Gigabit Ethernet PHY 0

Table 12: MIO Pins Connections Overview

[11]This pin is intentionally left unconnected to allow enabling the QSPI "Feedback Clk" and achieving QSPI transfer speeds greater than 40 MHz. Refer to the Zynq UltraScale+ Device Technical Reference Manual [27] for more information.

[12]UART RX is an MPSoC input. UART TX is an MPSoC output.

[13]Used for PCIe PERST# connection implementation. Refer to Section 3.8.2 for details.

3.8.8 Analog Inputs

The Zynq UltraScale+ MPSoC devices contain a system monitor in the PL and an additional system monitor block in the PS. These are used to sample analog inputs and to collect information on the internal voltages and temperatures.

The system monitor block in the PL provides a 10-bit ADC, which supports up to 17 external analog signal lines (1 dedicated differential input, 16 auxiliary differential inputs). The auxiliary analog signal lines of the MPSoC device are available on the module connector. These I/Os have the abbreviation "AD" followed by the ADC channel in the signal name. The ADC input channels are always used differentially. For single-ended applications, the *_N line must be connected to GND. The dedicated channel is not available on the module connector.

The analog input signals can be connected to any normal I/O FPGA bank, provided that all analog pins belong to the same bank. Note that the HD I/O banks have a limited number of analog inputs and they must be connected directly to the SYSMONE4 primitive instead of to the AMD System Management Wizard IP core.

For detailed information on the ADC and system monitor, refer to the UltraScale Architecture System Monitor document [29], Zynq UltraScale+ Device Technical Reference Manual [27] and System Management Wizard Product Guide [30].

Table 13 presents the ADC Parameters for the PL System Monitor (SYSMON). The PS System Monitor is only used for monitoring the on-chip power supply voltages and die temperature.

Parameter	Value (PL SYSMON)
VCC_ADC	1.8 V
VREF_ADC	Internal
ADC Range	0-1 V
Sampling Rate per ADC	0.2 MSPS
Total number of channels available on the module connector	16 (only auxiliary inputs)

Table 13: System Monitor (PL) Parameters

3.9 Multi-Gigabit Transceiver (MGT)

There are two types of multi-gigabit transceivers available on the Mercury XU5 SoC module: GTH transceivers (connected to the PL) and GTR transceivers (connected to the PS). The GTH transceivers are available only on modules equipped with ZU4/ZU5 MPSoC devices.

> **Tip**
>
> For optimal performance of high-speed interfaces, for example, PCIe, use redrivers on the base board.

> **Tip**
>
> The maximum data rate on the transceivers on the Mercury XU5 SoC module depends on the routing path for these signals. When using transceivers at high performance rates, ensure adequate signal integrity over the full signal path.

NOTICE

Damage to the transceivers

No AC coupling capacitors are placed on the Mercury XU5 SoC module on the transceivers.

- If required by your application, ensure that capacitors are mounted on the base board, close to the module pins.

GTH Transceivers

On modules equipped with ZU4/ZU5 there are 4 GTH MGTs available on the Mercury XU5 SoC module. Table 14 describes the connections.

The naming convention for the GTH MGT I/Os is:
MGT_B<BANK>_<FUNCTION>_<PACKAGE_PIN>_<POLARITY>.

For example, MGT_B224_TX2_R4_P is located on pin R4 of MGT I/O bank 224, it is a transmit pin and it has negative polarity.

Signal Name	Signal Description	Pairs	I/O Bank
MGT_B224_RX<...>	MGT receivers	4	224
MGT_B224_TX<...>	MGT transmitters	4	
MGT_B224_REFCLK<...>	MGT reference input clocks	2	
Total		**10**	

Table 14: MGT Pairs

The four GTH pairs and two reference input clock differential pairs are routed by default to module connector B on modules equipped with ZU4/ZU5 devices. Refer to Section 3.8.2 for details on the assembly variants and MGT connectivity.

The GTH MGTs on the MPSoC device support data rates of 12.5 Gbit/s.

The MPSoC devices assembled on the Mercury XU5 SoC module variants 4EV/5EV can support up to two integrated PCIe Gen3 $\times 4$ interfaces on the PL side, implemented using GTH transceivers. Simultaneous usage of these interfaces is limited to the available hardware resources (number of transceivers and lane mapping).

GTR Transceivers

There are four GTR MGT lanes and two reference input clock differential pairs on the Mercury XU5 SoC module connected to I/O bank 505. These are routed by default to module connector B. Refer to Section 3.8.2 for details on the assembly variants and MGT connectivity.

The naming convention for the GTR MGT I/Os is:
MGTPS_<FUNCTION>_<PACKAGE_PIN>_<POLARITY>.

For example, MGTPS_RX2_B28_N is located on pin B28 of PS GTR bank (bank 505), it is a receive pin and it has negative polarity.

The standard Mercury XU5 SoC module variants that use regular MGT routing support the implementation of a PCIe Gen2 $\times$4 interface.

When the PCIe hard block is used, it is not possible to use the Ethernet 0 interface. Ethernet PHY 0 is connected to ETH 0 controller from the PS I/O bank 501. One of the Ethernet TX data signals is shared with the PCIe reset signal (PERST#). Refer to Sections 3.8.2 and 3.8.7 for details on the PERST# connection.

The GTR lanes support data rates of 6 Gbit/s and can be used for the implementation of several interfaces such as PCIe Gen2 $\times$4, USB 3.0, DisplayPort, SATA, or Ethernet SGMII. Refer to the Zynq UltraScale+ Device Technical Reference Manual [27] and to the Zynq UltraScale+ MPSoC Data Sheet: Overview [32] for details.

A 100 MHz LVDS oscillator and a 27 MHz CMOS oscillator provide reference clock inputs to the PS GTR bank 505. Refer to Section 3.11 for details.

3.10 Power

3.10.1 Power Generation Overview

The Mercury XU5 SoC module uses a 5 to 15 V DC power input for generating the on-board supply voltages. Table 15 describes the power supplies generated on the module. The supply voltages accessible on the module connector are indicated with a source "VCC_MOD" in the table.

Generated Supply Name	Voltage Value	Rated Current	Source Supply Name	Shut down via PWR_EN	Influences PWR_GOOD
VCC_INT	0.72/0.85 V/0.9 V (PL core supply)	9 A	VCC_MOD	Yes	Yes
VCC_PSINT	0.85 V/0.9 V (PS core supply)	6 A	VCC_MOD	Yes	Yes
VCC_0V9	0.9 V (MGT and VCU core supply)	4 A[14]	VCC_MOD	Yes	Yes
VCC_1V2	1.2 V	6 A	VCC_MOD	Yes	Yes
VCC_BAT_FPGA	1.2 V	10 mA	VCC_BAT	No	No
VCC_1V8	1.8 V	2 A	VCC_MOD	Yes	Yes
VCC_2V5	2.5 V	0.5 A	VCC_3V3	Yes	No
VCC_3V3	3.3 V	9 A	VCC_MOD	No	Yes
VCC_5V0	5.0 V	0.15 A	VCC_MOD	Yes	No

Table 15: Generated Power Supplies

In the standard configuration, the PL core supply is 0.85 V. For product configurations in which a speed grade -3E MPSoC device is assembled, an assembly variant is available to switch the PL core operating voltage to 0.9 V. Similarly, in situations in which a speed grade -2LE or -1LI device is assembled (custom

[14] For revisions prior to R1.4, the rated current of VCC_0V9 is 3.2 A.

configurations), an assembly variant is available to switch the PL core operating voltage to 0.72 V.

In the standard configuration, the PS core supply is 0.85 V. For custom configurations in which a speed grade -3E MPSoC device is assembled, an assembly variant is available to switch the PS core operating voltage to 0.9 V.

Operation at 0.9 V is not supported on modules revision 1. Refer to the Mercury XU5 SoC Module Known Issues and Changes [7] for details.

Refer to the Mercury Mars Module Pin Connection Guidelines [11] for general rules on the power pins.

3.10.2 Power Enable / Power Good

The Mercury XU5 SoC module provides a power enable input on the module connector. This input may be used to shut down the DC-DC converters and LDOs. The list of power converters that can be disabled via PWR_EN signal is provided in Section 3.10.1.

The PWR_EN input is pulled to VCC_3V3 on the Mercury XU5 SoC module with a 10 kΩ resistor. The PWR_GOOD signal is pulled to VCC_3V3 on the Mercury XU5 SoC module with a 10 kΩ resistor.

PWR_GOOD is an open collector signal and must not be used to drive a load directly. This signal is pulled to ground if the onboard power converters fail or if the module is disabled via PWR_EN. The list of power converters that influence the state of PWR_GOOD signal is provided in Section 3.10.1.

The role of PWR_GOOD and PWR_EN on the VCC_IO power sequence is presented in Section 3.8.5.

NOTICE

Damage to the device due to unsuitable voltage

Appling unsuitable voltage to the power enable or power good pins can damage the Mercury XU5 SoC module.

- Do not actively drive the power enable or power good pins to anything other than ground.
- Do not pull these pins up to a voltage level higher than 3.3 V.

Signal Name	Module Connector Pin	Comment
PWR_EN	A-10	Floating/3.3 V: Module power enabled Driven low: Module power disabled
PWR_GOOD	A-12	0 V: Module supply not ok 3.3 V: Module supply ok

Table 16: Module Power Status and Control Pins

3.10.3 Voltage Supply Inputs

Table 17 describes the power supply inputs on the Mercury XU5 SoC module. The VCC voltages used as supplies for the I/O banks are described in Section 3.8.5.

Supply Name	Module Connector Pins	Voltage	Description
VCC_MOD	A-1, 2, 3, 4, 5, 6, 7, 8, 9, 11	5 - 15 V	Supply for on-module generated power supplies. The 2.5 V supply is generated from the 3.3 V supply. The input current is rated at 3 A (0.3 A per connector pin).
VCC_BAT	A-168	2.7 - 3.6 V	Supply for the battery voltage for MPSoC battery-backed RAM and battery-backed RTC

Table 17: Voltage Supply Inputs

3.10.4 Voltage Supply Outputs

Table 18 presents the supply voltages generated on the Mercury XU5 SoC module, that are available on the module connector.

Supply Name	Module Connector Pins	Voltage	Typical Available Current[15]	Comment
VCC_3V3	A-26, 29, 50, 86 B-55, 79, 115, 127, 152, 155	3.3 V $\pm$5%	4 A (and max. 0.3 A per pin)	Always active
VCC_2V5	A-53, 62, 65, 89	2.5 V $\pm$5%	0.11 A	Controlled by PWR_EN
VCC_1V8	B-52, 76, 108, 128	1.8 V $\pm$5%	1 A	Controlled by PWR_EN

Table 18: Voltage Supply Outputs

NOTICE

Damage to the device due to unsuitable usage of the output pins

- Do not connect any power supply to the voltage supply outputs.
- Do not short circuit any of the voltage supply outputs to ground.

3.10.5 Power Consumption

The power consumption of any MPSoC device strongly depends on the application (on the configured bitstream and I/O activity).

To estimate the power consumption of your design, use the power estimation tool provided by AMD for the corresponding device family, available on the AMD website.

[15] The maximum available output current depends on your design. See Sections 3.10.1 and 3.10.5 for details.

3.10.6 Heat Dissipation

High performance devices like the AMD Zynq UltraScale+ MPSoC need cooling in most applications. Always make sure the MPSoC is adequately cooled.

For Mercury modules an Enclustra heat sink kit is available for purchase along with the product. It represents an optimal solution to cool the Mercury XU5 SoC module. The heat sink body is low profile and usually covers the whole module surface. The kit comes with a gap pad for the MPSoC device, a fan and required mounting material to attach the heat sink to the module PCB and base board PCB. With additional user configured gap pads, it is possible to cool other components on the board as well.

Alternatively, if the Enclustra heat sink does not match the application requirements, a third-party heat sink body (ATS) and an additional gap pad (t-Global) may be used. The Enclustra heat sink kit already contains all necessary items for cooling the module (heat sink body, gap pad, fan, mounting material).

Table 19 lists the heat sink and thermal gap pad part numbers that are compatible with the Mercury XU5 SoC module. Details on the Mercury heat sink kit can be found in the Mercury Heat Sink Kits User Manual [22].

Product Name	Package Name	Enclustra Heat Sink	ATS Heat Sink	t-Global Thermal Gap Pad
Mercury XU5	SFVC784 [28]	ACC-HS3-Set	ATS-52230G-C1-R0	TG-A6200-25-25-1

Table 19: Heat Sink Characteristics

Tip

Adhesive heat sinks are only recommended for prototyping purposes. When the module is used in environments subject to vibrations, additional mechanical fixation is recommended.

NOTICE

Damage to the device due to overheating

Depending on the user application, the Mercury XU5 SoC module may consume more power than can be dissipated without additional cooling measures.

- Ensure that the MPSoC is always adequately cooled by installing a heat sink and/or providing air flow.

3.10.7 Voltage Monitoring

Several pins on the module connector on the Mercury XU5 SoC module are marked as VMON. These are voltage monitoring outputs that are used in the production test for measuring some of the on-board voltages.

It is not allowed to draw power from the voltage monitoring outputs.

Tip

The voltage monitoring outputs are for Enclustra-use only. Pinout changes may be applied between revisions.

Table 20 presents the VMON pins on the Mercury XU5 SoC module.

Signal Name	Mod. Conn. Pin	Assembly Variant	Connection	Description
VMON_0V9	B-167	All	VCC_0V9	0.9 V on-board voltage
VMON_1V2	B-8	Default	VCC_1V2	1.2 V on-board voltage
		Custom	VCC_BAT	MPSoC battery voltage
VMON_INT	A-102	All	VCC_INT	PL core voltage
VMON_PSINT	B-168	All	VCC_PSINT	PS core voltage

Table 20: Voltage Monitoring Outputs

3.11 Clock Generation

A 33.33 MHz oscillator is used for the Mercury XU5 SoC module clock generation. The 33.33 MHz clock is fed to the PS. A 100 MHz LVDS oscillator is connected to FPGA bank 64 and can serve as a reference for the PLL used to generate the clocks required for the PL DDR interface. The signal is terminated with a 100 Ω parallel resistor close to the FPGA pins.

A 100 MHz LVDS oscillator and a 27 MHz CMOS oscillator provide reference clock inputs to the PS GTR bank 505. A 24 MHz clock and a 25 MHz clock are used for the USB PHYs and Ethernet PHYs respectively. The crystal pads for the MPSoC RTC are connected to a 32.768 kHz oscillator on the Mercury XU5 SoC module.

Table 21 describes the clock connections to the MPSoC device.

Signal Name	Frequency	MPSoC Pin	MPSoC Pin Name
CLK33	33.33 MHz	R16	PS_REF_CLK
CLK100_PL_P CLK100_PL_N	100 MHz	AD5 AD4	IO_L13P_T2L0Q_GC_64 IO_L13N_T2L1Q_GC_64
CLK27_GTR_P CLK27_GTR_N	27 MHz	A21 A22	PS_MGTREFCLK3P_505 PS_MGTREFCLK3N_505
CLK100_GTR_P CLK100_GTR_N	100 MHz	C21 C22	PS_MGTREFCLK2P_505 PS_MGTREFCLK2N_505
PS_PADI PS_PADO	32.768 kHz	N17 N18	PS_PADI (crystal pad input for MPSoC built-in RTC) PS_PADO (crystal pad output for MPSoC built-in RTC)

Table 21: Module Clock Resources

3.12 Reset

The power-on reset signal (POR) and the PS system reset signal (SRST) of the MPSoC device are available on the module connector.

Pulling PS_POR# low resets the MPSoC device, the Ethernet and the USB PHYs, and the QSPI and eMMC flash devices. Refer to the Mercury Mars Module Pin Connection Guidelines [11] for general rules regarding the connection of reset pins.

Pulling PS_SRST# low resets the MPSoC device and enables the connection between QSPI flash and module connector, allowing the flash to be programmed from an external SPI master.

For details on the functions of the PS_POR_B and PS_SRST_B signals refer to the Zynq UltraScale+ Device Technical Reference Manual [27].

Table 22 presents the available reset signals. Both signals, PS_POR# and PS_SRST#, have on-board 10 kΩ pull-up resistors to VCC_CFG_MIO. For on-board devices using 1.8 V signaling, a PS_POR# low voltage variant is generated (PS_POR#_LV). PS_POR# is automatically asserted if PWR_GOOD is low.

Signal Name	Connector Pin	MPSoC Pin	MPSoC Pin Name	Description
PS_POR#	A-132	P16	PS_POR_B	Power-on reset
PS_SRST#	A-124	N19	PS_SRST_B	System reset

Table 22: Reset Resources

3.13 LEDs

There are four active-low user LEDs on the Mercury XU5 SoC module. One of them is connected to the PS, one connected to both PS and PL and two connected to the PL.

For the LED that can be driven from both PL and PS, it is recommended to drive the FPGA pin to a high impedance state before driving the PS pin and vice versa.

LED	Signal Name (PS)	MPSoC Pin (PS)	MPSoC Pin Name (PS)	Signal Name (PL)	MPSoC Pin (PL)	Comment
0	LED0#_PS	AB19	MIO[24]	–	–	User function/active-low
1	LED1#_PS	AB21	MIO[25]	LED1#_PL	H2	User function/active-low
2	–	–	–	LED2#_PL	P9	User function, active-low
3	–	–	–	LED3#_PL	K5	User function, active-low

Table 23: User LEDs

The module is also equipped with two status LEDs, which offer details on the configuration process for debugging purposes.

LED	PS Signal Name	PS Signal Location	Comment
E	PS_ERROR	P17 (PS_ERROR_OUT)	Refer to Zynq UltraScale+ Device Technical Reference Manual [27]
S	PS_STATUS	M20 (PS_ERROR_STATUS)	Refer to Zynq UltraScale+ Device Technical Reference Manual [27]

Table 24: Status LEDs

3.14 DDR4 SDRAM (PS)

There are two DDR4 SDRAM channels on the Mercury XU5 SoC module: one attached directly to the PS side (which is available only as a shared resource to the PL side) and one attached directly to the PL side.

The DDR4 SDRAM connected to the PS is mapped to I/O bank 504. The memory configuration on the Mercury XU5 SoC module supports ECC error detection and correction. The correction code type used is single bit error correction and double bit error detection (SEC-DED).

Five 16-bit memory chips are used to build an 72-bit wide memory (8 bits are unused): 64 bits for data and 8 bits for ECC.

On the smallest module variant (ME-XU5-2CG-1E-D10H), the DDR4 chip for ECC and half of the DDR4 chips for data are not assembled. In total, two memory chips are used for the PS DDR4 SDRAM.

The maximum memory bandwidth on the Mercury XU5 SoC module regular variants (full bandwidth) is:
2'400 Mbit/s $\times$ 64 bit = 19'200 MB/s
and for the smallest variant (half bandwidth) is:
2'400 Mbit/s $\times$ 32 bit = 9'600 MB/s

3.14.1 DDR4 SDRAM Characteristics

Table 25 describes the memory availability and configuration on the Mercury XU5 SoC module.

Module	Density	Configuration
ME-XU5-D10H ME-XU5-D11E	4 Gbit	256 M $\times$ 16 bit
ME-XU5-D12E	8 Gbit	512 M $\times$ 16 bit
ME-XU5-D13E	16 Gbit	1 G $\times$ 16 bit

Table 25: DDR4 SDRAM (PS) Characteristics

3.14.2 Signal Description

Refer to the Mercury XU5 SoC Module FPGA Pinout Excel Sheet [4] for detailed information on the DDR4 SDRAM connections.

3.14.3 Termination

> **Tip**
> No external termination is implemented for the data signals on the Mercury XU5 SoC module. Enclustra strongly recommends enabling the on-die termination (ODT) feature of the assembled device.

3.14.4 Parameters

Refer to the Mercury XU5 SoC Module Reference Design [2] for DDR4 settings guidelines.

The DDR4 SDRAM parameters to be set in the Vivado project are presented in Table 26.

Table 26 shows the parameters of the PS DDR4 SDRAM to be set in the Vivado/Libero project such that it corresponds to the reference design [2] of the Mercury XU5 SoC module.

Parameter	Value
Requested device frequency	1’200 MHz
Memory type	DDR4
Effective DRAM bus width	64 bit (32 bit for ME-XU5-2CG-1E-D10H variant)
ECC	Enabled (Disabled for ME-XU5-2CG-1E-D10H variant)
Speed bin	DDR4 2400T
CAS latency	17 cycles
RAS to CAS delay	17 cycles
Precharge time	17 cycles
CAS write latency	12 cycles
tRC	46.16 ns
tRASmin	32 ns
tFAW	30 ns
Additive latency	0 cycles
DRAM chip bus width (per die)	16 bits
DRAM device capacity (per die)	4’096, 8’192, or 16’384 Mbits
Bank group address count	1 bit
Bank address count	2 bit
Row address count	15-17 bit
Column address count	10

Table 26: DDR4 SDRAM (PS) Parameters

3.15 DDR4 SDRAM (PL)

The DDR4 SDRAM connected to the PL is mapped to I/O bank 64. The DDR bus width is 16-bit.

The DDR4 SDRAM memory connected to the PL supports different bandwidths depending on the MPSoC device assembled on the module:

- Speed grade 1 devices: up to 2’133 Mbit/s (1’066 MHz)
- Speed grade 2 and 3 devices: up to 2’400 Mbit/s (1’200 MHz)

Hence, the maximum memory bandwidth on the Mercury XU5 SoC module for the DDR4 SDRAM (PL) is:

- Speed grade 1 devices: up to 2’133 Mbit/s × 16 bit = 4’266 MB/s
- Speed grade 2 and 3 devices: up to 2’400 Mbit/s × 16 bit = 4’800 MB/s

Note that for MPSoC low power mode (at 0.72 V) the DDR speed is lower than mentioned above. For details, refer to the Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics [31].

3.15.1 DDR4 SDRAM Characteristics

Table 25 describes the memory availability and configuration on the Mercury XU5 SoC module.

Module	Density	Configuration
ME-XU5-D10H ME-XU5-D11E	4 Gbit	256 M $\times$ 16 bit
ME-XU5-D12E	8 Gbit	512 M $\times$ 16 bit
ME-XU5-D13E	16 Gbit	1 G $\times$ 16 bit

Table 27: DDR4 SDRAM (PL) Characteristics

3.15.2 Signal Description

Refer to the Mercury XU5 SoC Module FPGA Pinout Excel Sheet [4] for detailed information on the DDR4 SDRAM connections.

3.15.3 Termination

Tip

No external termination is implemented for the data signals on the Mercury XU5 SoC module. Enclustra strongly recommends enabling the on-die termination (ODT) feature of the assembled device.

3.15.4 Parameters

Refer to the Mercury XU5 SoC Module Reference Design [2] for DDR4 settings guidelines.

The DDR4 SDRAM parameters to be set in the Vivado project are presented in Table 28.

Table 28 shows the parameters of the PL DDR4 SDRAM to be set in the Vivado/Libero project such that it corresponds to the reference design [2] of the Mercury XU5 SoC module.

Parameter	Value
Memory Device Interface Speed (ps)	938
Reference Input Clock Speed (ps)	10'000 (100 MHz)[16]
Memory Part	MT40A256M16 / MT40A512M16 / MT40A1G16 [17]
Data Width	16
Data Mask and DBI	DM NO DBI
Cas Latency	16
Cas Write Latency	11

Table 28: DDR4 SDRAM (PL) Parameters

3.16 QSPI Flash

The QSPI flash can be used to boot the PS, and to store the FPGA bitstream, ARM application code and other user data.

3.16.1 QSPI Flash Characteristics

Table 29 describes the memory availability and configuration on the Mercury XU5 SoC module.

As there is one QSPI flash chip assembled on the Mercury XU5 SoC module, type "single" must be selected when programming the flash from Vivado tools.

Part Number	Size	Manufacturer
S25FL512S	512 Mbit	Infineon (Spansion)

Table 29: QSPI Flash Characteristics

> **Tip**
>
> Different flash memory devices may be assembled in future revisions of the Mercury XU5 SoC module. Any flash memory with a different speed and temperature range fulfilling the requirements of the module variant may be used.

3.16.2 Signal Description

The QSPI flash is connected to the PS MIO pins 0 to 5. Some of these signals are available on the module connector, allowing the user to program the QSPI flash from an external source.

The reset of the QSPI flash is connected to the PS_POR#_LV power-on reset signal.

Refer to Section 4 for details on programming the flash memory.

[16] An exact period of 10'000 ps may not be achievable. The clock speed closest to the desired frequency should be selected.
[17] The memory devices assembled on the module may not be available in Vivado. In this case, a similar memory part with compatible timing requirements should be selected.

> **Tip**
>
> For optimal signal integrity, avoid long traces when when connecting the QSPI flash signals on the base board. Long traces or high capacitance may disturb the data communication between the MPSoC and the flash device.

3.16.3 Configuration

The QSPI flash supports up to 50 MHz operation for standard read. For fast, dual and quad read speed values, refer to the flash device datasheet.

Note that the "Feedback Clk" option on pin MIO6 must be enabled in the Zynq configuration for clock rates higher than 40 MHz.

Refer to Zynq UltraScale+ Device Technical Reference Manual [27] for details on booting from the QSPI flash.

Using the Write Register (WWR) command can corrupt the QSPI flash. This issue is described in more details in the Mercury XU5 SoC Module Known Issues and Changes [7].

3.17 eMMC Flash

The eMMC flash can be used to boot the PS, and to store the FPGA bitstream, ARM application code and other user data.

3.17.1 eMMC Flash Characteristics

The Mercury XU5 SoC module is equipped with a 16 GB eMMC flash.

> **Tip**
>
> Different flash memory devices may be assembled in future revisions of the Mercury XU5 SoC module. Any flash memory with a different speed and temperature range fulfilling the requirements of the module variant may be used.

3.17.2 Signal Description

The eMMC flash signals are connected to the MIO pins 13 to 22 for 8-bit data transfer mode. The command signal has a 4.7 kΩ pull-up resistor to 1.8 V and the data signal lines have 47 kΩ pull-up resistors to 1.8 V.

3.18 SD Card

An SD card can be connected to the PS MIO pins 45 to 51. The corresponding MIO pins are available on the module connector. Information on SD card boot mode is available in Section 4.5.4.

External pull-ups are needed for SD card operation. Depending on the selected voltage for VCC_CFG_MIO, a level shifter to 3.3 V may be required (some level shifters also have built-in pull-ups).

For booting from an Ultra High Speed (UHS) SD card, an SD 3.0 compliant level shifter is required on the base board and VCC_CFG_MIO must be set to 1.8 V. This boot mode has not been tested, but it may be supported in the future.

3.19 Gigabit Ethernet (PS)

One 10/100/1000 Mbit Ethernet PHY is connected to the PS via RGMII interface. A second Ethernet PHY is connected to the PL and is described in Section 3.20.

3.19.1 Ethernet PHY Characteristics

Table 30 describes the Ethernet PHY (PS) device assembled on the Mercury XU5 SoC module.

Part Number	Manufacturer	Description
KSZ9031RNX	Microchip (Micrel)	10/100/1000 Mbit

Table 30: Gigabit Ethernet PHY (PS) Characteristics

3.19.2 Signal Description

Ethernet PHY 0 is connected to ETH 0 controller from the PS I/O bank 501. One of the Ethernet TX data signals is shared with the PCIe reset signal (PERST#). If the application requires a hard PCIe block, the ETH 0 interface is not available. Refer to Section 3.8.2 for details on the PERST# connection.

> **Tip**
>
> Remember that the Gigabit Ethernet 0 interface is not available when the PCIe endpoint in the PS is used, because of the PERST# connection.

The interrupt output of the Ethernet PHY is connected to the I2C interrupt line, available on MIO12 pin.

3.19.3 External Connectivity

The Ethernet signal lines can be connected directly to the magnetics. Refer to the Mercury Mars Module Pin Connection Guidelines [11] for details regarding the connection of Ethernet signals.

3.19.4 MDIO Address

The MDIO address assigned to PHY 0 is 3, and the PHY can be configured via MIO pins 76 and 77.

3.19.5 PHY Configuration

The configuration of the Ethernet PHY is bootstrapped when the PHYs are released from reset. Make sure all I/Os on the RGMII interface are initialized and all pull-up or pull-down resistors are disabled at that moment.

The bootstrap options of the Ethernet PHYs are set as indicated in Table 31.

Pin	Signal Value	Description
MODE[3-0]	1110	RGMII mode: advertise all capabilities (10/100/1000, half/full duplex) except 1000Base-T half duplex.
PHYAD[2-0]	011	MDIO address 3
CLK125_EN	0	125 MHz clock output disabled
LED_MODE	1	Single LED mode

Table 31: Gigabit Ethernet PHY (PS) Configuration - Bootstraps

For the Ethernet PHY configuration via the MDIO interface, the MDC clock frequency must not exceed 2 MHz.

The PHY is configured in single LED mode with active-low LEDs 1 and 2.

3.19.6 RGMII Delays Configuration

The Ethernet PHY (PS) is connected directly to the hard MAC controller present in the MPSoC device. In order to achieve the best sampling eye for the RX and TX data, it is recommended to adjust the pad skew delays as specified in Table 32. These values have been successfully tested on Enclustra side.

The delays can be adjusted by programming the RGMII pad skew registers of the Ethernet PHY. Refer to the PHY datasheet for details.

PHY Register Name	Register Value [binary]	Delay Value
RXD0-RXD3	0111	0 ps
RX_DV	0111	0 ps
RX_CLK	01111	0 ps
TXD0-TXD3	0111	0 ps
TX_EN	0111	0 ps
GTX_CLK	11110	900 ps

Table 32: Gigabit Ethernet PHY (PS) Configuration for KSZ9031 - RGMII Delays

For RX_CLK, the PHY itself uses an additional default delay of 1.2 ns.

3.20 Gigabit Ethernet (PL)

One 10/100/1000 Mbit Ethernet PHY is connected to the PL via RGMII interface. A second Ethernet PHY is connected to the PS and is described in Section 3.19.

3.20.1 Ethernet PHY Characteristics

Table 33 describes the Ethernet PHY (PL) device assembled on the Mercury XU5 SoC module.

Part Number	Manufacturer	Description
KSZ9031RNX	Microchip (Micrel)	10/100/1000 Mbit

Table 33: Gigabit Ethernet PHY (PL) Characteristics

3.20.2 Signal Description

Ethernet PHY 1 is connected to FPGA bank E, for usage with a soft Ethernet MAC IP core providing RGMII interface for communication with the PHY.

Alternatively, the Ethernet MAC from the PS can be used and mapped to EMIO pins. An GMII to RGMII converter must be used to convert the bus to the appropriate interface standard. The AMD GMII to RGMII converter cannot be used on the Mercury XU5 SoC module because this IP core includes I/O delay macros that are not supported in HD I/O banks (where the Ethernet pins are mapped).

Enclustra provides a netlist of a suitable GMII to RGMII converter, which is included in every Mercury XU5 SoC Module Reference Design [2]. A brief description of this GMII to RGMII converter can be found in the Enclustra Gigabit Ethernet Application Note [24].

The reset pin of the Ethernet PHY has a pull-down resistor and needs to be driven high to release the PHY from reset. The reset pin is connected to FPGA pin B10 from bank E. The interrupt output of the Ethernet PHY is connected to FPGA pin C11 from the same bank.

3.20.3 External Connectivity

The Ethernet signal lines can be connected directly to the magnetics. Refer to the Mercury Mars Module Pin Connection Guidelines [11] for details regarding the connection of Ethernet signals.

3.20.4 MDIO Address

The MDIO address assigned to PHY 1 is 3, and the PHY can be configured via FPGA pins A10 and B11 from bank E.

3.20.5 PHY Configuration

The configuration of the Ethernet PHY is bootstrapped when the PHYs are released from reset. Make sure all I/Os on the RGMII interface are initialized and all pull-up or pull-down resistors are disabled at that moment.

The bootstrap options of the Ethernet PHYs are set as indicated in Table 34.

Pin	Signal Value	Description
MODE[3-0]	1110	RGMII mode: advertise all capabilities (10/100/1000, half/full duplex) except 1000Base-T half duplex.
PHYAD[2-0]	011	MDIO address 3
Clk125_EN	0	125 MHz clock output disabled
LED_MODE	1	Single LED mode
LED1/LED2	1	Active-low LEDs

Table 34: Gigabit Ethernet PHY (PL) Configuration - Bootstraps

For the Ethernet PHY configuration via the MDIO interface, the MDC clock frequency must not exceed 2 MHz.

3.20.6 RGMII Delays Configuration

The Ethernet PHY (PL) is connected to the PL side of the MPSoC device, to be used in combination with a soft MAC controller. In order to achieve the best sampling eye for the RX and TX data, it is recommended to adjust the timing constraints of the FPGA pins and/or the pad skew delays of the Ethernet PHY as specified in Table 35. The Enclustra Gigabit Ethernet Application Note [24] explains how to configure these parameters.

The delays can be adjusted by programming the RGMII pad skew registers of the Ethernet PHY. Refer to the PHY datasheet for details.

PHY Register Name	Register Value [binary]	Delay Value
RXD0-RXD3	1111	480 ps
RX_DV	1111	480 ps
RX_CLK	00000	-900 ps
TXD0-TXD3	0111	0 ps
TX_EN	0111	0 ps
GTX_CLK	01111	0 ps

Table 35: Gigabit Ethernet PHY (PL) Configuration for KSZ9031 - RGMII Delays

For RX_CLK, the PHY itself uses an additional default delay of 1.2 ns.

3.21 USB 2.0

Two USB 2.0 PHYs are available on the Mercury XU5 SoC module, both connected to the PS to I/O bank 502. USB PHY 0 can be configured as host or device, while USB PHY 1 can be used only as host.

3.21.1 USB PHY Characteristics

Table 36 describes the USB PHYs device assembled on the Mercury XU5 SoC module.

Part Number	Manufacturer	Description
USB3320C	Microchip	USB 2.0 PHY

Table 36: USB 2.0 PHY Characteristics

3.21.2 Signal Description

The ULPI interface for the PHY 0 is connected to MIO pins 52 to 63, while the interface for the PHY 1 is connected to MIO pins 64 to 75.

3.22 USB 3.0

AMD Zynq UltraScale+ devices feature two built-in USB 3.0 controllers and PHYs, configurable as host or device. The PHY interface used by the USB 3.0 controller is PIPE3, supporting a 5 Gbit/s data rate in host or device modes. The interface of each USB 3.0 controller uses one of the PS GTR lanes.

A 100 MHz differential clock is available on the module and connected to PS_MGTREFCLK2 pins, to be used as a reference clock for the USB 3.0 interface. It is also possible to provide another reference clock from the base board to the MGTPS_REFCLK* pins.

Details on the built-in USB 2.0/3.0 controller and on the usage of the PS GTR lanes are available in the Zynq UltraScale+ Device Technical Reference Manual [27] and in the Zynq UltraScale+ MPSoC Data Sheet: Overview [32].

Figure 14 shows an example of a USB 3.0 implementation using the built-in AMD USB 3.0 interface and the USB 2.0 signals from the PHY, all routed to a USB 3.0 connector on the base board.

> **Tip**
>
> The USB 3.0 interface on the Mercury XU5 SoC module uses the GTR signal lines (MGTPS signals on module connector B), and not the USB_SSRX_P/N and USB_SSTX_P/N signal lines on module connector A.

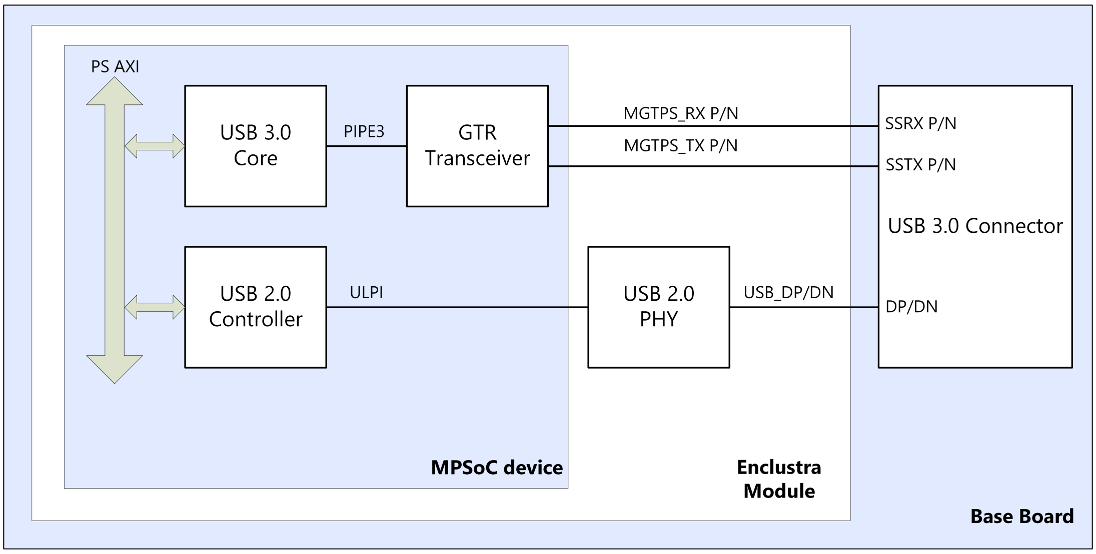

Figure 14: USB 3.0 Implementation Example

3.23 DisplayPort

AMD Zynq UltraScale+ devices feature two built-in DisplayPort controllers and PHYs, supporting up to two lanes at a 5.4 Gbit/s line rate. Each lane is represented by one of the PS GTR transceivers connected to the module connector.

A 27 MHz differential clock is available on the module and connected to PS_MGTREFCLK3 pins, to be used as a reference clock for the DisplayPort interface. It is also possible to provide another reference clock from the base board to the MGTPS_REFCLK* pins.

Details on the built-in DisplayPort controller and on the usage of the PS GTR lanes is available in the Zynq UltraScale+ Device Technical Reference Manual [27] and in the Zynq UltraScale+ MPSoC Data Sheet: Overview [32].

3.24 Real-Time Clock (RTC)

Zynq UltraScale+ devices include an internal real-time clock. The internal RTC can be accessed by the platform management unit (PMU). More information on the PMU is available in the Zynq UltraScale+ Device Technical Reference Manual [27].

The RTC crystal pad input and crystal pad output are connected on the Mercury XU5 SoC module to a 32.768 kHz oscillator.

A 1.2 V LDO is used to generate the battery voltage for the built-in RTC (supplied to VCC_PSBATT pin), based on the VCC_BAT voltage mapped to the module connector. This pin can be connected directly to a 3 V battery on the base board. Refer to the Mercury Mars Module Pin Connection Guidelines [11] for details.

3.25 Module Information

The module information is stored on a persistent storage element. It contains the module type and serial number, as well as the Ethernet MAC address and other information. It is connected to the Management (MGMT) I2C bus. Refer to Section 5 for more information on the I2C communication.

3.25.1 Persistent Storage Element Characteristics

Table 37 describes the persistent storage element device assembled on the Mercury XU5 SoC module.

Part Number	Manufacturer	Assembly Variant
ATSHA204A-MAHDA-T	Atmel	Default
DS28CN01	Maxim	Custom

Table 37: Persistent Storage Element Characteristics

An example demonstrating how to read data from the persistent storage element is included in the Mercury XU5 SoC Module Reference Design [2].

4 Device Configuration

4.1 JTAG

The Zynq UltraScale+ devices include two separate JTAG controllers: the Zynq UltraScale+ TAP and the ARM DAP. The first one uses the PS dedicated JTAG pins and has access to both PS and PL and the second one uses the PS PJTAG pins and is used for loading programs, system test, and PS debug.

Details on JTAG and on system test and debug are available in the Zynq UltraScale+ Device Technical Reference Manual [27].

Certain AMD tool versions support QSPI flash programming via JTAG only when JTAG boot mode is used (unavailable on the Mercury XU5 SoC module). Alternatively, the QSPI flash can be programmed in u-boot or Linux by the SPI controller in the PS or from an SPI external master.

4.1.1 JTAG on Module Connector

The PL and the PS JTAG interfaces are connected into one single chain available on the module connector. The PS_JTAG pins are used by the Zynq UltraScale+ TAP controller. The controller has full functionality only after the PS boot is complete. In order to enable the ARM DAP controller, special commands must be sent to the Zynq UltraScale+ TAP.

The MPSoC device and the flash devices can be configured via JTAG from AMD Vivado Hardware Manager or AMD Vitis. For this operation, the ARM DAP must be enabled.

Signal Name	Module Connector Pin	PS Dedicated Pin	Comment
JTAG_TCK	A-123	PS_JTAG_TCK	10 kΩ pull-up to VCC_CFG_MIO
JTAG_TMS	A-119	PS_JTAG_TMS	10 kΩ pull-up to VCC_CFG_MIO
JTAG_TDI	A-117	PS_JTAG_TDI	10 kΩ pull-up to VCC_CFG_MIO
JTAG_TDO	A-121	PS_JTAG_TDO	10 kΩ pull-up to VCC_CFG_MIO

Table 38: JTAG Interface - PL and PS Access and Debug

4.1.2 External Connectivity

The JTAG signals can be connected to a JTAG connector on the base board. No pull-up/pull-down resistors are necessary. The VREF pin of the programmer must be connected to VCC_CFG_MIO.

It is recommended to add series termination resistors between the module and the JTAG header, close to the source. Enclustra also recommends adding a transient-voltage-suppression diode close to the JTAG connector to protect the MPSoC from damage due to ESD (Electrostatic Discharge). Refer to the Mercury Mars Module Pin Connection Guidelines [11] for details on JTAG interface.

4.2 Configuration Signals

The PS of the MPSoC needs to be configured before the PL can be used. AMD Zynq devices need special boot images to boot from QSPI flash, eMMC flash or SD card. For more information, refer to the Zynq UltraScale+ Device Technical Reference Manual [27].

Table 39 describes the most important configuration pins and their location on the module connector. These signals allow the MPSoC to boot from QSPI flash, eMMC flash or SD card, and can be used to program the QSPI flash from an external master. Refer to Section 4.6.3 for details.

Signal Name	MPSoC Pin Name	Mod. Conn. Pin	Description	Comment
PS_DONE	PS_DONE	A-130	MPSoC device configuration done	1 kΩ pull-up to VCC_CFG_MIO
PS_POR#	PS_POR_B	A-132	MPSoC power-on reset	10 kΩ pull-up to VCC_CFG_MIO
PS_SRST#	PS_SRST_B	A-124	MPSoC system reset	10 kΩ pull-up to VCC_CFG_MIO
BOOT_MODE0	–	A-126	Boot mode selection	10 kΩ pull-up to VCC_CFG_MIO
BOOT_MODE1	–	A-112	Boot mode selection	10 kΩ pull-up to VCC_CFG_MIO

Table 39: MPSoC Configuration Pins

NOTICE

Damage to the device

- Only allow the signals PS_POR# and PS_SRST# to be driven low.
- Do not drive PS_POR# or PS_SRST# to a logic high level.
- Do not drive onto the PS_DONE pin on the base board.

4.3 Pull-Up During Configuration

The Pull-Up During Configuration signal (PUDC) is pulled to ground on the module. As PUDC is an active-low signal, all FPGA I/Os will have the internal pull-up resistors enabled during device configuration.

If the application requires the pull-up during configuration to be disabled, this can be achieved by removing R212 component and by mounting R211. In this configuration the PUDC pin is connected to 1.8 V.

Figure 15 illustrates the configuration of the I/O signals during power-up. Figure 16 indicates the location of the pull-up/pull-down resistors on the module PCB (middle right part on the bottom view drawing).

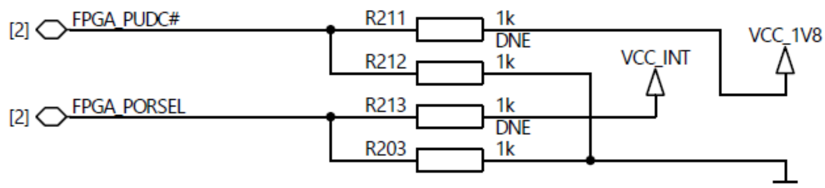

Figure 15: Pull-Up During Configuration (PUDC) and Power-on Reset Delay Override (PORSEL)

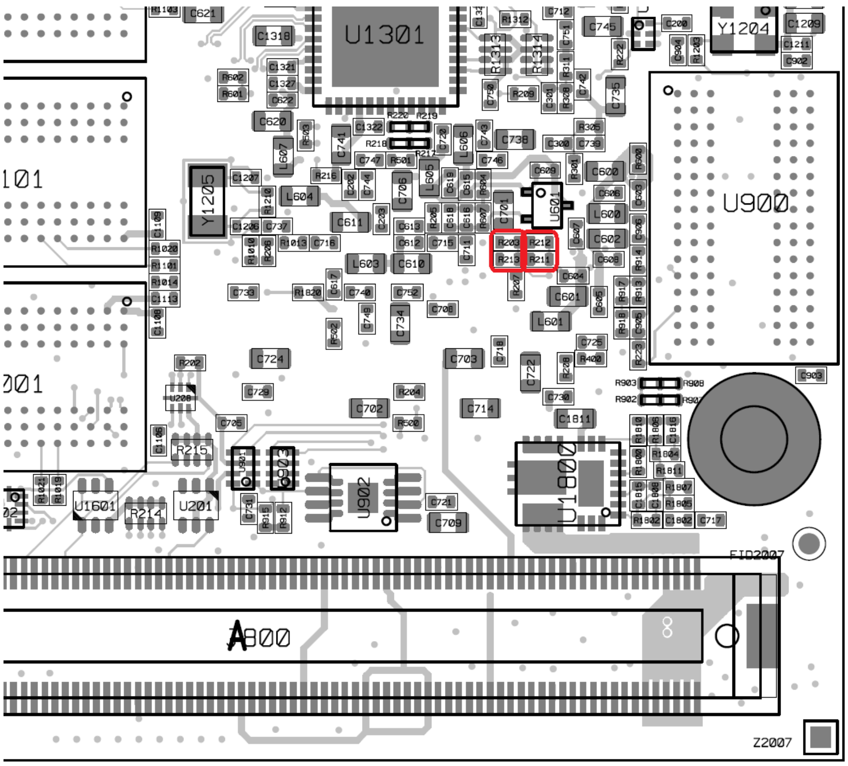

Figure 16: Pull-Up During Configuration (PUDC) and Power-on Reset Delay Override (PORSEL) Resistors

For details on the PUDC signal, refer to the Zynq UltraScale+ Device Technical Reference Manual [27].

4.4 Power-on Reset Delay Override

The power-on reset delay override MPSoC signal (POR_OVERRIDE) is pulled to ground on the module, setting the PL power-on delay time to the default standard time.

If the application requires faster PL power-on delay time, this can be achieved by removing R203 component and by mounting R213.

Figure 15 illustrates the configuration of the POR_OVERRIDE signal. Figure 16 indicates the location of the pull-up/pull-down resistors on the module PCB (middle right part on the bottom view drawing).

For details on the POR_OVERRIDE signal, refer to the Zynq UltraScale+ Device Technical Reference Manual [27].

4.5 Boot Mode

4.5.1 Boot Mode Selection

The boot mode can be selected via two signals available on the module connector.

Table 40 describes the available boot modes on the Mercury XU5 SoC module.

BOOT MODE1	BOOT MODE0	Mode Straps [3:0]	Description	Comment
0	0	0110	Boot from eMMC flash	–
0	1	1110	Boot from SD card (with an external SD 3.0 compliant level shifter; only available when VCC_CFG_MIO is 1.8 V)	Not supported (may be supported in the future)
1	0	0010	Boot from QSPI flash	–
1	1	0101	Boot from SD card (default mode)	–

Table 40: Boot Modes

4.5.2 eMMC Boot Mode

In the eMMC boot mode, the PS boots from the eMMC flash located on the module. The flash device is connected to the PS MIO pins 13 to 22 for 8-bit data transfer mode.

4.5.3 QSPI Boot Mode

In the QSPI boot mode, the PS boots from the QSPI flash located on the module. The flash device is connected to the PS MIO pins 0 to 5.

4.5.4 SD Card Boot Mode

In the SD card boot mode the PS boots from the SD card located on the base board. There are two SD card boot modes available on the Mercury XU5 SoC module. Note that the SD boot mode with level shifter is currently not supported.

The SD boot mode with level shifter is used with Ultra High Speed (UHS) SD cards. The controller will start the communication at 3.3 V and afterwards it will command the card to drop from 3.3 V operation to 1.8 V operation. For this mode, an external SD 3.0 compliant level shifter is required. This boot mode may be supported in the future by Enclustra modules and base boards.

Two SD card boot modes are available on the Mercury XU5 SoC module, as described in Table 40.

For the SD card boot mode, the following requirements must be met:

- The SD card must be connected to MIO pins 45 to 51.
- A Zynq boot image must be generated from an MPSoC design having the SDIO controller enabled.
- The boot image must be named "boot.bin" and then copied to the SD card.
- The SDIO controller must be fed with a reasonable clock frequency. Refer to the reference design for guidelines on SDIO settings.

For details on SD card boot, refer to the Zynq UltraScale+ Device Technical Reference Manual [27].

4.6 Flash Programming

4.6.1 eMMC Flash Programming

The eMMC flash can be formatted and/or programmed in u-boot or Linux, like a regular SD card. The boot image or independent partition files can be transmitted via Ethernet or copied from another storage device.

Certain AMD tool versions support eMMC flash programming via JTAG.

4.6.2 QSPI Flash Programming via JTAG

The AMD Vivado and Vitis software offer QSPI flash programming support via JTAG.

Certain AMD tools versions support QSPI flash programming via JTAG only when JTAG boot mode is used (unavailable on the Mercury XU5 SoC module). For more information, refer to the AMD documentation [27] and support. Alternatively, the QSPI flash can be programmed in u-boot or Linux by the SPI controller in the PS or from an SPI external master.

4.6.3 QSPI Flash Programming from an External SPI Master

The signals of the QSPI flash are directly connected to the module connector for flash access. As the flash signals are connected to the MPSoC device as well, the MPSoC device pins must be tri-stated while accessing the QSPI flash directly from an external device. This is ensured by pulling the PS_SRST# signal to ground followed by a pulse on PS_POR#, which puts the MPSoC device into reset state and tri-states all I/O pins. PS_SRST# must be low when PS_POR# is released and kept low until the flash programming has finished. Afterwards, all SPI signals and PS_SRST# must be tri-stated and another reset impulse must be applied to PS_POR#.

Signal Name	MPSoC Pin	Mod. Conn. Pin	Description	Comment
FLASH_CLK	MIO0	A-118	SPI CLK	10 kΩ pull-up to VCC_CFG_MIO
FLASH_DO	MIO1	A-122	SPI MISO	10 kΩ pull-up to VCC_CFG_MIO
FLASH_DI	MIO4	A-114	SPI MOSI	10 kΩ pull-up to VCC_CFG_MIO
FLASH_CS#	MIO5	A-116	SPI CS#	10 kΩ pull-up to VCC_CFG_MIO

Table 41: QSPI Flash Signals for External Access

Figure 17 shows the signal diagrams corresponding to flash programming from an external master.

In addition, a non-QSPI boot mode must be used during QSPI flash programming, otherwise the MPSoC device will attempt to boot from the flash and will disturb the clock.

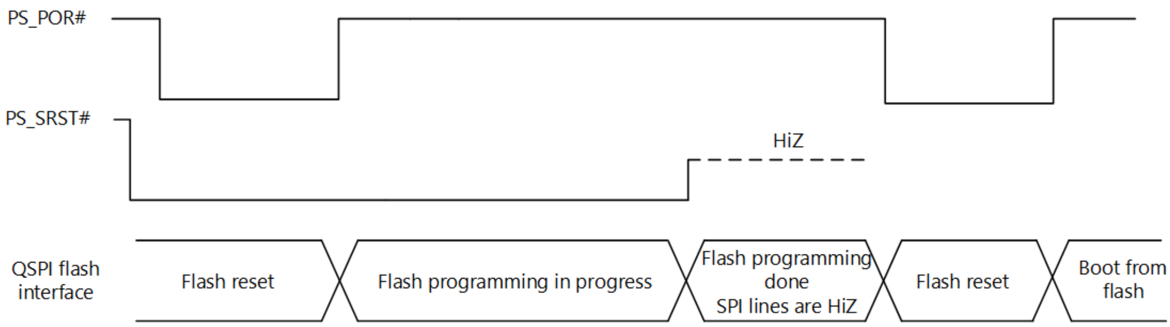

Figure 17: QSPI Flash Programming from an External SPI Master, Signal Diagrams

NOTICE

Damage to the device

The module can be damaged if the QSPI flash signals are driven simultaneously by the module and the base board.

- While accessing the QSPI flash from the module connector, put the MPSoC device into reset and select a non-QSPI boot mode.

4.7 Enclustra Module Configuration Tool

In combination with an Enclustra base board, the QSPI flash can be programmed using Enclustra Module Configuration Tool (MCT) [21]. For this method, a non-QSPI boot mode must be used during QSPI flash programming. The entire procedure is described in the reference design documentation.

The AMD Zynq devices do not support slave serial configuration, therefore only flash programming is supported by the Enclustra MCT for the Mercury XU5 SoC module.

5 I2C Communication

5.1 Overview

The I2C bus on the Mercury XU5 SoC module is connected to the MPSoC device and to the persistent storage element, and is available on the module connector. This allows external devices to read the module type and to connect more devices to the I2C bus.

The I2C clock frequency should not exceed 400 kHz.

> **Tip**
>
> Maximum I2C speed may be limited by the routing path and additional loads on the base board.

> **Tip**
>
> If the I2C traces on the base board are very long, 100 Ω series resistors should be added between the module and the I2C device on the base board.

5.2 Signal Description

Table 42 describes the signals of the I2C interface. The pins are connected to both PS and PL. All signals have on-board pull-up resistors to VCC_3V3.

All signals must be connected to open collector outputs and must not be driven high from any source. I2C_INT# is an input to the MPSoC and must not be driven from the MPSoC device.

Level shifters are used between the I2C bus and the PS/PL pins, to allow I/O voltages lower than 3.3 V. Make sure that all pins are configured correctly and no pull-down resistors are enabled.

Signal Name	MPSoC Pin (PS)	MPSoC Pin (PL)	Connector Pin	Comment
I2C_SDA	MIO11	C12	A-113	2.2 kΩ pull-up to VCC_3V3
I2C_SCL	MIO10	D12	A-111	2.2 kΩ pull-up to VCC_3V3
I2C_INT#	MIO12	–	A-115	4.7 kΩ pull-up to VCC_3V3

Table 42: I2C Signal Description

5.3 I2C Address Map

Table 43 describes the addresses for several devices connected on I2C bus. For details on the characteristics of the persistent storage element, refer to Section 3.25.

Address (7-bit)	Description	Assembly Variant
0x5C	Persistent storage element	Custom
0x64	Persistent storage element	Default

Table 43: I2C Addresses

5.4 Module Information

The module information is stored on the persistent storage element. It includes the module serial number and configuration. An example demonstrating how to read the module information from the persistent storage element memory is included in the Mercury XU5 SoC Module Reference Design [2].

> **Tip**
>
> Any attempt to write data to the persistent storage element causes the warranty to be rendered void.

5.4.1 Memory Map

Address	Length (bits)	Description
0x00	32	Module serial number
0x04	32	Module product information
0x08	40	Module configuration
0x0D	24	Reserved
0x10	48	Ethernet MAC address
0x16	48	Reserved
0x1C	32	Checksum (only for DS28CN01 type)

Table 44: Persistent Storage Element Sector 0 Memory Map

Module Serial Number

The module serial number is a unique 32-bit number that identifies the module. It is stored using big-endian byte order (MSB on the lowest address).

Module Product Information

This field indicates the type of module and hardware revision.

Module	Product Series	Reserved	Revision	Product Information
Mercury XU5 SoC module	0x0333	0x[XX]	0x[YY]	0x0333 [XX][YY]

Table 45: Product Information

Module Configuration

Addr.	Bits	Description	Min. Value	Max. Value	Comment
0x08	7-4	MPSoC type	0	9	See Table 47
	3-0	MPSoC device speed grade	1	3	–
0x09	7-6	Temperature range	0	2	See Table 48
	5	Power grade	0 (Normal)	1 (Low power)	–
	4-3	Gigabit Ethernet port count	0	2	–
	2	RTC equipped	0	1	–
	1	Alternative MGT routing[18]	0	1	–
	0	DDR4 PS ECC enabled[19]	0 (Yes)	1 (No)	–
0x0A	7-3	Reserved	–	–	–
	2	DDR4 PS bandwidth[20]	0 (Full)	1 (Half)	–
	1-0	USB 2.0 port count	0	2	–
0x0B	7-4	DDR4 RAM (PS) size (GB)	0 (0 GB)	4 (8 GB)	Resolution = 1 GB
	3-0	DDR4 RAM (PL) size (MB)	0 (0 MB)	9 (2'048 MB)	Resolution = 8 MB
0x0C	7-4	eMMC flash size (GB)	0 (0 GB)	7 (64 GB)	Resolution = 1 GB
	3-0	QSPI flash memory size (MB)	0 (0 MB)	7 (64 MB)	Resolution = 1 MB

Table 46: Module Configuration

The memory sizes are defined as Resolution$\times 2^{(\text{Value-1})}$, for example:

- DRAM = 0: none
- DRAM = 1: 1 GB
- DRAM = 2: 2 GB
- DRAM = 3: 4 GB

Table 47 shows the available MPSoC device types.

[18] This property indicates that the module uses the alternative "G1" MGT routing, as described in Section 3.8.2. For the "G1" assembly variant, a value of 1 is programmed to the persistent storage element. For the other module variants, a value of 0 is programmed to the persistent storage element.

[19] Property introduced to support the module variants without DDR4 ECC. The new persistent storage element map definition is backward compatible.

[20] This property was introduced to support the module variants equipped with half of the maximum number of DDR4 chips on the PS side. The new persistent storage element map definition is backward compatible.

Value	MPSoC Device Type
0	XCZU2EG
1	XCZU3EG
2	XCZU4EV
3	XCZU5EV
4	XCZU2CG
5	XCZU4CG
6	XCZU2EG 4524
7	XCZU4CG 4524
8	XCZU2CG 4524
9	XCZU5CG

Table 47: MPSoC Device Types

Table 48 shows the available temperature ranges.

Value	Module Temperature Range
0	Commercial
1	Extended
2	Industrial

Table 48: Module Temperature Range

Ethernet MAC Address

The Ethernet MAC address is stored using big-endian byte order (MSB on the lowest address). Each module is assigned two sequential MAC addresses. Only the lower one is stored in the persistent storage element.

6 Operating Conditions

6.1 Absolute Maximum Ratings

Table 49 indicates the absolute maximum ratings for Mercury XU5 SoC module. The values given are for reference only. For details, refer to the Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics [31].

Parameter	Description	Min.	Max.	Unit
VCC_MOD	Supply voltage relative to ground	-0.5	16.0	V
VCC_BAT	Supply voltage for MPSoC battery-backed RAM and battery-backed RTC	0.0	3.6	V
VCC_IO_BN VCC_IO_BO	I/O bank supply voltage relative to ground (V_{CCO})	-0.5	3.4	V
VCC_IO_B65 VCC_IO_B66	I/O bank supply voltage relative to ground (V_{CCO})	-0.5	2.0	V
VCC_CFG_MIO	I/O bank supply voltage relative to ground (V_{CCO_PSIO})	-0.5	3.63	V
IO_B[x]_<...>	I/O signal lines input voltage relative to ground (V_{IN})	-0.5	V_{CCO}+0.5	V
PS_MIO[x]_<...>	PS I/O signal lines input voltage relative to ground (V_{PSIN})	-0.5	V_{CCO_PSIO}+0.5	V

Table 49: Absolute Maximum Ratings

6.2 Recommended Operating Conditions

Table 50 indicates the recommended operating conditions for Mercury XU5 SoC module. The values given are for reference only. For details, refer to the Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics [31].

Parameter	Description	Min.	Typ.	Max.	Unit
VCC_MOD	Supply voltage relative to ground	4.75	5[21] – 15	15.75	V
VCC_BAT	Supply voltage for MPSoC battery-backed RAM and battery-backed RTC	2.7	–	3.6	V
VCC_IO_B[x]	I/O bank supply voltage relative to ground (V_{CCO})	Refer to Section 3.8.5			
VCC_CFG_MIO	I/O bank supply voltage relative to ground (V_{CCO_PSIO})				
IO_B[x]_<...>	I/O signal lines input voltage relative to ground (V_{IN})	-0.2	–	V_{CCO}+0.2	V
PS_MIO[x]_<...>	PS I/O signal lines input voltage relative to ground (V_{PSIN})	-0.5	–	V_{CCO_PSIO}+0.5	V
Power	Maximum module power consumption[22]	–	–	45	W
Temperature[23]	Temperature range for extended temperature modules (E)	0	–	+85	°C
	Temperature range for industrial modules (I)	-40	–	+85	°C

Table 50: Recommended Operating Conditions

NOTICE

Damage to the device due to overheating

Depending on the user application, the Mercury XU5 SoC module may consume more power than can be dissipated without additional cooling measures.

- Ensure that the MPSoC is always adequately cooled by installing a heat sink and/or providing air flow.

[21] Depending on your design and the operating conditions, 5 V might not be sufficient to supply every component/interface.
[22] Sum of all power inputs at maximum rated current
[23] The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.

7 Ordering and Support

7.1 Ordering

Use the Enclustra online request/order form for ordering or requesting information:
http://www.enclustra.com/en/order/

7.2 Support

Follow the instructions on the Enclustra online support site:
http://www.enclustra.com/en/support/

List of Figures

List of Tables

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