TE0821 TRM

Revision v.64

Exported on 2025-06-03

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4 Overview

The Trenz Electronic TE0821 is a powerful 4 x 5 cm MPSoC module integrated with a Xilinx Zynq UltraScale+ MPSoC. In addition, the module is equipped with 2x 1 GB DDR4 SDRAM chip, 4Gb up to 128 Gb eMMC chip, 2x 64 MB flash memory for configuration and data storage, as well as powerful switching power supplies for all required voltages. The module is equipped with a Lattice Mach XO2 CPLD for system controlling. 3x Robust high-speed connectors provide a large number of inputs and outputs.

The highly integrated modules are smaller than a credit card and are offered in several variants at an affordable price-performance ratio. Modules with a 4 x 5 cm form factor are completely mechanically and largely electrically compatible with each other.

All components cover at least the industrial temperature range. The temperature range in which the module can be used depends on the customer design and the selected cooling. Please contact us for special solutions.

Refer to http://trenz.org/te0821-info for the current online version of this manual and other available documentation.

4.1 Key Features

- **SoC/FPGA**
  - Package: SFVC784
  - Device: ZU2 ...ZU5, *
  - Engine: EG, CG, EV, *
  - Speed: -1, -1L, -2, -2L, 3, *, **
  - Temperature: I, E, *, **
- **RAM/Storage**
  - 2x DDR4 SDRAM,
    - Data Width: 16 Bit
    - Size: 8 Gb, *
    - Speed: 2400 Mbps, ***
  - 2x QSPI boot Flash in dual parallel mode
    - Data Width: 8 Bit
    - Size: 512 Mb Gb, *
  - 1x e.MMC Memory
    - Data Width: 16 Bit
    - Size: 8 Gb, *
  - MAC address serial EEPROM
- **On Board**
  - Lattice MachXO2 CPLD
  - Programmable Clock Generator
  - Hi-speed USB2 ULPI Transceiver
  - 4x LEDS
- **Interface**
  - 1 Gbps RGMII Ethernet interface
  - Hi-speed USB2 ULPI transceiver with full OTG support
  - Graphic Processor Mali-400 MP2, *
  - 34 x High Performance (HP) und 96 x High Density PL I/Os
  - 4 x serial PS GTR transceivers
    - PCI Express interface
    - SATA 3.1 interface
    - DisplayPort interface with video resolution up to 4k x 2k
    - 2x USB 3.0 specification compliant interface implementing a 5 Gbit/s line rate
- **Power**
  - All power regulators on board
- **Dimension**

    - 40 x 50 mm
- **Note**
    - * depends on assembly version
    - ** also non low power assembly options possible
    - *** depends on used U+ Zynq and DDR4 combination
    - Rugged for shock and high vibration

4.2 Block Diagram

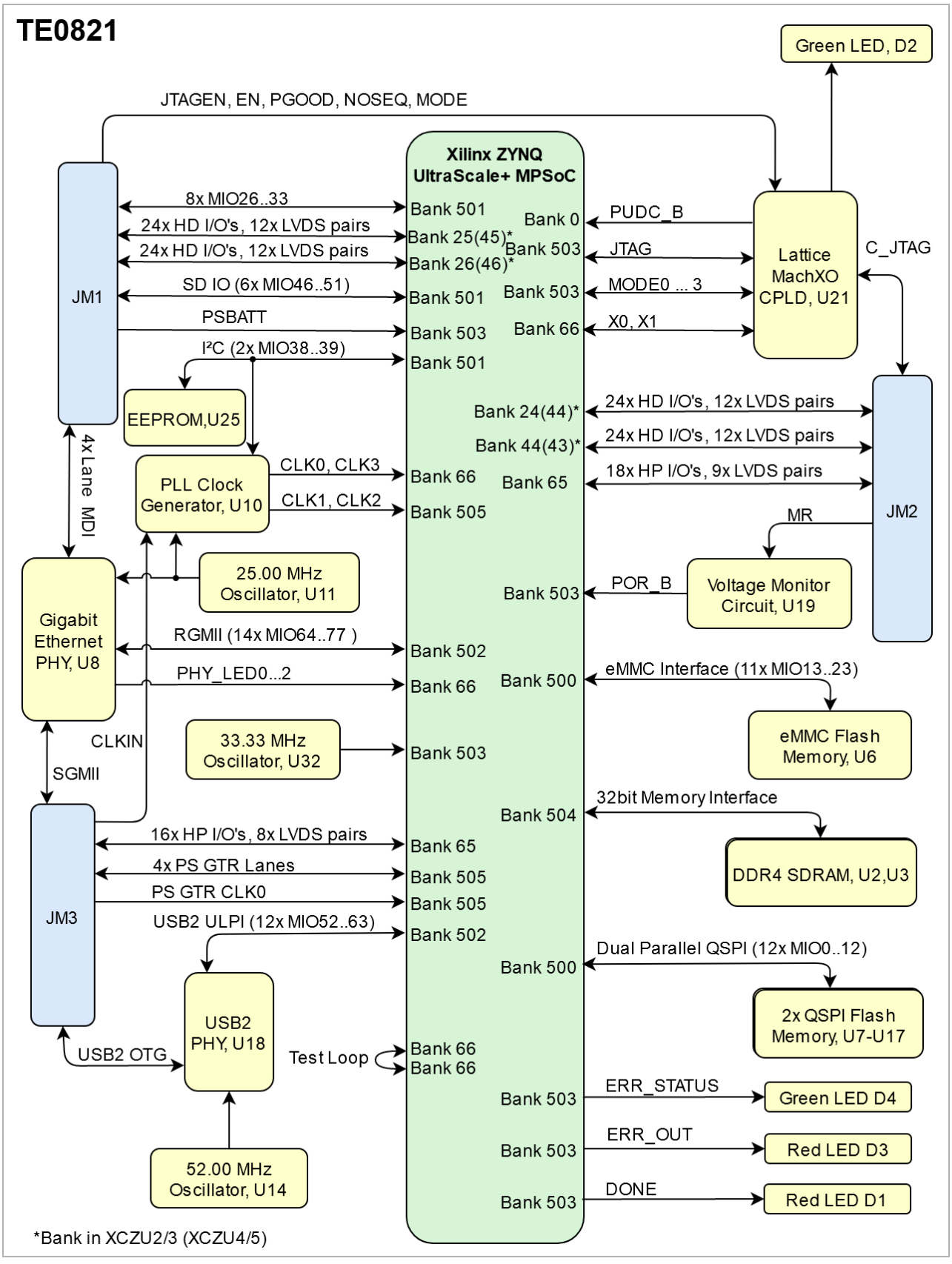

Figure 1: TE0821 block diagram

4.3 Main Components

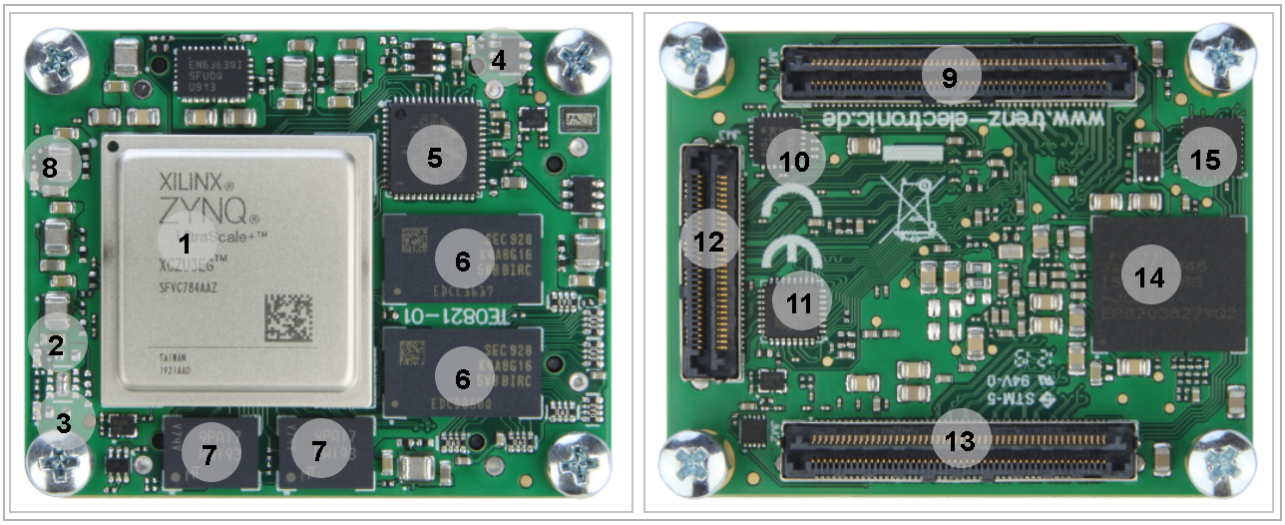

Figure 2: TE0821 main components

1. Xilinx ZYNQ UltraScale+ MPSoC, U1
2. Red LED (ERR_OUT), D3
3. Green LED (ERR_STATUS), D4
4. Red LED (DONE), D1
5. 10/100/1000 Mbps Energy Efficient Ethernet Transceiver, U8
6. 8Gb DDR4, U2-U3
7. 512 Mbit QSPI flash memory, U7-U17
8. Green User LED, D2
9. B2B connector Samtec Razor Beam, JM1
10. Programmable clock generator, U10
11. USB2.0 Transceiver, U18
12. B2B connector Samtec Razor Beam, JM3
13. B2B connector Samtec Razor Beam, JM2
14. 8 GByte eMMC memory, U6
15. Lattice Semiconductor MachXO2 System Controller CPLD, U21

Additional assembly options are available for cost or performance optimization upon request.

4.4 Initial Delivery State

Storage device name	Content	Notes
Dual QSPI Flash Memory	Not programmed	
eMMC Memory	Not programmed	
DDR4 SDRAM	Not programmed	

Storage device name	Content	Notes
Programmable Clock Generator	Not programmed	
CPLD (LCMXO2-256HC)	Programmed	TE0821 CPLD

Table 1: Initial delivery state of programmable devices on the module

4.5 Configuration Signals

Two different firmware versions are available, one with the QSPI boot option and other with the SD Card boot option.

MODE Pin	Boot Mode
High	QSPI*
Low	SD Card*

Table 2: Boot process.
*changable also with other CPLD Firmware: TE0821 CPLD.

Signal	B2B	I/O	Note
EN	JM1-28	Input	CPLD Enable Pin

Table 3: Reset process.

5 Signals, Interfaces and Pins

5.1 Board to Board (B2B) I/Os

FPGA bank number and number of I/O signals connected to the B2B connector:

FPGA Bank	Type	B2B Connector	I/O Signal Count	Voltage Level	Notes
24	HD	JM2	24x I/O, 12x LVDS Pairs	Variable	Max voltage 3.3V
25	HD	JM1	24x I/O, 12x LVDS Pairs	Variable	Max voltage 3.3V
26	HD	JM1	24x I/O, 12x LVDS Pairs	Variable	Max voltage 3.3V
44	HD	JM2	24x I/O, 12x LVDS Pairs	Variable	Max voltage 3.3V
65	HP	JM2	18x I/O, 9x LVDS Pairs	Variable	Max voltage 1.8V
65	HP	JM3	16x I/O, 8x LVDS Pairs	Variable	Max voltage 1.8V
505	GTR	JM3	16x I/O, 8x LVDS Pairs	-	4x lanes
505	GTR CLK	JM3	1x Diff Clock	-	
501	MIO	JM1	15 I/O	3.3V	

Table 4: General PL I/O to B2B connectors information
For detailed information about the pin-out, please refer to the Pin-out table.

5.2 JTAG Interface

JTAG access to the Xilinx Zynq UltraScale+ is applicable by using Lattice MachXO CPLD through B2B connector JM2.

JTAG Signal	B2B Connector	Note
TMS	JM2-93	
TDI	JM2-95	
TDO	JM2-97	
TCK	JM2-99	
JTAGEN	JM1-89	Pulled Low: Xilinx Zynq UltraScale+ MPSoC Pulled High: Lattice MachXO CPLD

Table 5: JTAG pins connection

5.3 MGT Lanes

There are 4x MGT Lanes connected to FPGA Bank 505-GTR. The Xilinx Zynq UltraScale+ device used on the TE0821 module has 4 GTR transceivers. All 4 are wired directly to B2B connector JM3. MGT (Multi Gigabit Transceiver) lane consists of one transmit and one receive (TX/RX) differential pairs, four signals total per one MGT lane. Following table lists lane number, FPGA bank number, transceiver type, signal schematic name, board-to-board pin connection and FPGA pins connection:

Lane	Schematic	B2B	Note
0	• B505_RX0_P • B505_RX0_N • B505_TX0_P • B505_TX0_N	• JM3-26 • JM3-28 • JM3-25 • JM3-27	
1	• B505_RX1_P • B505_RX1_N • B505_TX1_P • B505_TX1_N	• JM3-20 • JM3-22 • JM3-19 • JM3-21	
2	• B505_RX2_P • B505_RX2_N • B505_TX2_P • B505_TX2_N	• JM3-14 • JM3-16 • JM3-13 • JM3-15	
3	• B505_RX2_P • B505_RX2_N • B505_TX2_P • B505_TX2_N	• JM3-8 • JM3-10 • JM3-7 • JM3-9	

Table 6: MGT Lanes connection

5.4 Gigabit Ethernet

On-board Gigabit Ethernet PHY is provided with Marvell Alaska 88E1512 chip. The Ethernet PHY RGMII interface is connected to the Zynq Ethernet0 PS GEM0. I/O voltage is fixed at 1.8V for HSTL signaling. SGMII (SFP copper or fiber) can be used directly with the Ethernet PHY, as the SGMII pins are available on the B2B connector JM3. The reference clock input of the PHY is supplied from an on-board 25MHz oscillator (U11), the 125MHz output clock is left unconnected.

Pin	Schematic	Connected to	Note
MDIP0...3	PHY_MDI0...3	B2B, JM1	
MDC	ETH_MDC	MIO76	
MDIO	ETH_MDIO	MIO77	
S_IN	S_IN	B2B, JM3	
S_OUT	S_OUT	B2B, JM3	
TXD0..3	ETH_TXD0...3	MIO65...68	
TX_CTRL	ETH_TXCTL	MIO69	
TX_CLK	ETH_TXCK	MIO64	
RXD0...3	ETH_RXD0...3	MIO71...74	
RX_CTRL	ETH_RXCTL	MIO75	
RX_CLK	ETH_RXCK	MIO70	
LED0...2	PHY_LED0...2	FPGA Bank 66	
RESETn	ETH_RST	MIO24	

Table 7: GigaBit Ethernet connection

5.5 System Controller CPLD

Special purpose pins are connected to System Controller CPLD and have following default configuration:

Pin Name	Mode	Function	Default Configuration
EN1	Input	Power Enable	No hard wired function on PCB. When forced low, PGOOD goes low without effect on power management
PGOOD	Output	Power Good	Only indirect used for power status, see CPLD description
NOSEQ	-	-	No used for Power sequencing, see CPLD description
RESIN	Input	Reset	Active low reset, gated to POR_B
JTAGEN	Input	JTAG Select	Low for normal operation, high for CPLD JTAG access

Table 8: System Controller CPLD special purpose pins
Please check the entire information at TE0821 CPLD.

5.6 USB Interface

USB PHY is provided by Microchip USB3320. The ULPI interface is connected to the Zynq PS USB0. I/O voltage is fixed at 1.8V. Reference clock input for the USB PHY is supplied by the on-board 52.00 MHz oscillator (U14).

PHY Pin	ZYNQ Pin	B2B Name	Notes
ULPI	MIO52..63	-	Zynq USB0 MIO pins are connected to the USB PHY.
REFCLK	-	-	52.00 MHz from on-board oscillator (U14).
REFSEL[0..2]	-	-	Reference clock frequency select, all set to GND selects 52.00 MHz.
RESETB	MIO25	-	Active low reset.
CLKOUT	MIO52	-	Connected to 1.8V, selects reference clock operation mode.

PHY Pin	ZYNQ Pin	B2B Name	Notes
DP, DM	-	OTG_D_P, OTG_D_N	USB data lines routed to B2B connector JM3 pins 47 and 49.
CPEN	-	VBUS_V_EN	External USB power switch active high enable signal, routed to JM3 pin 17.
VBUS	-	USB_VBUS	Connect to USB VBUS via a series of resistors, see reference schematics, routed to JM3 pin 55.
ID	-	OTG_ID	For an A-device connect to ground, for a B-device left floating. routed from JM3 pin 23.

Table 9: General overview of the USB PHY signals

5.7 I2C Interface

On-board I^2C devices are connected to MIO38 (SCL) and MIO39 (SDA) which are configured as I^2C0 by default. Addresses for on-board I^2C slave devices are listed in the table below:

I2C Device	I2C Address	Notes
Si5338A PLL	0x70	-
EEPROM	0x50	-

Table 10: Address table of the I2C bus slave devices

5.8 MIO Pins

MIO Pin	Connected to	B2B	Notes
0...5	QSPI Flash, U7	-	SPI Flash
7...12	QSPI Flash, U17	-	SPI Flash
13...23	eMMC, U6		

MIO Pin	Connected to	B2B	Notes
24	ETH Transceiver, U8	-	ETH_RST
25	USB2.0 Transceiver, U18	-	OTG_RST
26...33	User MIO	JM1	
34...37	N.C	-	N.C
38...39	EEPROM, U25	-	I2C_SDA/SCL
40...45	N.C		N.C
46...51	SD Card	JM1	
52...63	USB2.0 Transceiver, U18	-	
63...77	Ethernet Transceiver, U8	-	

Table 11: MIOs pins

5.9 Test Points

Test Point	Signal	Connected to	Notes
1	I2C_SCL	EEPROM, U25	
2	I2C_SDA	EEPROM, U25	
3	SRST_B	FPGA Bank 503	PSCONFIG
4	PS_CLK	FPGA Bank 503	PSCONFIG
5	PROG_B	FPGA Bank 503	PSCONFIG
6	INIT_B	FPGA Bank 503	PSCONFIG
7	DONE	Red LED, D1	

Test Point	Signal	Connected to	Notes
8	PS_LP0V85	Voltage Regulator, U12	
9	DDR_2V5	Voltage Regulator, U4	
10	PS_AVCC	Voltage Regulator, U9	
11	DDR_1V2	Voltage Regulator, U15	
12	PS_AVTT	Voltage Regulator, U13	
13	PS_FP0V85	Voltage Regulator, U26	
14	POR_B	Voltage Translator, U19	
15	PS_PLL	Voltage Regulator, U23	
16	PL_VCCINT	Voltage Regulator, U5	

Table 12: Test Points Information

6 On-board Peripherals

Chip/Interface	Designator	Notes
QSPI Flash	U7, U17	
EEPROM	U25	
DDR4 SDRAM	U2,U3	
GigaBit Ethernet	U8	
USB2.0 Transceiver	U18	
eMMC Memory	U6	
Oscillators	U32, U14, U11	
Programmable Clock Generator	U10	
CPLD	U21	
LEDs	D1...3	

Table 13: On board peripherals

6.1 Quad SPI Flash Memory

The TE0821 is equipped with dual Flash Memory, U7, U17. Two quad SPI compatible serial bus flash MT25QU512ABB8E12-0SIT memory chips are provided for FPGA configuration file storage. After configuration completes the remaining free memory can be used for application data storage. All four SPI data lines are connected to the FPGA allowing x1, x2 or x4 data bus widths to be used. The maximum data transfer rate depends on the bus width and clock frequency.

Pin	Schematic		Notes
	U7 Pin	U17 Pin	
nCS	MIO5	MIO7	
CLK	MIO0	MIO12	

Pin	Schematic		Notes
	U7 Pin	U17 Pin	
DI/IO0	MIO4	MIO8	
DO/IO1	MIO1	MIO9	
nHOLD/IO3	MIO3	MIO11	
WP/IO2	MIO2	MIO10	

Table 14: Quad SPI interface MIOs and pins

6.2 EEPROM

There is a 2Kb EEPROM provided on the module TE0821.

MIO Pin	Schematic	U25 Pin	Notes
MIO39	I2C_SDA	SDA	
MIO38	I2C_SCL	SCL	

Table 15: I2C EEPROM interface MIOs and pins

MIO Pin	I2C Address	Designator	Notes
MIO38...39	0x50	U25	

Table 16: I2C address for EEPROM

6.3 LEDs

Designator	Color	Connected to	Active Level	Note
D1	Red	DONE	Low	
D2	Green	USR_LED	High	
D3	Red	ERR_OUT	High	

Designator	Color	Connected to	Active Level	Note
D4	Green	ERR_STATUS	High	

Table 17: On-board LEDs

6.4 DDR4 SDRAM

The TE0821 SoM has dual 8 Gb volatile DDR4 SDRAM IC for storing user application code and data.

- Part number: K4A8G165WB-BIRC
- Supply voltage: 1.2V
- Speed: 2400 Mbps
- Temperature: -40 ~ 95 °C

6.5 System Controller CPLD

The System Controller CPLD (U21) is provided by Lattice Semiconductor LCMXO2-256HC (MachXO2 product family). It is the central system management unit with module specific firmware installed to monitor and control various signals of the FPGA, on-board peripherals, I/O interfaces and module as a whole.

See also TE0821 System Controller CPLD page.

6.6 GigaBit Ethernet

On-board Gigabit Ethernet PHY (U8) is provided with Marvell Alaska 88E1512 IC (U8). The Ethernet PHY RGMII interface is connected to the ZynqMP Ethernet3 PS GEM3. I/O voltage is fixed at 1.8V for HSTL signaling. The reference clock input of the PHY is supplied from an on-board 25.00 MHz oscillator (U11).

Pin	Schematic	Connected to	Note
MDIP0...3	PHY_MDI0...3	B2B, JM1	
MDC	ETH_MDC	MIO76	
MDIO	ETH_MDIO	MIO77	
S_IN	S_IN	B2B, JM3	
S_OUT	S_OUT	B2B, JM3	
TXD0..3	ETH_TXD0...3	MIO65...68	
TX_CTRL	ETH_TXCTL	MIO69	

Pin	Schematic	Connected to	Note
TX_CLK	ETH_TXCK	MIO64	
RXD0...3	ETH_RXD0...3	MIO71...74	
RX_CTRL	ETH_RXCTL	MIO75	
RX_CLK	ETH_RXCK	MIO70	
LED0...2	PHY_LED0...2	FPGA Bank 66	
RESETn	ETH_RST	MIO24	

Table 18: Ethernet PHY to Zynq SoC connections

6.7 USB2.0 Transceiver

Hi-speed USB ULPI PHY (U18) is provided with USB3320 from Microchip. The ULPI interface is connected to the Zynq PS USB0 via MIO52..63, bank 502. The I/O voltage is fixed at 1.8V and PHY reference clock input is supplied from the on-board 52.00 MHz oscillator (U14).

6.8 eMMC Flash Memory

eMMC Flash memory device(U6) is connected to the ZynqMP PS MIO bank 500 pins MIO13..MIO23. eMMC chips IS21ES08G-JCLI (FLASH - NAND Speicher-IC (64 Gb x 1) MMC) is used.

6.9 Clock Sources

Designator	Description	Frequency	Note
U11	MEMS Oscillator	25 MHz	
U14	MEMS Oscillator	52 MHz	
U32	MEMS Oscillator	80 MHz	

Table 19: Osillators

6.10 Programmable Clock Generator

There is a Silicon Labs I^{2}C programmable clock generator Si5338A (U10) chip on the module. It's output frequencies can be programmed using the I^{2}C bus address 0x70 or 0x71. Default address is 0x70, IN4/I2C_LSB pin must be set to high for address 0x71.

A 25.00 MHz oscillator is connected to the pin IN3 and is used to generate the output clocks. The oscillator has its output enable pin permanently connected to 1.8V power rail, thus making output frequency available as soon as 1.8V is present. Three of the Si5338 clock outputs are connected to the FPGA. One is connected to a logic bank and the other two are connected to the GTR banks.

Once running, the frequency and other parameters can be changed by programming the device using the I^{2}C bus connected between the FPGA (master) and clock generator (slave). For this, proper I^{2}C bus logic has to be implemented in FPGA.

U25 Pin	Signal	Connected to	Direction	Note
IN0..1	CLK_IN	JM3	IN	
IN2	CLK_25M	Oscillator, U11	IN	
SCL	I2C_SCL	EEPROM,U25	INOUT	
SDA	I2C_SDA	EEPROM,U25	INOUT	
CLK0	CLK0	JM3	OUT	
CLK1	B505_CLK3	FPGA Bank 505	IN	
CLK2	B505_CLK1	FPGA Bank 505	IN	
CLK3	CLK3_N		IN	

Table 20: Programmable Clock Generator Inputs and Outputs

7 Power and Power-On Sequence

7.1 Power Supply

Power supply with minimum current capability of 3 A for system startup is recommended.

7.2 Power Consumption

Power Input Pin	Typical Current
VIN	TBD*
3.3VIN	TBD*

Table 21: Power Consumption
* TBD - To Be Determined

7.3 Power Distribution Dependencies

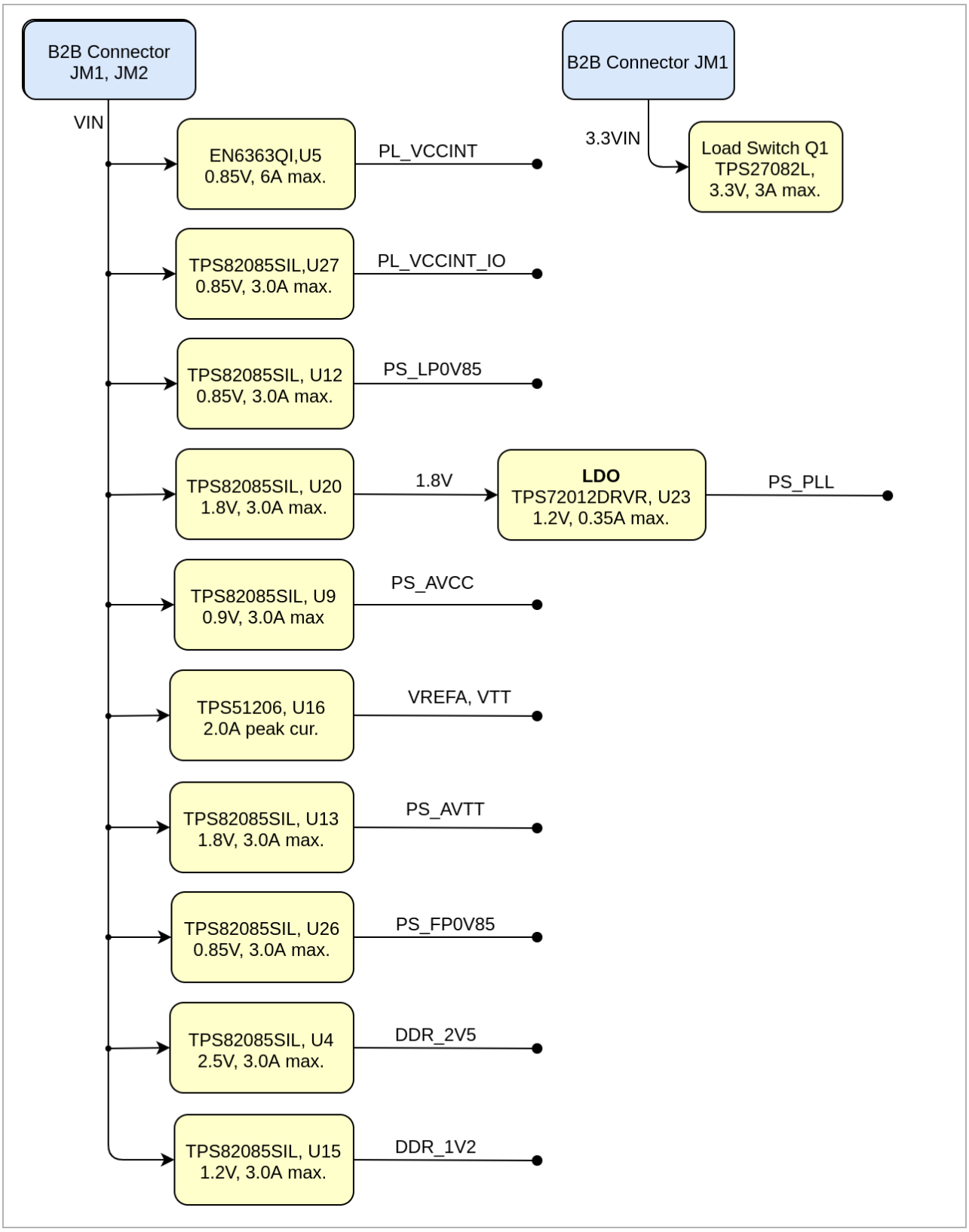

Figure 3: Power Distribution

7.4 Power-On Sequence

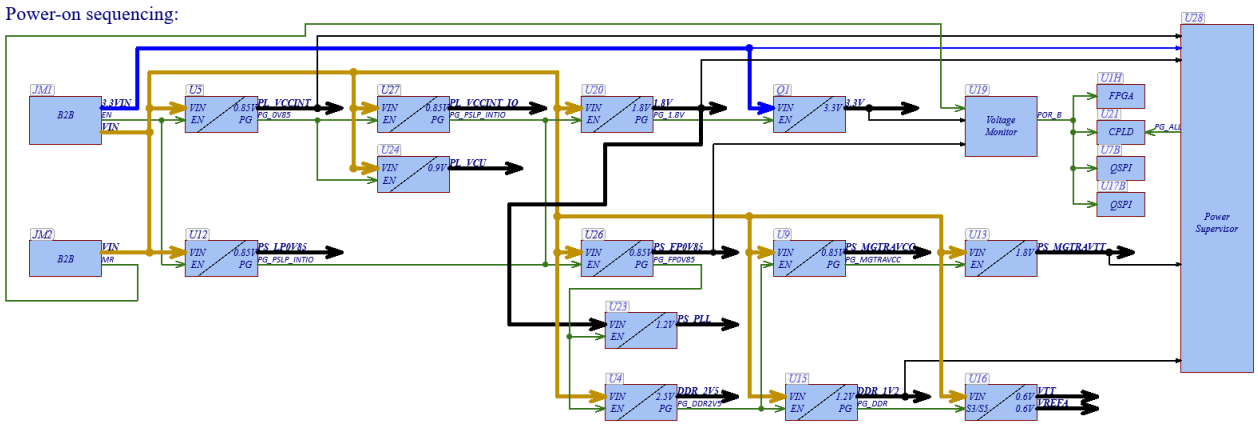

Figure 4: Power Sequency

7.5 Power Rails

Power Rail Name	B2B JM1 Pin	B2B JM2 Pin	B2B JM3 Pin	Direction	Notes
VIN	1, 3, 5	2, 4, 6, 8	-	Input	Supply voltage from the carrier board
3.3V	-	10, 12	-	Output	Internal 3.3V voltage level
VCCO_HD25_26	9,11		-	Input	0 to 3.3V Voltage
3.3VIN	13, 15	-	-	Input	Supply voltage from the carrier board
1.8V	39	-	-	Output	Internal 1.8V voltage level
JTAG VREF	-	91	-	Output	JTAG reference voltage. Attention: Net name on schematic is "3.3VIN"

Power Rail Name	B2B JM1 Pin	B2B JM2 Pin	B2B JM3 Pin	Direction	Notes
VCCO_HD24_44	-	7, 9	-	Input	0 to 3.3V Voltage
VCCO_65	-	5	-	Input	0 to 1.8V Voltage
PSBATT	79	-	-	Input	1.2 to 1.5V Voltage

Table 22: Module power rails.

7.6 Bank Voltages

FPGA Bank	Schematic	Voltage	Note
Bank 24 HD	VCCO_HD24_44	Variable	Max voltage 3.3V
Bank 25 HD	VCCO_HD25_26	Variable	Max voltage 3.3V
Bank 26 HD	VCCO_HD25_26	Variable	Max voltage 3.3V
Bank 44 HD	VCCO_HD24_44	Variable	Max voltage 3.3V
Bank 64 HP	VCCO_64	N.C	Not Connected
Bank 65 HP	VCCO_65	Variable	Max voltage 1.8V
Bank 66 HP	VCCO_66	1.8V	
Bank 500 PSMIO	VCCO_PSIO0_500	1.8V	
Bank 501 PSMIO	VCCO_PSIO1_501	3.3V	

FPGA Bank	Schematic	Voltage	Note
Bank 502 PSMIO	VCCO_PSIO2_502	1.8V	
Bank 503 PSCONFIG	VCCO_PSIO3_503	1.8V	
Bank 504 PSDDR	DDR_1V2	1.2V	

Table 23: Zynq SoC bank voltages.

8 Board to Board Connectors

> These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.

4 x 5 modules use two or three Samtec Razor Beam LSHM connectors on the bottom side.

- 2 x REF-189016-02 (compatible to LSHM-150-04.0-L-DV-A-S-K-TR), (100 pins, "50" per row)
- 1 x REF-189017-02 (compatible to LSHM-130-04.0-L-DV-A-S-K-TR), (60 pins, "30" per row) (depending on module)

8.1 Connector Mating height

When using the same type on baseboard, the mating height is 8mm. Other mating heights are possible by using connectors with a different height

Order number	Connector on baseboard	compatible to	Mating height
23836	REF-189016-01	LSHM-150-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-150-03.0-L-DV-A-S-K-TR	LSHM-150-03.0-L-DV-A-S-K-TR	7.0 mm
23838	REF-189016-02	LSHM-150-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-150-06.0-L-DV-A-S-K-TR	LSHM-150-06.0-L-DV-A-S-K-TR	10.0mm
26125	REF-189017-01	LSHM-130-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-130-03.0-L-DV-A-S-K-TR	LSHM-130-03.0-L-DV-A-S-K-TR	7.0 mm
24903	REF-189017-02	LSHM-130-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-130-06.0-L-DV-A-S-K-TR	LSHM-130-06.0-L-DV-A-S-K-TR	10.0mm

Table 24: Connectors.

The module can be manufactured using other connectors upon request.

8.2 Connector Speed Ratings

The LSHM connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
12 mm, Single-Ended	7.5 GHz / 15 Gbps
12 mm, Differential	6.5 GHz / 13 Gbps
5 mm, Single-Ended	11.5 GHz / 23 Gbps
5 mm, Differential	7.0 GHz / 14 Gbps

Table 25: Speed rating.

8.3 Current Rating

Current rating of Samtec Razor Beam™ LSHM B2B connectors is 2.0A per pin (2 adjacent pins powered).

8.4 Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

9 Technical Specifications

9.1 Absolute Maximum Ratings

Description	Min	Max	Unit	Notes
VIN supply voltage	-0.3	7	V	See EN6347QI and TPS82085SIL datasheets
3.3VIN supply voltage	-0.1	3.630	V	Xilinx DS925 and TPS27082L datasheet
PS I/O supply voltage, VCCO_PSIO	-0.5	3.630	V	Xilinx document DS925
PS I/O input voltage	-0.5	VCCO_PSIO + 0.55	V	Xilinx document DS925
HP I/O bank supply voltage, VCCO	-0.5	2.0	V	Xilinx document DS925
HP I/O bank input voltage	-0.55	VCCO + 0.55	V	Xilinx document DS925
HD I/O bank supply voltage, VCCO	-0.5	3.4	V	Xilinx document DS925
HD I/O bank input voltage	-0.55	VCCO + 0.55	V	Xilinx document DS925
PS GTR reference clocks absolute input voltage	-0.5	1.1	V	Xilinx document DS925
PS GTR absolute input voltage	-0.5	1.1	V	Xilinx document DS925
Voltage on SC CPLD pins	-0.5	3.75	V	Lattice Semiconductor MachXO2 datasheet

Description	Min	Max	Unit	Notes
Storage temperature	-40	+85	°C	See eMMC datasheet

Table 26: PS absolute maximum ratings

9.2 Recommended Operating Conditions

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

Parameter	Min	Max	Units	Reference Document
VIN supply voltage	3.3	6	V	See TPS82085S datasheet
3.3VIN supply voltage	3.3	3.465	V	See LCMXO2-256HC, Xilinx DS925 datasheet
PS I/O supply voltage, VCCO_PSIO	1.710	3.465	V	Xilinx document DS925
PS I/O input voltage	–0.20	VCCO_PSIO + 0.20	V	Xilinx document DS925
HP I/O banks supply voltage, VCCO	0.950	1.9	V	Xilinx document DS925
HP I/O banks input voltage	-0.20	VCCO + 0.20	V	Xilinx document DS925
HD I/O banks supply voltage, VCCO	1.14	3.4	V	Xilinx document DS925
HD I/O banks input voltage	-0.20	VCCO + 0.20	V	Xilinx document DS925
Voltage on SC CPLD pins	-0.3	3.6	V	Lattice Semiconductor MachXO2 datasheet
Operating Temperature Range	0	85	°C	Xilinx document DS925, extended grade Zynq temperarure range

Table 27: Recommended operating conditions.

9.3 Physical Dimensions

- Module size: 40 mm × 50 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 8 mm.

PCB thickness: 1.74 mm.

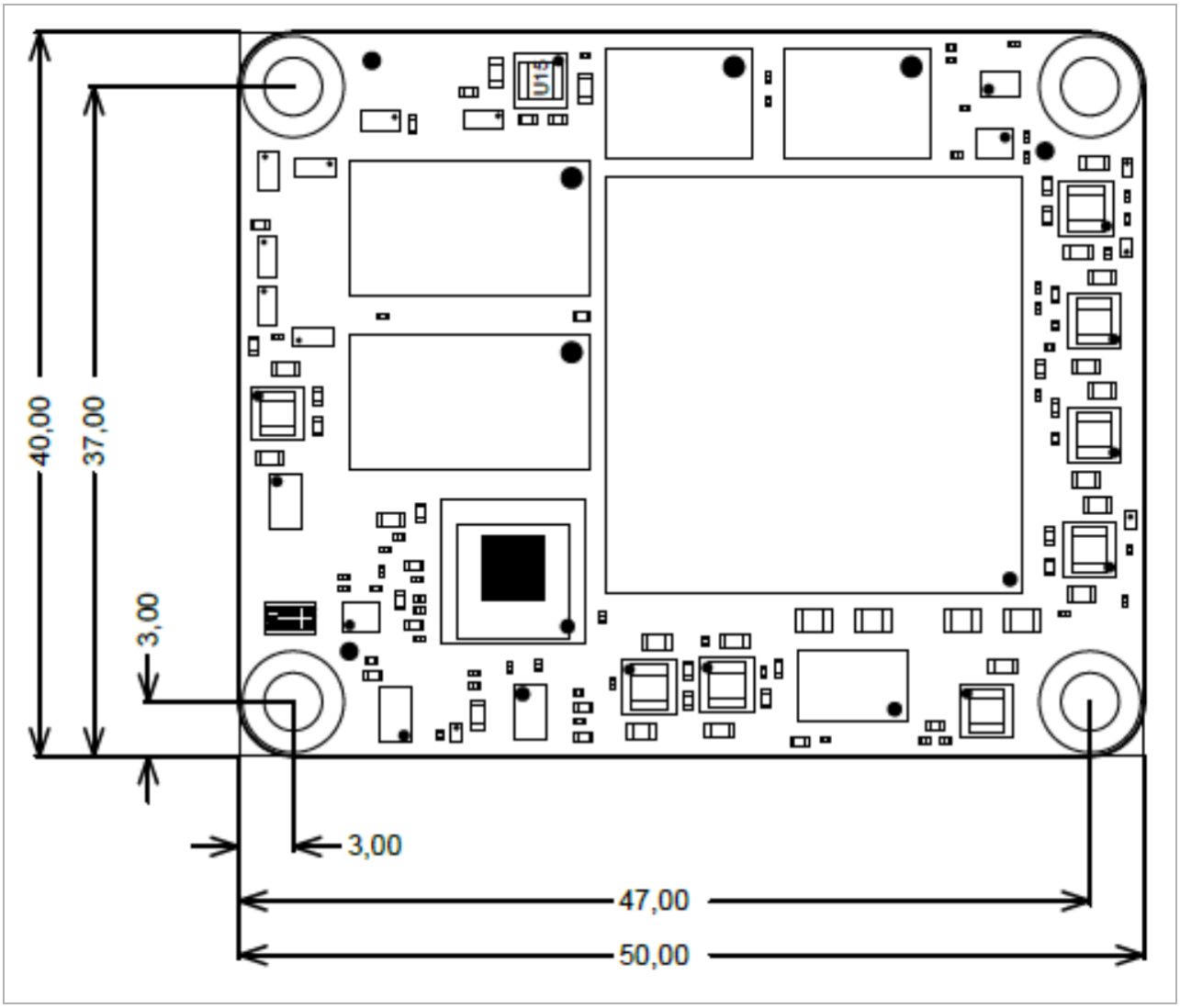

Figure 5: Physical Dimension

10 Currently Offered Variants

Trenz shop TE0821 overview page	
English page	German page

Table 28: Trenz Electronic Shop Overview

11 Revision History

11.1 Hardware Revision History

Date	Revision	Changes	Documentation Link
2019-04-26	REV01	• Initial Release	REV01

Table 29: Hardware Revision History
Hardware revision number can be found on the PCB board together with the module model number separated by the dash.

Figure 6: Board hardware revision number.

11.2 Document Change History

Date	Revision	Contributor	Description
2025-01-29	v.64	Martin Rohrmüller	• Corrected IO number in key features
12 Aug 2021	v.63	Martin Rohrmüller	• bugfix boot mode
2021-07-05	v.61	John Hartfiel	• Update download Link • Update Change history

Date	Revision	Contributor	Description
2021-06-07	v.59	Vadim Yunitski	• Added missing text in Bank Voltages • Fixed typo in Bank Voltages
2020-07-15	v.50	Pedram Babakhani	• Initial Release
--	all	Maksim Tserabei , Pedram Babakhani , John Hartfiel , Martin Rohrmüller , Vadim Yunitski	• --

Table 30: Document change history.

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2019-06-07