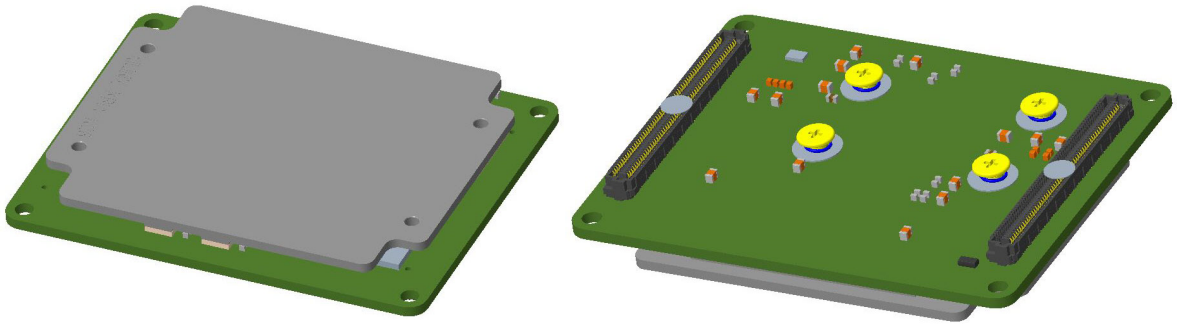
Overview

Module Description

The Xilinx® Kria™ K26 system-on-module (SOM) is a compact embedded platform that integrates a custom-built Zynq® UltraScale+™ MPSoC that runs optimally (and exclusively) on the K26 SOM with DDR memory, nonvolatile storage devices, a security module, and an aluminum thermal heat spreader. The SOM is designed to be plugged into a carrier card with solution-specific peripherals. Key target applications include smart city, machine vision, industrial robotics, and AI/ML computing. The following figure shows the top-side and bottom-side connector view.

Figure 1: **K26 SOM**



X25044-013121

Ordering Information

Table 1: **Ordering Information**

Part Number	Device	Temperature Grade	Encryption	Description
SM-K26-XCL2GC	XCK26-C	Commercial	Enabled	K26C SOM
SM-K26-XCL2GC-ED	XCK26-C	Commercial	Disabled	K26C SOM with encryption disabled
SM-K26-XCL2GI	XCK26-I	Industrial	Enabled	K26I SOM
SM-K26-XCL2GI-ED	XCK26-I	Industrial	Disabled	K26I SOM with encryption disabled

Functional Overview and Block Diagram

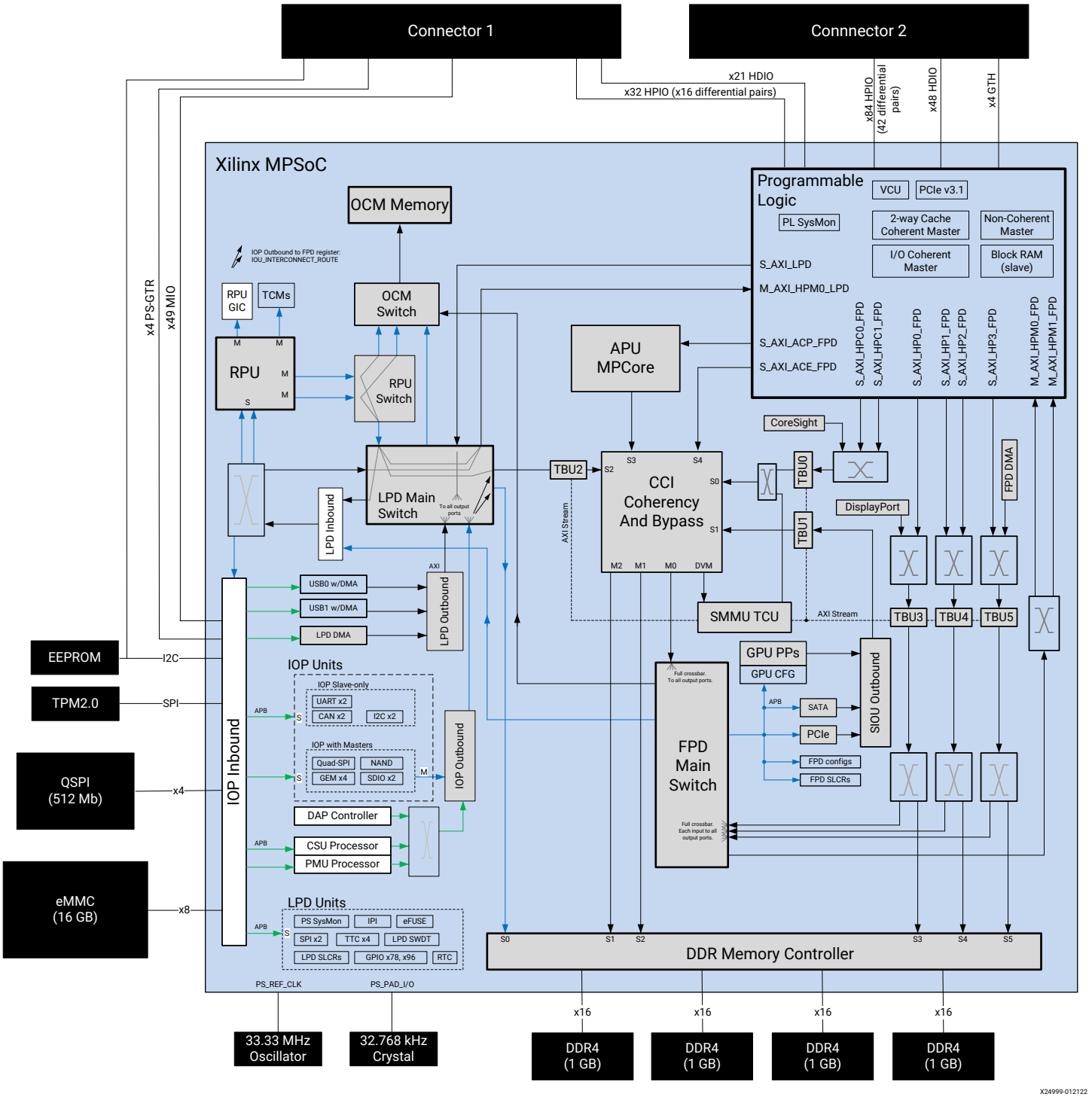
The K26 SOM leverages the XCK26-SFVC784-2LV-C/I, a custom-built Zynq UltraScale+ MPSoC that runs optimally (and exclusively) on the SOM. It provides an embedded processing system (PS) with tightly integrated programmable logic and a rich set of configurable I/O capabilities. The SOM hardware features include:

- Zynq UltraScale+ MPSoC (XCK26 in commercial (C) grade or industrial (I) grade)
- 4 GB 64-bit wide, 2400 Mb/s memory
- Integrated non-volatile memory devices
  - 512 Mb QSPI
  - 16 GB eMMC
  - 64 Kb EEPROM
- TPM2.0 security module
- Two 240-pin connectors with access to user-configurable I/O:
  - PS MIO
  - PS-GTR transceivers
  - PS I2C platform control bus
  - PL HPIO
  - PL HDIO
  - PL GTH transceivers
  - Sideband platform signals
  - Power and power sequencing signals
- Integrated and flexible power design
  - SOC power supplies derived from a single +5V input
  - PL I/O supplies customized through carrier card defined power rails
- Compact mechanical size with integrated thermal heat spreader

The following sections provide a more detailed description of:

- Functional interfaces and input/output
- MPSoC processing system (PS)
- MPSoC programmable logic (PL)
- Boot sources and storage devices
- Security features and module

Figure 2: **K26 SOM Block Diagram**



Functional Interfaces

The K26 SOM provides a combination of fixed and user-defined functional interfaces. Each interface is implemented with one of the major systems within the MPSoC. The following table is a summary of the interfaces, and system association (PS or PL), with a description of their use.

Table 2: **Interfaces Summary**

Interface	Physical Location	Linked Subsystem	Functional Description
QSPI	MIO bank 500 MIO[5:0]	PS	SOM QSPI memory
SD	MIO bank 500 MIO[23:13]	PS	SOM eMMC memory, MIO[22:13] = eMMC, MIO[23] = eMMC reset
I2C	MIO bank 500 MIO[25:24]	PS	SOM power management, EEPROM, and carrier card extensible I2C bus
SPI	MIO bank 500 MIO[11:9], MIO[6]	PS	Isolated SPI interface for TPM 2.0 security module
Power management	MIO bank 501 MIO[34:32]	PS	Fixed PMU SOM based power management
Power management	MIO bank 501 MIO[31]. MIO[35]	PS	MIO35_WD_OUT and MIO31_SHUTDOWN: Optional power management control signals for use by CC designer
MIO – user defined I/O	MIO bank 501 MIO[30:26], MIO[51:38]	PS	19 user-defined multiplexed CPU connected I/O pins
MIO – user defined I/O	MIO Bank 502 MIO[77:52]	PS	26 user-defined multiplexed CPU connected I/O pins
DDR memory controller	MIO bank 504	PS	SOM DDR4 memory
HDA	HDIO bank 45	PL	21 user-defined high-density input/output pins
HDB	HDIO bank 43	PL	24 user-defined high-density input/output pins
HDC	HDIO bank 44	PL	24 user-defined high-density input/output pins
HPA	HPIO bank 66	PL	16 user-defined high-performance input/output differential pin pairs
HPB	HPIO bank 65	PL	21 user-defined high-performance input/output differential pin pairs
HPC	HPIO bank 64	PL	21 user-defined high-performance input/output differential pin pairs
PS-GTR transceivers	PS GTR 505	PS	Four lanes of user-defined high-speed serial transceivers
GTH transceivers	GTH Quad	PL	Four lanes of user-defined high-speed serial transceivers

The K26 SOM provides a large number of flexible user-defined I/O that can be configured for various I/O standards and voltage levels. Voltage levels for each HDIO and HPIO bank can be customized by the SOM carrier card to provide the application-required voltage rails to the corresponding I/O banks. See the Supported I/O Standards section for the I/O voltage rail pin definitions and corresponding decoupling requirements.

The K26 SOM provides PS-GTR and GTH transceivers to implement various high-speed protocols. The supported protocols are listed in the protocol tables of the *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925), and are described in the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) and *Zynq UltraScale+ MPSoC: Software Developers Guide* (UG1137). The transceivers are configured via the Vivado® Design Suite.

Processing System

This section outlines the processing system (PS) resources. It includes:

- **APU:** Arm® Cortex®-A53 based application processing unit (APU) consisting of quad-core Cortex-A53 processors with an F_{MAX} = 1333 MHz, L2 cache, SIMD, VFP4 floating point, and cryptography extensions.
- **RPU:** Arm Cortex-R5F based real-time processing unit (RPU) consisting of dual-core Cortex-R5F processors with floating point unit support with an F_{MAX} = 533 MHz, able to operate in stand-alone and lock-step functions.
- **PMU:** Platform management unit for dedicated SOM power and subsystem management functions.
- **Dynamic memory controller (DDRC):** DDR4 memory controller with configurable quality-of-service configuration capabilities.
- **GPU:** Arm Mali™-400 MP2 based graphics processing unit with an F_{MAX} = 600 MHz.
- **System Monitor:** Built-in analog-digital-converter (ADC) with threshold checks for monitoring and reporting power supply and temperature conditions.
- **RTC:** Real-time clock for maintaining an accurate time base with optional battery backup through a carrier card pin.

The PS provides access to a number of integrated peripherals through multiplexed input/output (MIO) banks. The MPSoC has a total of three MIO banks. The SOM uses the first bank for the on-board peripherals, while the other two MIO banks are customizable and available through the SOM connector interface. All three MIO banks are powered by the SOM with a 1.8V power rail.

Refer to the *MIO Interfaces* table in the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) for more information on MIO usage for Zynq UltraScale+ MPSoCs. MIO mapping must comply with the Zynq UltraScale+ MPSoC design constraints and requirements.

MIO Banks

For MIO assignment, refer to the *MIO Table at a Glance* in *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) for complete constraints.

Table 3: **MIO Banks**

MIO Banks													
Bank 500	0	1	2	3	4	5	6	7	8	9	10	11	12
	QSPI						SPI1	GPIO0		SPI1			GPIO0[1.a]
	sclk_out	miso_mo1	mo2	mo3	mosi_mi0	n_ss_out	sclk_out	LED_DS35	LED_DS36	n_ss_out	miso	mosi	FW_UEn
	13	14	15	16	17	18	19	20	21	22	23	24	25
	eMMC (SD0)										GPIO0	I2C1	
	data[0]	data[1]	data[2]	data[3]	data[4]	data[5]	data[6]	data[7]	cmd_out	clk_out	eMMC_Rst	scl	sda
Bank 501	26	27	28	29	30	31	32	33	34	35	36	37	38
	User Defined					PMU_GPI[1.b]	PMU_GPO[2]	PMU_GPO[2]	PMU_GPO[2]	PMU_GPO[1.c]	UART1[1.d]		User Defined
						SHUTDOWN	FPD_Pwr_En	PL_Pwr_EN	PS_Pwr_En	WD_OUT	txd	rxd	
	39	40	41	42	43	44	45	46	47	48	49	50	51
	User Defined												

Table 3: **MIO Banks** *(cont'd)*

MIO Banks													
Bank 502	52	53	54	55	56	57	58	59	60	61	62	63	64
	User Defined												
	65	66	67	68	69	70	71	72	73	74	75	76	77
	User Defined												

Notes:

1. Xilinx carrier cards, their reference designs and software stacks use some MIO pins for special purposes as listed by pin. They are used in the released Linux image, image selector, image recovery, PMU firmware, and other firmware apps. Custom designs can choose to align the MIO pins to these optional default assignments to adopt these software features with minimal customization.
   a. MIO12 is the firmware update enable pin
   b. MIO31 is the hardware driven shutdown pin when used as an input to the PMU
   c. MIO35 is the PMU external watchdog pin
   d. MIO36 and MIO37 are the default Linux console interface pins
2. MIO31, MIO32, and MIO33 are reserved for the PMU. These pins are fixed in the SOM hardware design.

MIO Peripherals

A number of peripherals are available within the MIO. The following is a summary of the interfaces that can be configured for your applications.

- **PS-GTR transceivers (x4):** Four dedicated PS-GTR receivers and transmitters with up to 6.0 Gb/s data rates supporting SGMII, tri-speed Ethernet, PCI Express® Gen2, serial ATA (SATA), USB3.0, and DisplayPort
- **Gigabit Ethernet MAC (GEM):** Four 10/100/1000 tri-speed GEM peripherals with IEEE Std 802.3 and IEEE Std 1588 revision 2.0 support
- **DisplayPort controller:** Provides a flexible display output with direct memory access (DMA), centralized buffer manager, rendering block, and audio mixer block.
- **CAN controller:** Two full CAN 2.0B, CAN 2.0A, and ISO 118981-1 standards compliant CAN bus interfaces.
- **USB controller:** Two USB 3.0/2.0 device, host, or OTG peripherals, each supporting up to 12 endpoints.
- **PCI Express controller:** Compliant with the PCI Express base specification 2.1 with support for x1, x2, or x4 line width at Gen1 (2.5 GT/s) or Gen2 (5 GT/s) rates.
- **SD/SDIO/eMMC controller:** One SD/SDIO 2.0/eMMC4.51 compliant controller.
- **UART controller:** One high-speed UART (up to 1 Mb/s)
- **SPI controller:** One full-duplex SPI port with three peripheral chip selects.
- **SATA Host controller:** Supports up to two channels at 1.5, 3.0, and 6.0 Gb/s data rates as defined by the SATA specification, revision 3.1
- **I2C controller:** Master and slave I2C interface with support for multi-master designs and clock rates up to 400 Kb/s.

I2C Bus Interface

The PS hosts the SOM I2C platform management bus for interfacing with supporting SOM peripherals. These devices are summarized in the following table. The PS I2C bus interface can be extended on a carrier card, but must not introduce address conflicts. The following table defines the K26 SOM I2C device addresses in 7-bit format.

Table 4: **SOM I2C Interface Addresses**

I2C 7-bit Address	Description
0x50, 0x58	SOM EEPROM
0x30, 0x31	DA9062 PMIC
0x32	DA9130 PMIC
0x33	DA9131 PMIC
0x68	PL power domain monitor
0x70	PS power domain monitor

Programmable Logic

The K26 SOM includes a custom-built Zynq UltraScale+ MPSoC (XCK26), that runs optimally (and exclusively) on the K26 SOM and includes a flexible and extensible programmable logic system (PL), an integrated video codec (VCU), and 12.5 Gb/s high-speed transceivers (GTH). The PL resources are summarized in the following table.

Table 5: **PL Resources**

Resource	K26 SOM	Description
System logic cells	256,200	Programmable logic cells for available
CLB flip-flops	234,240	Configurable logic block (CLB): Total number of flip-flops
CLB LUTs	117,120	Configurable logic block: Total number of look-up tables
Distributed RAM (Mb)	3.5	Distributed memory
Block RAM	144	Number of 36 Kb block RAMs
Block RAM (Mb)	5.1	Total block RAM memory footprint
UltraRAM blocks	64	288 Kb dual-port, 72-bit-wide memory with error correction
DSP slices	1,248	27 x 18 signed multiplier with 48-bit adder/accumulator
GTH transceivers	4	12.5 Gb/s serial transceivers
Video Codec	1	H.264 and H.265 supported simultaneous encode/decode
HDIO	69	High-density I/O supports 1.2V to 3.3V rails
HPIO	58	High-performance I/O differential pairs supports 1.0V to 1.8V rails

Boot Sources and Storage Devices

The K26 SOM includes two nonvolatile storage boot devices, a QSPI flash memory, and an eMMC flash memory. The primary boot device is selected by tying the MODE[3:0] pins to the desired value on your carrier card. The boot-mode pins are made available at the SOM connector to allow flexibility in defining the boot device. The boot-mode configurations for using QSPI or eMMC are shown in the following table. Other boot-mode options can be introduced based on your carrier card design. See the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) for the full set of boot-mode definitions. Reference the *Kria SOM Carrier Card Design Guide* (UG1091) for details on strapping the boot-mode resistors.

Table 6: **Boot Mode Pins and Location**

Boot Mode	PS_Mode Pins[3:0]	Physical Pin Location
Quad-SPI (32 bit)	0010	MIO[5:0]
eMMC	0110	MIO[22:13]

The K26 SOM provides two storage devices to enable a primary/secondary boot process with isolation between boot firmware and operating system (OS) storage, or similar device firmware segmentation. As an example of the supported hierarchical boot process, the SOM boot mode can be set to QSPI as the primary boot device, which contains the power-on boot firmware, and then the power-on boot loader (e.g., U-Boot) loads the OS from the eMMC secondary boot device.

Security Features

The K26 SOM provides two levels of security with dedicated hardware built into the MPSoC and an on-board trusted platform module (TPM) device. Together they enable implementation of tamper monitoring, secure boot, measured boot, and hardware accelerated cryptographic functions.

The K26 SOM includes the following security features:

- Encryption and authentication of configuration files (non-ED devices only)
- Hardened crypto-accelerators available for user applications (non-ED devices only)
- Secure methods for storing cryptographic keys via eFUSEs
- Methods for detecting and responding to device tamper events

MPSoCs have a dedicated configuration security unit (CSU), which is used for supporting secure boot, tamper monitoring, secure key storage, and cryptographic hardware acceleration. See the *Security* chapter in the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) for implementation details. The cryptographic accelerators available on the MPSoC are as follows:

- SHA-3/384
- AES-GCM-256
- RSA exponential multiplier

The CSU, an internal on-chip memory (OCM), and flexible key storage provide hardware root of trust mechanisms for implementing secure boot within the MPSoC. The hardware capabilities support authenticated and encrypted protections for boot and associated configuration files.

After ensuring the initial boot integrity of the device, the CSU then acts as a centralized tamper monitoring and response controller using the MPSoC integrated system monitor (SYSMON) for measuring and implementing voltage and temperature alarms and configurations. Various alarms and set points can be configured as defined in the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085).

The MPSoC includes a key management infrastructure supporting battery-backed RAM (BBRAM), eFUSE, embedded boot keys, and device family keys. When BBRAM is required, battery backup must be provided on the carrier card. Additional details on the key management functions of the MPSoC are outlined in the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085).

The MPSoC contains a 96-bit unique, nonvolatile device identifier called the device DNA that is permanently programmed in the MPSoC. The SOM EEPROM also contains a unique identifier (UID), programmed at the time of SOM manufacturing. These unique identifiers support the implementation over-the-air (OTA) device enrollment and attestation functionality.

The MPSoC eFUSEs allow permanent enable or disable of specific features to protect deployed systems. A complete list of these capabilities is outlined in the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085). Two commonly used features are:

- **RSA_EN:** Forces every device boot to be authenticated via RSA
- **JTAG_DIS:** Disables JTAG

In addition to the MPSoC security features, the SOM includes an external TPM device, compliant with the trusted computing group (TCG) TPM 2.0 standard. The TPM 2.0 device enables hardware-based security for remote attestation, measured boot, and other secure cryptographic functions. The TPM reset is connected to PS_POR_L.

Electrical Specifications

This section describes the electrical interfaces and connections available on the SOM to use with your carrier card design.

SOM Connector Overview

The K26 SOM uses two 240-pin connectors to provide electrical connectivity between the SOM and the carrier card. These two connectors are referred to as SOM240_1 and SOM240_2.

The SOM240_1 and SOM240_2 connectors use the Samtec 0.635 mm AcceleRate HD high-density 4-row, 60 position connector set. The part number for the socket (ADF6-60-03.5-L-4-2-A) is used on the bottom side of the SOM. The part number for the terminal (ADM6-60-01.5-L-4-2-A) is for use on the carrier card.

Note: The ADM6-60-01.5-L-4-2-A connector is referenced throughout this document. However, the Samtec REF-226081 is an alternative connector. Contact your Samtec distributor for more information.

The SOM240_1 and SOM240_2 connectors provide support for following interfaces.

- Control and status signals
- Multiplexed I/O (MIO) bank
- PS-GTR high-speed serial transceiver signals
- High-performance I/O (HPIO) bank signals
- High-density I/O (HDIO) bank signals
- GTH high-speed serial transceiver signals
- Power system

Supported I/O Standards

The K26 SOM supports all I/O standards supported by the respective bank that a signal is connected to with the exception of I/O standards that require a reference voltage (V_{REF}). For more information, refer to the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

During power-up and configuration, internal pull-up resistors are disabled and each SelectIO™ pin is set to 3-state.

The K26 SOM is built with the XCK26-SFVC784-2LV device; which has a -2 speed grade and is an LV device (operates at V_{CCINT} = 0.72V). Consult the corresponding I/O speed tables in *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925) for the definition of maximum data rates.

Signal Naming Conventions

For signal to connector mapping in text format, see the relevant XDC and trace delay files. These files provide the Zynq® UltraScale+™ MPSoC constraints and package pin name to SOM240_x mapping. The SOM240 connectors adopt the naming conventions outlined in the following table.

Table 7: **SOM240 Signal Naming Conventions**

Signal	Description
Module (M)	The SOM, in this case the K26 SOM.
Carrier card (C)	The board that the SOM is plugged into is called the carrier card.
C2M	Signal names with `C2M` indicate that the signal is driven by the carrier card and received by the SOM.
M2C	Signal names with `M2C` indicate that the signal is driven by the SOM and received by the carrier card.
_P	The postfix `_P` on differential signal pairs indicates the positive component of a differential signal.
_N	The postfix `_N` on differential signal pairs indicates the negative component of a differential signal.
_L	The postfix `_L` on a single-ended signal indicates an active-Low signal. This is used for the connector pinouts only. The postfix _B is also used to indicate an active-Low signal.

Table 8: **Legend for Connector Pinouts**

Example	SOM240 Connector	Function
GND	Both SOM240_1 and SOM240_2	Ground pins
VCC_SOM	Both SOM240_1 and SOM240_2	Power connection pins
MIO35	SOM240_1	MIO 501 bank pins
MIO58	SOM240_1	MIO 502 bank pins
JTAG_TMS_C2M	SOM240_1	Configuration and control pins
GTR_DP1_M2C_P	SOM240_1	PS-GTR transceiver pins
HPA04_P	SOM240_1	HPA pins
HDA00_CC	SOM240_1	HDA pins
HPB15_CC_P	SOM240_2	HPB pins
HPC07_P	SOM240_2	HPC pins
HDB12	SOM240_2	HDB pins
HDC00_CC	SOM240_2	HDC pins
GTH_DP2_C2M_P	SOM240_2	GTH transceiver pins

Refer to the *Zynq UltraScale+ Device Packaging and Pinouts Product Specification User Guide* (UG1075) for more information on pin types.

Table 9: **Legend for Pin Types**

Example	Definition
GC	Global clock
HDGC	Global clock
VRP	DCI voltage reference resistor
QBC	Byte lane clock
DBC	Byte lane clock
PERSTN	Default reset pin locations for integrated block for PCI Express®
PU18_10	10.0 KΩ pull-up resistor to VCC_PS_1V80
PU18_2p2	2.21 KΩ pull-up resistor to VCC_PS_1V80
PU18_4p7	4.7 KΩ pull-up resistor to VCC_PS_1V80
PU50	10.0 KΩ pull-up resistor to VCC_5V0
PD50	49.9 KΩ pull-down resistor to VCC_5V0
AC01UF	AC coupled with 0.01 µF capacitor on the SOM

SOM240_1 Connector Pinout

The SOM240_1 connector provides access to two MIO banks (MIO501, MIO502), HPIO bank 66 (HPA), HDIO bank 45 (HDA), and the PS-GTR transceivers (MIO505). It also provides sideband signals for configuration and operation of the board. For additional pin definitions see the K26 SOM XDC file.

Table 10: **SOM240_1 Connector Pinout**

Connector Row/Pin Number	A	B	C	D
1	VCC_BATT	HPA05_CC_P	GND	VCCO_HPA
2	GND	HPA05_CC_N	GND	VCCO_HPA
3	HPA06_P	GND	HPA00_CC_P	GND
4	HPA06_N	HPA04_P	HPA00_CC_N	HPA02_P
5	GND	HPA04_N	GND	HPA02_N
6	HPA_CLK0_P	GND	HPA03_P	GND
7	HPA_CLK0_N	HPA07_P	HPA03_N	HPA01_P
8	GND	HPA07_N	GND	HPA01_N
9	HPA12_P	GND	HPA08_P	GND
10	HPA12_N	HPA11_P	HPA08_N	HPA09_P
11	GND	HPA11_N	GND	HPA09_N
12	HPA13_P	GND	HPA10_CC_P	GND
13	HPA13_N	VCCO_HDA	HPA10_CC_N	HPA14_P
14	GND	VCCO_HDA	GND	HPA14_N
15	HDA09	GND	PS_POR_L	GND
16	HDA10	HDA03	PS_SRST_C2M_L	HDA00_CC
17	HDA11	HDA04	GND	HDA01
18	GND	HDA05	HDA06	HDA02
19	VCCOEN_PS_M2C	GND	HDA07	GND

Table 10: **SOM240_1 Connector Pinout** *(cont'd)*

Connector Row/Pin Number	A	B	C	D
20	VCCOEN_PL_M2C	HDA15	HDA08_CC	HDA12
21	GND	HDA16_CC	GND	HDA13
22	JTAG_TMS_C2M	HDA17	HDA18	HDA14
23	JTAG_TDO_M2C	GND	HDA19	GND
24	JTAG_TDI_C2M	PS_ERROR_OUT_M2C	HDA20	PWRGD_FPD_M2C
25	JTAG_TCK_C2M	PS_ERROR_STATUS_M2C	GND	PWRGD_LPD_M2C
26	GND	PWROFF_C2M_L	MIO24_I2C_SCK	PWRGD_PL_M2C
27	MODE0_C2M	GND	MIO25_I2C_SDA	GND
28	MODE1_C2M	MIO35_WD_OUT	MIO12_FWUEN_C2M_L	MIO26
29	MODE2_C2M	MIO36	GND	MIO27
30	MODE3_C2M	MIO37	MIO29	MIO28
31	Reserved	GND	MIO30	GND
32	Reserved	MIO38	MIO31_SHUTDOWN	MIO44
33	GND	MIO39	GND	MIO45
34	MIO41	MIO40	MIO47	MIO46
35	MIO42	GND	MIO48	GND
36	MIO43	MIO50	MIO49	MIO52
37	GND	MIO51	GND	MIO53
38	MIO61	Reserved	MIO55	MIO54
39	MIO62	GND	MIO56	GND
40	MIO63	MIO58	MIO57	MIO64
41	GND	MIO59	GND	MIO65
42	MIO73	MIO60	MIO67	MIO66
43	MIO74	GND	MIO68	GND
44	MIO75	MIO70	MIO69	MIO76
45	GND	MIO71	Reserved	MIO77
46	GND	MIO72	GND	Reserved
47	GTR_DP1_M2C_P	GND	GTR_REFCLK0_C2M_P	GND
48	GTR_DP1_M2C_N	GND	GTR_REFCLK0_C2M_N	GND
49	GND	GTR_REFCLK1_C2M_P	GND	GTR_DP3_C2M_P
50	GND	GTR_REFCLK1_C2M_N	GND	GTR_DP3_C2M_N
51	GTR_REFCLK3_C2M_P	GND	GTR_DP3_M2C_P	GND
52	GTR_REFCLK3_C2M_N	GND	GTR_DP3_M2C_N	GND
53	GND	GTR_DP2_C2M_P	GND	GTR_REFCLK2_C2M_P
54	GND	GTR_DP2_C2M_N	GND	GTR_REFCLK2_C2M_N
55	GTR_DP0_C2M_P	GND	GTR_DP1_C2M_P	GND
56	GTR_DP0_C2M_N	GND	GTR_DP1_C2M_N	GND
57	GND	GTR_DP0_M2C_P	GND	GTR_DP2_M2C_P
58	GND	GTR_DP0_M2C_N	GND	GTR_DP2_M2C_N
59	VCC_SOM	GND	VCC_SOM	GND

Table 10: **SOM240_1 Connector Pinout** *(cont'd)*

Connector Row/Pin Number	A	B	C	D
60	VCC_SOM	VCC_SOM	VCC_SOM	VCC_SOM

SOM240_1 Signal Names and Descriptions

See the *Zynq UltraScale+ Device Packaging and Pinouts Product Specification User Guide* (UG1075) for further pin descriptions.

Table 11: **SOM240_1 Signal Pins**

Pin Number	Pin Type	Signal Name	Signal Description
Connector Row A			
A1		VCC_BATT	PS BBRAM and real-time clock (RTC) supply voltage, requires external battery. Connect to GND when battery is not used.
A2		GND	Ground, connect to carrier card ground plane
A3		HPA06_P	HPIO on bank 66
A4		HPA06_N	HPIO on bank 66
A5		GND	Ground, connect to carrier card ground plane
A6	GC	HPA_CLK0_P	HPIO global clock pin on bank 66
A7	GC	HPA_CLK0_N	HPIO global clock pin on bank 66
A8		GND	Ground, connect to carrier card ground plane
A9		HPA12_P	HPIO on bank 66
A10		HPA12_N	HPIO on bank 66
A11		GND	Ground, connect to carrier card ground plane
A12	QBC	HPA13_P	HPIO on bank 66
A13	QBC	HPA13_N	HPIO on bank 66
A14		GND	Ground, connect to carrier card ground plane
A15	HDGC	HDA09	HDIO on bank 45
A16		HDA10	HDIO on bank 45
A17		HDA11	HDIO on bank 45
A18		GND	Ground, connect to carrier card ground plane
A19	PD50	VCCOEN_PS_M2C	Indication to turn on power for PS I/O peripherals on the carrier card
A20	PD50	VCCOEN_PL_M2C	Indication to turn on power for PL /IO peripherals on the carrier card
A21		GND	Ground, connect to carrier card ground plane
A22	PU18_4p7	JTAG_TMS_C2M	JTAG mode select
A23	PU18_4p7	JTAG_TDO_M2C	JTAG data out
A24	PU18_4p7	JTAG_TDI_C2M	JTAG data in
A25	PU18_4p7	JTAG_TCK_C2M	JTAG clock
A26		GND	Ground, connect to carrier card ground plane
A27	PU18_4p7	MODE0_C2M	PS mode bit 0
A28	PU18_4p7	MODE1_C2M	PS mode bit 1
A29	PU18_4p7	MODE2_C2M	PS mode bit 2

Table 11: **SOM240_1 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
A30	PU18_4p7	MODE3_C2M	PS mode bit 3
A31		Reserved	No connect on the SOM
A32		Reserved	No connect on the SOM
A33		GND	Ground, connect to carrier card ground plane
A34		MIO41	PS MIO signal on bank 501
A35		MIO42	PS MIO signal on bank 501
A36		MIO43	PS MIO signal on bank 501
A37		GND	Ground, connect to carrier card ground plane
A38		MIO61	PS MIO signal on bank 502
A39		MIO62	PS MIO signal on bank 502
A40		MIO63	PS MIO signal on bank 502
A41		GND	Ground, connect to carrier card ground plane
A42		MIO73	PS MIO signal on bank 502
A43		MIO74	PS MIO signal on bank 502
A44		MIO75	PS MIO signal on bank 502
A45		GND	Ground, connect to carrier card ground plane
A46		GND	Ground, connect to carrier card ground plane
A47		GTR_DP1_M2C_P	PS-GTR lane 1 TX, bank 505
A48		GTR_DP1_M2C_N	PS-GTR lane 1 TX, bank 505
A49		GND	Ground, connect to carrier card ground plane
A50		GND	Ground, connect to carrier card ground plane
A51	AC01UF	GTR_REFCLK3_C2M_P	PS-GTR REFCLK3 input, bank 505
A52	AC01UF	GTR_REFCLK3_C2M_N	PS-GTR REFCLK3 input, bank 505
A53		GND	Ground, connect to carrier card ground plane
A54		GND	Ground, connect to carrier card ground plane
A55		GTR_DP0_C2M_P	PS-GTR lane 0 RX, bank 505
A56		GTR_DP0_C2M_N	PS-GTR lane 0 RX, bank 505
A57		GND	Ground, connect to carrier card ground plane
A58		GND	Ground, connect to carrier card ground plane
A59		VCC_SOM	SOM main supply voltage, +5V
A60		VCC_SOM	SOM main supply voltage, +5V
Connector Row B			
B1	QBC	HPA05_CC_P	HPIO clock-capable pin on bank 66
B2	QBC	HPA05_CC_N	HPIO clock-capable pin on bank 66
B3		GND	Ground, connect to carrier card ground plane
B4		HPA04_P	HPIO on bank 66
B5		HPA04_N	HPIO on bank 66
B6		GND	Ground, connect to carrier card ground plane
B7		HPA07_P	HPIO on bank 66
B8		HPA07_N	HPIO on bank 66
B9		GND	Ground, connect to carrier card ground plane
B10	GC	HPA11_P	HPIO on bank 66

Table 11: **SOM240_1 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
B11	GC	HPA11_N	HPIO on bank 66
B12		GND	Ground, connect to carrier card ground plane
B13		VCCO_HDA	HDA I/O voltage rail, 1.2V to 3.3V
B14		VCCO_HDA	HDA I/O voltage rail, 1.2V to 3.3V
B15		GND	Ground, connect to carrier card ground plane
B16		HDA03	HDIO on bank 45
B17		HDA04	HDIO on bank 45
B18		HDA05	HDIO on bank 45
B19		GND	Ground, connect to carrier card ground plane
B20		HDA15	HDIO on bank 45
B21	HDGC	HDA16_CC	HDIO clock-capable pin on bank 45
B22	HDGC	HDA17	HDIO on bank 45
B23		GND	Ground, connect to carrier card ground plane
B24		PS_ERROR_OUT_M2C	PS error indication from SOM
B25		PS_ERROR_STATUS_M2C	PS error status from SOM
B26	PU50	PWROFF_C2M_L	Control signal to turn off all power rails on the SOM
B27		GND	Ground, connect to carrier card ground plane
B28		MIO35_WD_OUT	PS MIO signal on bank 501. Optional use as PMU output. Default use as PMU watchdog output in the released Kria PetaLinux BSPs.
B29		MIO36	PS MIO signal on bank 501. Optional use as PMU output. Default use as UART txd in the released Kria PetaLinux BSPs.
B30		MIO37	PS MIO signal on bank 501. Optional use as PMU output. Default use as UART rxd in the released Kria PetaLinux BSPs.
B31		GND	Ground, connect to carrier card ground plane
B32		MIO38	PS MIO signal on bank 501
B33		MIO39	PS MIO signal on bank 501
B34		MIO40	PS MIO signal on bank 501
B35		GND	Ground, connect to carrier card ground plane
B36		MIO50	PS MIO signal on bank 501
B37		MIO51	PS MIO signal on bank 501
B38		Reserved	Not connected to SOM connector
B39		GND	Ground, connect to carrier card ground plane
B40		MIO58	PS MIO signal on bank 502
B41		MIO59	PS MIO signal on bank 502
B42		MIO60	PS MIO signal on bank 502
B43		GND	Ground, connect to carrier card ground plane
B44		MIO70	PS MIO signal on bank 502
B45		MIO71	PS MIO signal on bank 502
B46		MIO72	PS MIO signal on bank 502
B47		GND	Ground, connect to carrier card ground plane
B48		GND	Ground, connect to carrier card ground plane
B49	AC01UF	GTR_REFCLK1_C2M_P	PS-GTR REFCLK1 input, bank 505
B50	AC01UF	GTR_REFCLK1_C2M_N	PS-GTR REFCLK1 input, bank 505

Table 11: **SOM240_1 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
B51		GND	Ground, connect to carrier card ground plane
B52		GND	Ground, connect to carrier card ground plane
B53		GTR_DP2_C2M_P	PS-GTR lane 2 RX, bank 505
B54		GTR_DP2_C2M_N	PS-GTR lane 2 RX, bank 505
B55		GND	Ground, connect to carrier card ground plane
B56		GND	Ground, connect to carrier card ground plane
B57		GTR_DP0_M2C_P	PS-GTR lane 0 TX, bank 505
B58		GTR_DP0_M2C_N	PS-GTR lane 0 TX, bank 505
B59		GND	Ground, connect to carrier card ground plane
B60		VCC_SOM	SOM main supply voltage, +5V
Connector Row C			
C1		GND	Ground, connect to carrier card ground plane
C2		GND	Ground, connect to carrier card ground plane
C3	DBC	HPA00_CC_P	HPIO clock-capable pin on bank 66
C4	DBC	HPA00_CC_N	HPIO clock-capable pin on bank 66
C5		GND	Ground, connect to carrier card ground plane
C6	DBC	HPA03_P	HPIO on bank 66
C7	DBC	HPA03_N	HPIO on bank 66
C8		GND	Ground, connect to carrier card ground plane
C9	QBC	HPA08_P	HPIO on bank 66
C10	QBC	HPA08_N	HPIO on bank 66
C11		GND	Ground, connect to carrier card ground plane
C12	GC, QBC	HPA10_CC_P	HPIO clock-capable pin on bank 66
C13	GC, QBC	HPA10_CC_N	HPIO clock-capable pin on bank 66
C14		GND	Ground, connect to carrier card ground plane
C15	PU18_4p7	PS_POR_L	PS power-on reset driven by the carrier card. When deasserted, the PS begins the boot process.
C16	PU18_4p7	PS_SRST_C2M_L	PS system reset driven by the carrier card. When asserted, forces the PS to enter the system reset sequence.
C17		GND	Ground, connect to carrier card ground plane
C18		HDA06	HDIO on bank 45
C19		HDA07	HDIO on bank 45
C20	HDGC	HDA08_CC	HDIO clock-capable pin on bank 45
C21		GND	Ground
C22		HDA18	HDIO on bank 45
C23		HDA19	HDIO on bank 45
C24		HDA20	HDIO on bank 45
C25		GND	Ground, connect to carrier card ground plane
C26	PU18_2p2	MIO24_I2C_SCK	PS I2C clock output, bank 500
C27	PU18_2p2	MIO25_I2C_SDA	PS I2C serial data, bank 500
C28	PU18_10	MIO12_FWUEN_C2M_L	PS MIO signal on bank 500. Optional default use as firmware update enable indication in the released Kria PetaLinux BSPs.
C29		GND	Ground, connect to carrier card ground plane

Table 11: **SOM240_1 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
C30		MIO29	PS MIO signal on bank 501. Optional use as PMU input.
C31		MIO30	PS MIO signal on bank 501. Optional use as PMU input.
C32		MIO31_SHUTDOWN	PS MIO signal on bank 501. Optional use as PMU input. In default Kria PetaLinux BSPs, this is a PMU library enabled input for hardware-initiated shutdown by the PMU.
C33		GND	Ground, connect to carrier card ground plane
C34		MIO47	PS MIO signal on bank 501
C35		MIO48	PS MIO signal on bank 501
C36		MIO49	PS MIO signal on bank 501
C37		GND	Ground, connect to carrier card ground plane
C38		MIO55	PS MIO signal on bank 502
C39		MIO56	PS MIO signal on bank 502
C40		MIO57	PS MIO signal on bank 502
C41		GND	Ground, connect to carrier card ground plane
C42		MIO67	PS MIO signal on bank 502
C43		MIO68	PS MIO signal on bank 502
C44		MIO69	PS MIO signal on bank 502
C45		Reserved	No connect on the SOM
C46		GND	Ground, connect to carrier card ground plane
C47	AC01UF	GTR_REFCLK0_C2M_P	PS-GTR REFCLK0 input, bank 505
C48	AC01UF	GTR_REFCLK0_C2M_N	PS-GTR REFCLK0 input, bank 505
C49		GND	Ground, connect to carrier card ground plane
C50		GND	Ground, connect to carrier card ground plane
C51		GTR_DP3_M2C_P	PS-GTR lane 3 TX, bank 505
C52		GTR_DP3_M2C_N	PS-GTR lane 3 TX, bank 505
C53		GND	Ground, connect to carrier card ground plane
C54		GND	Ground, connect to carrier card ground plane
C55		GTR_DP1_C2M_P	PS-GTR lane 1 RX, bank 505
C56		GTR_DP1_C2M_N	PS-GTR lane 1 RX, bank 505
C57		GND	Ground, connect to carrier card ground plane
C58		GND	Ground, connect to carrier card ground plane
C59		VCC_SOM	SOM main supply voltage, +5V
C60		VCC_SOM	SOM main supply voltage, +5V
Connector Row D			
D1		VCCO_HPA	HPA I/O voltage rail, 1.0V to 1.8V
D2		VCCO_HPA	HPA I/O voltage rail, 1.0V to 1.8V
D3		GND	Ground, connect to carrier card ground plane
D4		HPA02_P	HPIO on bank 66
D5		HPA02_N	HPIO on bank 66
D6		GND	Ground, connect to carrier card ground plane
D7		HPA01_P	HPIO on bank 66
D8		HPA01_N	HPIO on bank 66

Table 11: **SOM240_1 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
D9		GND	Ground, connect to carrier card ground plane
D10	GC	HPA09_P	HPIO on bank 66
D11	GC	HPA09_N	HPIO on bank 66
D12		GND	Ground, connect to carrier card ground plane
D13		HPA14_P	HPIO on bank 66
D14		HPA14_N	HPIO on bank 66
D15		GND	Ground, connect to carrier card ground plane
D16	HDGC	HDA00_CC	HDIO clock-capable pin on bank 45
D17	HDGC	HDA01	HDIO on bank 45
D18		HDA02	HDIO on bank 45
D19		GND	Ground, connect to carrier card ground plane
D20	HDGC	HDA12	HDIO on bank 45
D21	HDGC	HDA13	HDIO on bank 45
D22		HDA14	HDIO on bank 45
D23		GND	Ground, connect to carrier card ground plane
D24	PD50	PWRGD_FPD_M2C	Power good indication for PS FPD power rails
D25	PD50	PWRGD_LPD_M2C	Power good indication for PS LPD power rails
D26	PD50	PWRGD_PL_M2C	Power good indication for all PL power rails
D27		GND	Ground, connect to carrier card ground plane
D28		MIO26	PS MIO signal on bank 501. Optional use as PMU input.
D29		MIO27	PS MIO signal on bank 501. Optional use as PMU input.
D30		MIO28	PS MIO signal on bank 501. Optional use as PMU input.
D31		GND	Ground, connect to carrier card ground plane
D32		MIO44	PS MIO signal on bank 501
D33		MIO45	PS MIO signal on bank 501
D34		MIO46	PS MIO signal on bank 501
D35		GND	Ground, connect to carrier card ground plane
D36		MIO52	PS MIO signal on bank 502
D37		MIO53	PS MIO signal on bank 502
D38		MIO54	PS MIO signal on bank 502
D39		GND	Ground, connect to carrier card ground plane
D40		MIO64	PS MIO signal on bank 502
D41		MIO65	PS MIO signal on bank 502
D42		MIO66	PS MIO signal on bank 502
D43		GND	Ground, connect to carrier card ground plane
D44		MIO76	PS MIO signal on bank 502
D45		MIO77	PS MIO signal on bank 502
D46		Reserved	No connect on the SOM
D47		GND	Ground, connect to carrier card ground plane
D48		GND	Ground, connect to carrier card ground plane
D49		GTR_DP3_C2M_P	PS-GTR lane 3 RX, bank 505
D50		GTR_DP3_C2M_N	PS-GTR lane 3 RX, bank 505

Table 11: **SOM240_1 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
D51		GND	Ground, connect to carrier card ground plane
D52		GND	Ground, connect to carrier card ground plane
D53	AC01UF	GTR_REFCLK2_C2M_P	PS-GTR REFCLK2 input, bank 505
D54	AC01UF	GTR_REFCLK2_C2M_N	PS-GTR REFCLK2 input, bank 505
D55		GND	Ground, connect to carrier card ground plane
D56		GND	Ground, connect to carrier card ground plane
D57		GTR_DP2_M2C_P	PS-GTR lane 2 TX, bank 505
D58		GTR_DP2_M2C_N	PS-GTR lane 2 TX, bank 505
D59		GND	Ground, connect to carrier card ground plane
D60		VCC_SOM	SOM main supply voltage, +5V

SOM240_2 Connector Pinout

The SOM240_2 connector provides access to two HPIO bank 65 (HPB), HPIO bank 64 (HPC), HDIO bank43 (HDB, HDIO bank 44 (HDC), and the PL GTH Quad. For additional pin definitions see the K26 SOM XDC file.

Table 12: **SOM240_2 Connector Pinout**

Connector Row/Pin Number	A	B	C	D
1	GND	GTH_DP2_C2M_P	GND	GTH_DP1_C2M_P
2	GND	GTH_DP2_C2M_N	GND	GTH_DP1_C2M_N
3	GTH_DP3_M2C_P	GND	GTH_REFCLK0_C2M_P	GND
4	GTH_DP3_M2C_N	GND	GTH_REFCLK0_C2M_N	GND
5	GND	GTH_DP2_M2C_P	GND	GTH_DP3_C2M_P
6	GND	GTH_DP2_M2C_N	GND	GTH_DP3_C2M_N
7	GTH_REFCLK1_C2M_P	GND	GTH_DP1_M2C_P	GND
8	GTH_REFCLK1_C2M_N	GND	GTH_DP1_M2C_N	GND
9	GND	GTH_DP0_C2M_P	GND	GTH_DP0_M2C_P
10	GND	GTH_DP0_C2M_N	GND	GTH_DP0_M2C_N
11	HPB15_CC_P	GND	HPB09_P	GND
12	HPB15_CC_N	HPB10_CC_P	HPB09_N	HPB01_P
13	GND	HPB10_CC_N	GND	HPB01_N
14	HPB08_P	GND	HPB14_P	GND
15	HPB08_N	HPB07_P	HPB14_N	HPB00_CC_P
16	GND	HPB07_N	GND	HPB00_CC_N
17	HPB12_P	GND	HPB02_P	GND
18	HPB12_N	HPB05_CC_P	HPB02_N	HPB_CLK0_P
19	GND	HPB05_CC_N	GND	HPB_CLK0_N
20	HPB06_P	GND	HPB13_P	GND
21	HPB06_N	HPB11_P	HPB13_N	HPB04_P
22	GND	HPB11_N	GND	HPB04_N

Table 12: **SOM240_2 Connector Pinout** *(cont'd)*

Connector Row/Pin Number	A	B	C	D
23	HPB16_P	GND	HPB_18_P	GND
24	HPB16_N	HPB03_P	HPB_18_N	HPB17_P
25	GND	HPB03_N	GND	HPB17_N
26	HPB_19_P	GND	HPC17_P	GND
27	HPB_19_N	HPC06_P	HPC17_N	HPC09_P
28	GND	HPC06_N	GND	HPC09_N
29	HPC08_P	GND	HPC10_CC_P	GND
30	HPC08_N	HPC13_P	HPC10_CC_N	HPC01_P
31	GND	HPC13_N	GND	HPC01_N
32	HPC19_P	GND	HPC11_P	GND
33	HPC19_N	HPC16_P	HPC11_N	HPC00_CC_P
34	GND	HPC16_N	GND	HPC00_CC_N
35	HPC14_P	GND	HPC12_P	GND
36	HPC14_N	HPC07_P	HPC12_N	HPC02_P
37	GND	HPC07_N	GND	HPC02_N
38	HPC15_CC_P	GND	HPC05_CC_P	GND
39	HPC15_CC_N	HPC18_P	HPC05_CC_N	HPC04_P
40	GND	HPC18_N	GND	HPC04_N
41	HPC03_P	GND	HPC_CLK0_P	GND
42	HPC03_N	VCCO_HPB	HPC_CLK0_N	VCCO_HPC
43	GND	GND	GND	GND
44	VCCO_HPB	HDB12	VCCO_HPC	HDB00_CC
45	GND	HDB13	GND	HDB01
46	HDB18	HDB14	HDB06	HDB02
47	HDB19	GND	HDB07	GND
48	HDB20	HDB15	HDB08_CC	HDB03
49	GND	HDB16_CC	GND	HDB04
50	HDB21	HDB17	HDB09	HDB05
51	HDB22	GND	HDB10	GND
52	HDB23	HDC12	HDB11	HDC00_CC
53	GND	HDC13	GND	HDC01
54	HDC18	HDC14	HDC06	HDC02
55	HDC19	GND	HDC07	GND
56	HDC20	HDC15	HDC08_CC	HDC03
57	GND	HDC16_CC	GND	HDC04
58	HDC21	HDC17	HDC09	HDC05
59	HDC22	VCCO_HDB	HDC10	VCCO_HDC
60	HDC23	VCCO_HDB	HDC11	VCCO_HDC

SOM240_2 Signal Names and Descriptions

See the *Zynq UltraScale+ Device Packaging and Pinouts Product Specification User Guide* (UG1075) for further pin descriptions.

Table 13: **SOM240_2 Signal Pins**

Pin Number	Pin Type	Signal Name	Signal Description
Connector Row A			
A1		GND	Ground, connect to carrier card ground plane
A2		GND	Ground, connect to carrier card ground plane
A3		GTH_DP3_M2C_P	GTH lane 3 TX, bank 224
A4		GTH_DP3_M2C_N	GTH lane 3 TX, bank 224
A5		GND	Ground, connect to carrier card ground plane
A6		GND	Ground, connect to carrier card ground plane
A7	AC01UF	GTH_REFCLK1_C2M_P	GTH REFCLK1 input, bank 224
A8	AC01UF	GTH_REFCLK1_C2M_N	GTH REFCLK1 input, bank 224
A9		GND	Ground, connect to carrier card ground plane
A10		GND	Ground, connect to carrier card ground plane
A11	DBC	HPB15_CC_P	HPIO clock-capable pin on bank 65
A12	DBC	HPB15_CC_N	HPIO clock-capable pin on bank 65
A13		GND	Ground, connect to carrier card ground plane
A14	QBC	HPB08_P	HPIO on bank 65
A15	QBC	HPB08_N	HPIO on bank 65
A16		GND	Ground, connect to carrier card ground plane
A17		HPB12_P	HPIO on bank 65
A18		HPB12_N	HPIO on bank 65
A19		GND	Ground, connect to carrier card ground plane
A20		HPB06_P	HPIO on bank 65
A21		HPB06_N	HPIO on bank 65
A22		GND	Ground, connect to carrier card ground plane
A23		HPB16_P	HPIO on bank 65
A24		HPB16_N	HPIO on bank 65
A25		GND	Ground, connect to carrier card ground plane
A26	PERSTN1	HPB_19_P	HPIO on bank 65
A27	PERSTN0	HPB_19_N	HPIO on bank 65
A28		GND	Ground, connect to carrier card ground plane
A29	QBC	HPC08_P	HPIO on bank 64
A30	QBC	HPC08_N	HPIO on bank 64
A31		GND	Ground, connect to carrier card ground plane
A32		HPC19_P	HPIO on bank 64
A33		HPC19_N	HPIO on bank 64
A34		GND	Ground, connect to carrier card ground plane
A35		HPC14_P	HPIO on bank 64
A36		HPC14_N	HPIO on bank 64

Table 13: **SOM240_2 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
A37		GND	Ground, connect to carrier card ground plane
A38	DBC	HPC15_CC_P	HPIO clock-capable pin on bank 64
A39	DBC	HPC15_CC_N	HPIO clock-capable pin on bank 64
A40		GND	Ground, connect to carrier card ground plane
A41	DBC	HPC03_P	HPIO on bank 64
A42	DBC	HPC03_N	HPIO on bank 64
A43		GND	Ground, connect to carrier card ground plane
A44		VCCO_HPB	HPB I/O voltage rail, 1.0V to 1.8V
A45		GND	Ground, connect to carrier card ground plane
A46		HDB18	HDIO on bank 43
A47		HDB19	HDIO on bank 43
A48		HDB20	HDIO on bank 43
A49		GND	Ground, connect to carrier card ground plane
A50		HDB21	HDIO on bank 43
A51		HDB22	HDIO on bank 43
A52		HDB23	HDIO on bank 43
A53		GND	Ground, connect to carrier card ground plane
A54		HDC18	HDIO on bank 44
A55		HDC19	HDIO on bank 44
A56		HDC20	HDIO on bank 44
A57		GND	Ground, connect to carrier card ground plane
A58		HDC21	HDIO on bank 44
A59		HDC22	HDIO on bank 44
A60		HDC23	HDIO on bank 44
Connector Row B			
B1		GTH_DP2_C2M_P	GTH lane 2 RX, bank 224
B2		GTH_DP2_C2M_N	GTH lane 2 RX, bank 224
B3		GND	Ground, connect to carrier card ground plane
B4		GND	Ground, connect to carrier card ground plane
B5		GTH_DP2_M2C_P	GTH lane 2 TX, bank 224
B6		GTH_DP2_M2C_N	GTH lane 2 TX, bank 224
B7		GND	Ground, connect to carrier card ground plane
B8		GND	Ground, connect to carrier card ground plane
B9		GTH_DP0_C2M_P	GTH lane 0 RX, bank 224
B10		GTH_DP0_C2M_N	GTH lane 0 RX, bank 224
B11		GND	Ground, connect to carrier card ground plane
B12	GC, QBC	HPB10_CC_P	HPIO clock-capable pin on bank 65
B13	GC, QBC	HPB10_CC_N	HPIO clock-capable pin on bank 65
B14		GND	Ground, connect to carrier card ground plane
B15		HPB07_P	HPIO on bank 65
B16		HPB07_N	HPIO on bank 65
B17		GND	Ground, connect to carrier card ground plane

Table 13: **SOM240_2 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
B18	QBC	HPB05_CC_P	HPIO clock-capable pin on bank 65
B19	QBC	HPB05_CC_N	HPIO clock-capable pin on bank 65
B20		GND	Ground, connect to carrier card ground plane
B21	GC	HPB11_P	HPIO on bank 65
B22	GC	HPB11_N	HPIO on bank 65
B23		GND	Ground, connect to carrier card ground plane
B24	DBC	HPB03_P	HPIO on bank 65
B25	DBC	HPB03_N	HPIO on bank 65
B26		GND	Ground, connect to carrier card ground plane
B27		HPC06_P	HPIO on bank 64
B28		HPC06_N	HPIO on bank 64
B29		GND	Ground, connect to carrier card ground plane
B30	QBC	HPC13_P	HPIO on bank 64
B31	QBC	HPC13_N	HPIO on bank 64
B32		GND	Ground, connect to carrier card ground plane
B33		HPC16_P	HPIO on bank 64
B34		HPC16_N	HPIO on bank 64
B35		GND	Ground, connect to carrier card ground plane
B36		HPC07_P	HPIO on bank 64
B37		HPC07_N	HPIO on bank 64
B38		GND	Ground, connect to carrier card ground plane
B39	DBC	HPC18_P	HPIO on bank 64
B40	DBC	HPC18_N	HPIO on bank 64
B41		GND	Ground, connect to carrier card ground plane
B42		VCCO_HPB	HPB I/O voltage rail, 1.0V to 1.8V
B43		GND	Ground, connect to carrier card ground plane
B44	HDGC	HDB12	HDIO on bank 43
B45	HDGC	HDB13	HDIO on bank 43
B46		HDB14	HDIO on bank 43
B47		GND	Ground, connect to carrier card ground plane
B48		HDB15	HDIO on bank 43
B49	HDGC	HDB16_CC	HDIO clock-capable pin on bank 43
B50	HDGC	HDB17	HDIO on bank 43
B51		GND	Ground, connect to carrier card ground plane
B52	HDGC	HDC12	HDIO on bank 44
B53	HDGC	HDC13	HDIO on bank 44
B54		HDC14	HDIO on bank 44
B55		GND	Ground, connect to carrier card ground plane
B56		HDC15	HDIO on bank 44
B57	HDGC	HDC16_CC	HDIO clock-capable pin on bank 44
B58	HDGC	HDC17	HDIO on bank 44
B59		VCCO_HDB	HDB I/O voltage rail, 1.2V to 3.3V

Table 13: **SOM240_2 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
B60		VCCO_HDB	HDB I/O voltage rail, 1.2V to 3.3V
Connector Row C			
C1		GND	Ground, connect to carrier card ground plane
C2		GND	Ground, connect to carrier card ground plane
C3	AC01UF	GTH_REFCLK0_C2M_P	GTH REFCLK0 input, bank 224
C4	AC01UF	GTH_REFCLK0_C2M_N	GTH REFCLK0 input, bank 224
C5		GND	Ground, connect to carrier card ground plane
C6		GND	Ground, connect to carrier card ground plane
C7		GTH_DP1_M2C_P	GTH lane 1 TX, bank 224
C8		GTH_DP1_M2C_N	GTH lane 1 TX, bank 224
C9		GND	Ground, connect to carrier card ground plane
C10		GND	Ground, connect to carrier card ground plane
C11	GC	HPB09_P	HPIO on bank 65
C12	GC	HPB09_N	HPIO on bank 65
C13		GND	Ground, connect to carrier card ground plane
C14		HPB14_P	HPIO on bank 65
C15		HPB14_N	HPIO on bank 65
C16		GND	Ground, connect to carrier card ground plane
C17		HPB02_P	HPIO on bank 65
C18		HPB02_N	HPIO on bank 65
C19		GND	Ground, connect to carrier card ground plane
C20	QBC	HPB13_P	HPIO on bank 65
C21	QBC	HPB13_N	HPIO on bank 65
C22		GND	Ground, connect to carrier card ground plane
C23		HPB_18_P	HPIO on bank 65
C24		HPB_18_N	HPIO on bank 65
C25		GND	Ground, connect to carrier card ground plane
C26		HPC17_P	HPIO on bank 64
C27		HPC17_N	HPIO on bank 64
C28		GND	Ground, connect to carrier card ground plane
C29	GC, QBC	HPC10_CC_P	HPIO clock-capable pin on bank 64
C30	GC, QBC	HPC10_CC_N	HPIO clock-capable pin on bank 64
C31		GND	Ground, connect to carrier card ground plane
C32	GC	HPC11_P	HPIO on bank 64
C33	GC	HPC11_N	HPIO on bank 64
C34		GND	Ground, connect to carrier card ground plane
C35		HPC12_P	HPIO on bank 64
C36		HPC12_N	HPIO on bank 64
C37		GND	Ground, connect to carrier card ground plane
C38	QBC	HPC05_CC_P	HPIO clock-capable pin on bank 64
C39	QBC	HPC05_CC_N	HPIO clock-capable pin on bank 64
C40		GND	Ground, connect to carrier card ground plane

Table 13: **SOM240_2 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
C41	GC	HPC_CLK0_P	HPIO global clock pin on bank 64
C42	GC	HPC_CLK0_N	HPIO global clock pin on bank 64
C43		GND	Ground, connect to carrier card ground plane
C44		VCCO_HPC	HPC I/O voltage rail, 1.0V to 1.8V
C45		GND	Ground, connect to carrier card ground plane
C46		HDB06	HDIO on bank 43
C47		HDB07	HDIO on bank 43
C48	HDGC	HDB08_CC	HDIO clock-capable pin on bank 43
C49		GND	Ground, connect to carrier card ground plane
C50	HDGC	HDB09	HDIO on bank 43
C51		HDB10	HDIO on bank 43
C52		HDB11	HDIO on bank 43
C53		GND	Ground, connect to carrier card ground plane
C54		HDC06	HDIO on bank 44
C55		HDC07	HDIO on bank 44
C56	HDGC	HDC08_CC	HDIO clock-capable pin on bank 44
C57		GND	Ground, connect to carrier card ground plane
C58	HDGC	HDC09	HDIO on bank 44
C59		HDC10	HDIO on bank 44
C60		HDC11	HDIO on bank 44
Connector Row D			
D1		GTH_DP1_C2M_P	GTH lane 1 RX, bank 224
D2		GTH_DP1_C2M_N	GTH lane 1 RX, bank 224
D3		GND	Ground, connect to carrier card ground plane
D4		GND	Ground, connect to carrier card ground plane
D5		GTH_DP3_C2M_P	GTH lane 3 RX, bank 224
D6		GTH_DP3_C2M_N	GTH lane 3 RX, bank 224
D7		GND	Ground, connect to carrier card ground plane
D8		GND	Ground, connect to carrier card ground plane
D9		GTH_DP0_M2C_P	GTH lane 0 TX, bank 224
D10		GTH_DP0_M2C_N	GTH lane 0 TX, bank 224
D11		GND	Ground, connect to carrier card ground plane
D12		HPB01_P	HPIO on bank 65
D13		HPB01_N	HPIO on bank 65
D14		GND	Ground, connect to carrier card ground plane
D15	DBC	HPB00_CC_P	HPIO clock-capable pin on bank 65
D16	DBC	HPB00_CC_N	HPIO clock-capable pin on bank 65
D17		GND	Ground, connect to carrier card ground plane
D18	GC	HPB_CLK0_P	HPIO global clock pin on bank 65
D19	GC	HPB_CLK0_N	HPIO global clock pin on bank 65
D20		GND	Ground, connect to carrier card ground plane
D21		HPB04_P	HPIO on bank 65

Table 13: **SOM240_2 Signal Pins** *(cont'd)*

Pin Number	Pin Type	Signal Name	Signal Description
D22		HPB04_N	HPIO on bank 65
D23		GND	Ground, connect to carrier card ground plane
D24	DBC	HPB17_P	HPIO on bank 65
D25	DBC	HPB17_N	HPIO on bank 65
D26		GND	Ground, connect to carrier card ground plane
D27	GC	HPC09_P	HPIO on bank 64
D28	GC	HPC09_N	HPIO on bank 64
D29		GND	Ground, connect to carrier card ground plane
D30		HPC01_P	HPIO on bank 64
D31		HPC01_N	HPIO on bank 64
D32		GND	Ground, connect to carrier card ground plane
D33	DBC	HPC00_CC_P	HPIO clock-capable pin on bank 64
D34	DBC	HPC00_CC_N	HPIO clock-capable pin on bank 64
D35		GND	Ground, connect to carrier card ground plane
D36		HPC02_P	HPIO on bank 64
D37		HPC02_N	HPIO on bank 64
D38		GND	Ground, connect to carrier card ground plane
D39		HPC04_P	HPIO on bank 64
D40		HPC04_N	HPIO on bank 64
D41		GND	Ground, connect to carrier card ground plane
D42		VCCO_HPC	HPC I/O voltage rail, 1.0V to 1.8V
D43		GND	Ground, connect to carrier card ground plane
D44	HDGC	HDB00_CC	HDIO clock-capable pin on bank 43
D45	HDGC	HDB01	HDIO on bank 43
D46		HDB02	HDIO on bank 43
D47		GND	Ground, connect to carrier card ground plane
D48		HDB03	HDIO on bank 43
D49		HDB04	HDIO on bank 43
D50		HDB05	HDIO on bank 43
D51		GND	Ground, connect to carrier card ground plane
D52	HDGC	HDC00_CC	HDIO clock-capable pin on bank 44
D53	HDGC	HDC01	HDIO on bank 44
D54		HDC02	HDIO on bank 44
D55		GND	Ground, connect to carrier card ground plane
D56		HDC03	HDIO on bank 44
D57		HDC04	HDIO on bank 44
D58		HDC05	HDIO on bank 44
D59		VCCO_HDC	HDC I/O voltage rail, 1.2V to 3.3V
D60		VCCO_HDC	HDC I/O voltage rail, 1.2V to 3.3V

Functional Signal Descriptions

Sideband Signals

The sideband signals consist of power, processor, and configuration signals. V_{CCO} for sideband signals is 1.80V.

- **JTAG:** The JTAG signals JTAG_TCK_C2M, JTAG_TMS_C2M, JTAG_TDI_C2M, and JTAG_TDO_M2C connect to the SOM Zynq UltraScale+ MPSoC JTAG port.
- **PS_REF_CLK:** The PS_REF_CLK input is connected to a 33.33 MHz oscillator.
- **PS_PAD_I/O:** The PS RTC inputs are connected to a 32.768 kHz crystal.
- **I2C:** The I2C signals I2C_SCK and I2C_SDA connect to an I2C master on MIO bank 500 of the SOM Zynq UltraScale+ MPSoC. The I2C I/O standard is 1.8V.
- **PS_MODE[3:0]:** The connector PS_MODE[3:0] pins connect to the SOM Zynq UltraScale+ MPSoC PS_MODE pins. All mode pins are pulled High to 1.8V through a resistor on the SOM.The carrier card boot mode is required to set the PS_MODE pins to a valid boot mode as defined in the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085). To configure a PS_MODE pin to a logic 1, the pin must be left floating, to configure a logic 0, the PS_MODE pin must be connected to GND with a 0Ω resistor.
- **PS_POR_L:** During power up, a voltage monitor keeps PS_POR_L asserted (Low) until all SOM power rails are stabilized. Afterward, PS_POR_L is released and the boot process starts. A carrier card can use PS_POR_L to reset any on-board devices. The carrier card can also force PS_POR_L Low to extend the reset during power on to reset the system at any time. The PS_POR_L signal drives the PS_POR_B signal on Zynq UltraScale+ MPSoC. This signal is pulled up to 1.8V through a 4.70 KΩ resistor on the SOM.
- **PS_SRST_C2M_L:** The PS_SRST_C2M_L pin connects to PS_SRST_B signal on the SOM Zynq UltraScale+ MPSoC. PS_SRST_B input signal to the Zynq UltraScale+ MPSoC is the system reset signal, and it is commonly used during debug. PS_SRST_C2M_L is pulled High to 1.8V on the SOM.

Power Management Signals

- **PWROFF_ C2M_L:**
  - PWROFF_C2M_L is an active-Low signal to power down the SOM and pulled High to the +5V SOM input power rail.
  - When PWROFF_C2M_L is asserted, the SOM power regulators perform a full-power shutdown of the device following the correct regulator power-down sequence. This signal does not alert application software to the power shutdown.
  - Upon deassertion of PWROFF_C2M_L, the SOM power regulators initiate a power-on sequence.

  ***Note*:** Asserting PWROFF_C2M_L does not perform a software shutdown or notify the system of the shutdown. The power regulators will start to power down instantly. Use the MIO31_SHUTDOWN pin and PMU functionality to initiate a software shutdown.

- **PWRGD_LPD_M2C:** PWRGD_LPD_M2C is an active-High push-pull output signal from the SOM power system that indicates the power status of all SOM PS low-power domain (LPD) rails. PWRGD_LPD_M2C is pulled Low when inactive. When active, it sources the 5.0V rail on the SOM. A carrier card can use this signal to monitor LPD status.

- **PWRGD_FPD_M2C:** PWRGD_FPD_M2C is an active-High push-pull output signal from the SOM power system that indicates the power status of all SOM PS full-power domain (FPD) rails. PWRGD_FPD_M2C is pulled Low when inactive. When active, it sources the 5.0V rail on the SOM. A carrier card can use this signal to monitor FPD status.

  Note: The K26 SOM does not have split rails for LPD and FPD. PWRGD_LPD_M2C and PWRGD_FPD_M2C are tied together on the SOM.

- **PWRGD_PL_M2C:** PWRGD_PL_M2C is an active-High push-pull output signal from the SOM power system that indicates the power status of all SOM PL power rails. PWRGD_PL_M2C is pulled Low when inactive. When active, it sources the 5.0V rail on the SOM. A carrier card can use this signal to monitor PL power status.

- **VCCOEN_PS_M2C:** VCCOEN_PS_M2C is an active-High push-pull output signal from the SOM power system to enable the PS V_{CCO} rails that are supplied by the carrier card. VCCOEV_PS_M2C is pulled Low when inactive. When active, it sources the 5.0V rail on the SOM. A carrier card can use this signal as an indication to turn power on for all PS peripherals.

- **VCCOEN_PL_M2C:** VCCOEN_PL_M2C is an active-High push-pull output signal from the SOM power system to enable the PL V_{CCO} rails that are supplied by the carrier card. VCCOEN_PL_M2C is pulled Low when inactive. When active, it sources the 5.0V rail on the SOM. A carrier card can use this signal as an indication to turn power on for all PL peripherals.

MIO Banks

- MIO banks 501 and 502 signals are accessible through the SOM240_1 connector.
- MIO bank 501 contains the MIO[51:26] pins.

  Note: The MIO[34:32] pins of bank 501 are reserved for the MPSoC PMU processor for power management functions, they are not connected to the SOM240_1 connector.

- MIO bank 502 contains the MIO[77:52] pins.
- The maximum data rate supported on MIO signals is 250 Mb/s.

A carrier card is not required to deliver V_{CCO} to the MIO banks. The V_{CCO} for MIO banks 501 and 502 is fixed at 1.8V and is supplied by the K26 SOM.

Platform Management Unit Signals

- The platform management unit (PMU) processor supports up to twelve GPIO pins that are configurable within MIO bank 501. MIO[31:26] can be configured as PMU inputs, and MIO[37:35] can be configured as PMU outputs.

  Note: MIO[34:32] are reserved on the K26 SOM for power management functions.

- The PMU GPIOs are used for a variety of critical systems functions like watchdog timers and power management related signals.
- When not used by the PMU, these signals can be used as regular MIO pins.

PS-GTR Transceivers

- PS-GTR transceivers are accessible through the SOM240_1 connector.

- GTR_DP[3:0]_M2C_P/N pins are transmit signals from the MPSoC.
- GTR_DP[3:0]_C2M_P/N pins are receive signals to the MPSoC.
- GTR_REFCLK[3:0]_P/N pins are REFCLKs inputs to the MPSoC.
- PS-GTR transceivers support a maximum transfer rate of 6 Gb/s over each lane.
- The carrier cards must supply the appropriate clock signals as required by the application.
- The PS-GTR transceivers support the following protocols:
  - PCIe Gen1/2
  - Serial ATA (SATA) 3.1
  - USB 3.0
  - DisplayPort 1.2
  - 10M/100M/1G Ethernet MAC (GEM)

HPIO: HPA, HPB, and HPC Banks

This section describes the high-performance I/O (HPIO) banks. The HPIO bank HPA (bank 66) is accessible through the SOM240_1 connector. The HPIO banks HPB (bank 65) and HPC (bank 64) are accessible through the SOM240_2 connector.

- All signals in the HPIO banks are routed as differential pairs. Each HPIO bank has a separate differential global clock input, namely HPA_CLK0_P/N, HPB_CLK0_P/N, and HPC_CLK0_P/N.
- The maximum data rate supported on HPIO signals is 2.5 Gb/s.
- V_{CCO} for the HP(x) bank is supplied by the carrier card through the VCCO_HP(x) pins where x = A, B, C.

HPIO bank connections are listed in the following table.

Table 14: **HPIO Bank Connections**

HPIO Bank	Connector	HPIO Signals	Clock-capable Pins	V_{CCO}
HPA bank 66	SOM240_1	HPA[14:00]_P/N, HPA_CLK0_P/N	HPA_CLK0_P/N	VCCO_HPA
HPB bank 65	SOM240_2	HPB[19:00]_P/N, HPB_CLK0_P/N	HPB_CLK0_P/N	VCCO_HPB
HPC bank 64	SOM240_2	HPC[19:00]_P/N, HPC_CLK0_P/N	HPC_CLK0_P/N	VCCO_HPC

MIPI Support

The differential signal pairs in HPIO banks HPA, HPB, and HPC are organized to support MIPI links with up to four lanes. A four lane MIPI link requires five differential HPIO signals, with the first signal pair supporting a clock-capable signal pair. Bank HPA can support three MIPI links. Banks HPB and HPC can support four MIPI links each. The following table lists the MIPI links.

Table 15: **Bank Organization**

	CLK	CSI0	CSI1	CSI2	CSI3
MIPIA0	HPA00_CC	HPA01	HPA02	HPA03	HPA04
MIPIA1	HPA05_CC	HPA06	HPA07	HPA08	HPA09
MIPIA2	HPA10_CC	HPA11	HPA12	HPA13	HPA14
MIPIB0	HPB00_CC	HPB01	HPB02	HPB03	HPB04
MIPIB1	HPB05_CC	HPB06	HPB07	HPB08	HPB09
MIPIB2	HPB10_CC	HPB11	HPB12	HPB13	HPB14
MIPIB3	HPB15_CC	HPB16	HPB17	HPB18	HPB19
MIPIC0	HPC00_CC	HPC01	HPC02	HPC03	HPC04
MIPIC1	HPC05_CC	HPC06	HPC07	HPC08	HPC09
MIPIC2	HPC10_CC	HPC11	HPC12	HPC13	HPC14
MIPIC3	HPC15_CC	HPC16	HPC17	HPC18	HPC19

HDIO: HDA, HDB, and HDC Banks

This section describes the high-density I/O (HDIO) banks. The HDIO bank HDA (bank 45) is accessible through the SOM240_1 connector. HDIO banks HDB (bank 43) and HDC (bank 44) are accessible through the SOM240_2 connector.

- The HDA bank supports 21 single-ended signals HDA[20:0]. Three signals (HDA00_CC, HDA08_CC, and HDA16_CC) are clock-capable inputs available on the MPSoC.
- The HDB and HDC bank supports 24 single-ended signals HDx[23:0]. Three signals (HDx00_CC, HDx08_CC, and HDx16_CC) are clock-capable inputs available on the MPSoC.
- The maximum data rate supported on HDIO signals is 250 Mb/s.
- V_{CCO} for the HD(x) bank is supplied by the carrier card through the VCCO_HD(x) pins where x = A, B, or C.

HDIO bank connections are listed in the following table.

Table 16: **HDIO Bank Connections**

HDIO Bank	Connector	HDIO Signals	Clock-capable Pins	V_{CCO}
HDA bank 45	SOM240_1	HDA[20:00]	HDA00, HDA08, HDA16	VCCO_HDA
HDB bank 43	SOM240_2	HDB[23:00]	HDB00, HDB08, HDB16	VCCO_HDB
HDC bank 44	SOM240_2	HDC[23:00]	HDC00, HDC08, HDC16	VCCO_HDC

GTH Transceivers

- The PL GTH transceiver lanes on bank 224 are accessible through the SOM240_2 connector.
- The GTH_DP[0:3]_M2C_P/N pins are transmit signals from the MPSoC.
- The GTH_DP[3:0]_C2M_P/N pins are receive signals to the MPSoC.
- The GTH_REFCLK[0:1]_P/N pins are REFCLK inputs to the MPSoC.
- GTH transceivers support a maximum transfer rate of 12.5 Gb/s over each lane.
- The carrier cards must supply REFCLKs to the GTH_REFCLK[0:1]_P/N pins on the SOM240_2 connector.

See the *UltraScale Architecture GTH Transceivers User Guide* (UG576) for more information on the GTH transceivers.

Power Management and Sequencing

The main power supply for the K26 SOM is a single +5V power rail that is supplied by the carrier card. The V_{CCO} power rails for the PL HPIO and HDIO banks are also powered by the carrier card. The carrier card can also supply an external battery power rail to the VCC_BATT pin for RTC battery-backup power.

SOM Connector Power Pins

The following table lists all power rails required for the proper operation of the K26 SOM. The carrier card designed for your application should provide these power rails based on the required peripheral I/O voltage. These supplies must be intentionally sequenced as outlined in the Power Sequencing section. Connect the VCCO pins of unused banks together and to the same potential (GND or a valid V_{CCO} voltage).

Table 17: **SOM Power Rails**

Power Rail Name	Supported Voltage Range	Maximum Current	Description
V_{CC_SOM}	5V (4.75V – 5.25V) 50 mV p-p maximum noise	4A	Main power input to the SOM. Supplies power to on-board power regulators.
V_{CC_BATT}[1]	1.20 – 1.50V	150 nA – 3650 nA	External battery input for the RTC
V_{CCO_HPA}	1.00V – 1.80V	1.0A	Voltage rail for HPIO bank 66
V_{CCO_HPB}	1.00V – 1.80V	1.0A	Voltage rail for HPIO bank 65
V_{CCO_HPC}	1.00V – 1.80V	1.0A	Voltage rail for HPIO bank 64
V_{CCO_HDA}	1.20V – 3.30V	1.0A	Voltage rail for HDIO bank 45
V_{CCO_HDB}	1.20V – 3.30V	1.0A	Voltage rail for HDIO bank 43
V_{CCO_HDC}	1.20V – 3.30V	1.0A	Voltage rail for HDIO bank 44

Notes:

1. See *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925) for recommended device conditions when RTC is enabled or disabled.

For the selected I/O type, the supply voltage tolerance at the SOM connector must be within +3%/–2%. For example:

- If an HPIO bank is configured for the LVDS (1.8V) standard, the V_{CCO} at the SOM connector pin must be within 1.764V–1.854V.
- If an HDIO bank is configured for the LVDS_25 standard, the V_{CCO} at the SOM connector pin must be within 2.450V–2.575V.

Power Sequencing

The carrier card power management circuit for your application must use the following sequence to power on the K26 SOM. Your carrier card supplies the +5V SOM power rail (V_{CC_SOM}).

1. When the V_{CC_SOM} voltage level is within the specified range, the carrier card deasserts the POWER_OFF_C2M_L signal.

2. The K26 SOM initiates onboard power sequencing.
3. The K26 SOM asserts the VCCOEN_PS_M2C signal, indicating to the carrier card to turn on the supply rails for the PS peripheral devices.
4. The K26 SOM asserts the VCCOEN_PL_M2C signal, indicating to the carrier card to turn on the supply rails for the PL peripheral devices as well as all V_{CCO} rails for the HPIO and HDIO banks.

PL Power Domain Control

The K26 provides a mechanism to dynamically power up or down the PL power domain through the on-board PMICs. To change the state of the PL power domain, use an I2C register write to the PL power control register in the PL power domain monitor IC. The PL power state register and value for toggling the on/off state is defined in the following table.

Table 18: **PL Power State Register**

PL Power State	Register	Value
Off	0x08	0x00
On	0x08	0x3E

A reference implementation is available in the `som-pwrctl` function of the Xilinx `xmutil` tool suite available on GitHub under som-pwerctl.

Software Controlled Power Down

The K26 SOM provides a mechanism to power down all SOM power rails from software via the Zynq® UltraScale+™ MPSoC power management unit (PMU). The MIO34 pin on the Zynq® UltraScale+™ MPSoC is connected to the power shutdown request of the SOM power sequencer on the board. The power sequencer device sequences down all supplies when it observes a transition from a logic-High to a logic-Low state. On power up, the power sequencer ignores the shutdown request signal until after the POR_B is released. When using the software commanded shutdown feature, the MIO34 signal should be enabled and mapped to the PMU subsystem in the Vivado configuration for your design. In released Vivado designs and PMUFW, the MIO34 signal is mapped to and driven by the PMU IOMODULE GPO1 register, bit 2 (GPO1[2]). Because this pin is edge sensitive and the MIO multiplexer mappings on the Zynq® UltraScale+™ MPSoC are reset when the device is reset (POR_B or SRST), the PMU firmware must include the PMU build-time configuration CONNECT_PMU_GPO_2_VAL= 0, to avoid glitches on the MIO34 signal during reset cycles. When not using the software commanded shutdown feature, the MIO34 signal should not be configured and assigned to any PCW functionality in the Vivado hardware project. The MIO34 signal is left in reset as a tri-state voltage with external pull-up. For additional PMU firmware guidance, see the Kria K26 SOM Wiki.

Absolute Maximum Specifications

The following tables describe the absolute maximum specifications.

Table 19: **Absolute Maximum Ratings**

Symbol	Description[1, 2]	Min	Max	Units
V_{CC_SOM}	Primary supply voltage for the SOM	–0.500	6.000	V

Table 19: **Absolute Maximum Ratings** *(cont'd)*

Symbol	Description[1, 2]	Min	Max	Units
V_{CCO}	Output drivers supply voltage for HD I/O banks (HDA, HDB, HDC)	–0.500	3.400	V
	Output drivers supply voltage for HP I/O banks (HPA, HPB, HPC)	–0.500	2.000	V
V_{IN}[3, 4]	I/O input voltage for HD I/O banks	–0.550	V_{CCO} + 0.550	V
	I/O input voltage for HP I/O banks	–0.550	V_{CCO} + 0.550	V
	I/O input voltage for MIO (PS I/O)	–0.550	2.350	V
V_{CC_BATT}	PS battery-backed RAM and battery-backed real-time clock (RTC) supply voltage	–0.500	2.000	V
GTH Transceivers[5, 6]				
$V_{MGTREFCLK}$	Transceiver reference clock absolute input voltage	–0.500	1.300	V
V_{IN}	Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage	–0.500	1.200	V
Temperature[7]				
T_{STG}	Storage temperature (ambient)	–65	150	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For more information on absolute ratings see *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925).
3. The lower absolute voltage specification always applies.
4. For I/O operation, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
5. For more information on supported GTH transceiver terminations see the *UltraScale Architecture GTH Transceivers User Guide* (UG576).
6. DC coupled operation is not supported for RX termination = programmable.
7. For thermal considerations, see the *Kria K26 SOM Thermal Design Guide* (UG1090) and the Power Design Manager (PDM) tool (download at www.xilinx.com/power).

Vivado Device Model

This chapter specifies where to locate the Vivado® device model for the Zynq UltraScale+ MPSoC used on a Kria K26C SOM or a Kria K26I SOM.

Commercial Grade (K26C) Specifications

The commercial grade Kria K26C SOM (K26C) uses a standard Zynq UltraScale+ MPSoC with the speed/temperature grade of -2LE (V_{CCINT} = 0.72V). The *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925) lists the specifications for the -2 speed grade when V_{CCINT} = 0.72V that is applicable to the -2LE (V_{CCINT} = 0.72V) devices.

Industrial Grade (K26I) Specifications

The industrial grade Kria K26I SOM (K26I) uses an exclusive Zynq UltraScale+ MPSoC with the speed/temperature grade of -2LI (V_{CCINT} = 0.72V). This device is not specified in the *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925). For some of the Zynq UltraScale+ MPSoC blocks, the -2LI (V_{CCINT} = 0.72V) and -2LE (V_{CCINT} = 0.72V) have the same switching characteristics. For the switching characteristics of -2LI that are the same as the -2LE, refer to the *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925). For switching characteristics that are not the same as those in the data sheet and are relevant to the K26I SOM, refer to the following tables.

Table 20: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	-2LI Speed Grade and Operating Voltage (V_{CCINT} = 0.72V)	Units
Maximum Frequency			
$F_{MAX\_WF\_NC}$	Block RAM (WRITE_FIRST and NO_CHANGE modes)	516	MHz
F_{MAX_RF}	Block RAM (READ_FIRST mode)	495	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC	516	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration without PIPELINE	460	MHz
	Block RAM and FIFO in ECC configuration with PIPELINE and Block RAM in WRITE_FIRST or NO_CHANGE mode	516	MHz
T_{PW}[1]	Minimum pulse width	578	ps
Block RAM and FIFO Clock-to-Out Delays			
T_{RCKO_DO}	Clock CLK to DOUT output (without output register)	1.53	ns, Max
$T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (with output register)	0.44	ns, Max

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

Table 21: **UltraRAM Switching Characteristics**

Symbol	Description	-2LI Speed Grade and Operating Voltage (V_{CCINT} = 0.72V)	Units
Maximum Frequency			
F_{MAX}	UltraRAM maximum frequency with OREG_B = True	495	MHz
$F_{MAX\_ECC\_NOPIPELINE}$	UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = True	303	MHz
$F_{MAX\_NOPIPELINE}$	UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = False	389	MHz
T_{PW}[1]	Minimum pulse width	832	ps
T_{RSTPW}	Asynchronous reset minimum pulse width. One cycle required	1 clock cycle	

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

Table 22: **DSP48 Slice Switching Characteristics**

Symbol	Description	-2LI Speed Grade and Operating Voltage (V_{CCINT} = 0.72V)[1]	Units
Maximum Frequency			
F_{MAX}	With all registers used	600	MHz
F_{MAX_PATDET}	With pattern detector	524	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	413	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	371	MHz
$F_{MAX\_PREADD\_NOADREG}$	Without ADREG	423	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	304	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	280	MHz

Notes:

1. For devices operating at the lower power V_{CCINT} = 0.72V voltages, DSP cascades that cross the clock region center might operate below the specified F_{MAX}.

Table 23: **GTH Transceiver Performance**

Symbol	Description	Output Divider	-2LI Speed Grade and Operating Voltage (V_{CCINT} = 0.72V)[1]		Units
F_{GTHMAX}	GTH maximum line rate		10.3125		Gb/s
F_{GTHMIN}	GTH minimum line rate		0.5		Gb/s
			Min	**Max**	
$F_{GTHCRANGE}$	CPLL line rate range[2]	1	4	8.5	Gb/s
		2	2	4.25	Gb/s
		4	1	2.125	Gb/s
		8	0.5	1.0625	Gb/s
		16	N/A		Gb/s
			Min	**Max**	
$F_{GTHQRANGE1}$	QPLL0 line rate range[3]	1	9.8	10.3125	Gb/s
		2	4.9	8.15	Gb/s
		4	2.45	4.075	Gb/s
		8	1.225	2.0375	Gb/s
		16	0.6125	1.0118	Gb/s
			Min	**Max**	
$F_{GTHQRANGE2}$	QPLL1 line rate range[4]	1	8.0	10.3125	Gb/s
		2	4.0	6.5	Gb/s
		4	2.0	3.25	Gb/s
		8	1.0	1.625	Gb/s
		16	0.5	0.8125	Gb/s
			Min	**Max**	
$F_{CPLLRANGE}$	CPLL frequency range		2	4.25	GHz
$F_{QPLL0RANGE}$	QPLL0 frequency range		9.8	16.375	GHz

Table 23: **GTH Transceiver Performance** *(cont'd)*

Symbol	Description	Output Divider	-2LI Speed Grade and Operating Voltage (V_{CCINT} = 0.72V)[1]		Units
$F_{QPLL1RANGE}$	QPLL1 frequency range		8	13	GHz

Notes:

1. The GTH transceiver line rates on the K26I SOMsupports data rates up to 12.5 Gb/s.
2. The values listed are the rounded results of the calculated equation (2 × CPLL_Frequency)/Output_Divider.
3. The values listed are the rounded results of the calculated equation (QPLL0_Frequency)/Output_Divider.
4. The values listed are the rounded results of the calculated equation (QPLL1_Frequency)/Output_Divider.

Table 24: **GTH Transceiver User Clock Switching Characteristics**

Symbol	Description[1]	Data Width Conditions (Bit)		-2LI Speed Grade and Operating Voltage (V_{CCINT} = 0.72V)[2]	Units
		Internal Logic	Interconnect Logic		
$F_{TXOUTPMA}$	TXOUTCLK maximum frequency sourced from OUTCLKPMA			322.266	MHz
$F_{RXOUTPMA}$	RXOUTCLK maximum frequency sourced from OUTCLKPMA			322.266	MHz
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	MHz
F_{TXIN}	TXUSRCLK[3] maximum frequency	16	16, 32	322.266	MHz
		32	32, 64	322.266	MHz
		20	20, 40	257.813	MHz
		40	40, 80	257.813	MHz
F_{RXIN}	RXUSRCLK[3] maximum frequency	16	16, 32	322.266	MHz
		32	32, 64	322.266	MHz
		20	20, 40	257.813	MHz
		40	40, 80	257.813	MHz
F_{TXIN2}	TXUSRCLK2[3] maximum frequency	16	16	322.266	MHz
		16	32	161.133	MHz
		32	32	322.266	MHz
		32	64	161.133	MHz
		20	20	322.266	MHz
		20	40	161.133	MHz
		40	40	257.813	MHz
		40	80	128.906	MHz

Table 24: **GTH Transceiver User Clock Switching Characteristics** *(cont'd)*

Symbol	Description[1]	Data Width Conditions (Bit)		-2LI Speed Grade and Operating Voltage (V_{CCINT} = 0.72V)[2]	Units
		Internal Logic	Interconnect Logic		
F_{RXIN2}	RXUSRCLK2[3] maximum frequency	16	16	322.266	MHz
		16	32	161.133	MHz
		32	32	322.266	MHz
		32	64	161.133	MHz
		20	20	257.813	MHz
		20	40	128.906	MHz
		40	40	257.813	MHz
		40	80	128.906	MHz

Notes:

1. Clocking must be implemented as described in *UltraScale Architecture GTH Transceivers User Guide* (UG576).
2. For speed grade -2LI (V_{CCINT} = 0.72V), a 16-bit and 20-bit internal data path can only be used for line rates less than 5.15625 Gb/s.
3. When the gearbox is used, these maximums refer to the XCLK. For more information, see the *UltraScale Architecture GTH Transceivers User Guide* (UG576).

Device Firmware

The K26 SOM includes two memory devices that are used for nonvolatile storage of firmware and an EEPROM for SOM device configuration information.

Application-agnostic reference implementations of the SOM boot firmware and fixed peripheral board support package (BSP) are made available in the Xilinx tools and software repositories. The references include:

- First-stage boot loader (FSBL)
- Arm trusted firmware (ATF)
- U-Boot
- Platform management unit (PMU)

The reference implementations are available for you to use and modify for your unique product implementation.

EEPROM

The K26 SOM EEPROM is pre-programmed during manufacturing and provides device configuration, identification, and manufacturing data. The EEPROM content is protected as a read-only interface and organized per the IPMI specification. See the information on EEPROM data mapping in the *IPMI Platform Management FRU Information Storage Definition v1.0*, Revision 1.3, March 24, 2015.

The K26 SOM EEPROM includes the IPMI records defined in the following table. The addresses are expressed in EEPROM physical address offsets.

Table 25: **EEPROM Content Summary**

Record Area	IPMI Record Type	Record Start	Record End
Header and board area record	Board area record	0x00	0x67
DC load multi-record	OEM multi-record	0x68	0x79
MAC address multi-record	OEM multi-record	0x7A	0x88
Memory configuration multi-record	OEM multi-record	0x9B	0xF6

The following table defines the specific content of the EEPROM.

Table 26: **EEPROM Content**

Address	Byte Length	Format	Description
Header and Board Area Record			
0	1	Binary	Version
1	1	Binary	Internal user area
2	1	Binary	Chassis information area
3	1	Binary	Board area
4	1	Binary	Product information area
5	1	Binary	Multi-record area
6	1	Binary	Pad
7	1	Binary	Checksum
8	1	Binary	Version
9	1	Binary	Length
A	1	Binary	Language code
B	3	Binary	Manufacturing date starting on 1/1/1996 in minutes
E	1	Binary	Board manufacturer type-length
F	6	ASCII	Board manufacturer is Xilinx
15	1	Binary	Board product name type-length
16	16	ASCII	Board product name
26	1	Binary	Board serial type-length
27	16	ASCII	Board serial number (any printable ASCII character)
37	1	Binary	Board part number type-length
38	9	ASCII	Board part number
41	1	Binary	FRU file ID type-length
42	1	ASCII	FRU file ID (00)
43	1	Binary	Revision type-length
44	8	ASCII	Revision number
4C	1	Binary	PCIe information type/length byte
4D	8	Binary	PCIe information
55	1	Binary	UUID type-length byte
56	16	Binary	UUID
66	1	Binary	End of field
67	1	Binary	Board area checksum

Table 26: **EEPROM Content** *(cont'd)*

Address	Byte Length	Format	Description
DC Load Multi-record			
68	1	Binary	Record type (DC load)
69	1	Binary	Record format
6A	1	Binary	Length
6B	1	Binary	Record checksum
6C	1	Binary	Header checksum
6D	1	Binary	Output number
6E	2	Binary	Nominal voltage (10 mV): V_{CC_SOM} (5V)
70	2	Binary	Specified minimum voltage (10 mV)
72	2	Binary	Specified maximum voltage (10 mV)
74	2	Binary	Specified ripple and noise pk-pk 10 Hz to 30 MHz (mV)
76	2	Binary	Minimum current load (mA)
78	2	Binary	Maximum current load (mA)
MAC Address Multi-record			
7A	1	Binary	Record type (OEM)
7B	1	Binary	Type
7C	1	Binary	Length
7D	1	Binary	Record checksum
7E	1	Binary	Header checksum
7F	3	Binary	Xilinx internet assigned numbers authority (IANA) ID
82	1	Binary	Version number
83	6	Binary	MAC ID 0
Memory Configuration Multi-record			
9B	1	Binary	Record type (OEM)
9C	1	Binary	Record format
9D	1	Binary	Length
9E	1	Binary	Record checksum
9F	1	Binary	Header checksum
A0	3	Binary	Xilinx IANA ID
A3	8	ASCII	Memory
AB	12	ASCII	Primary boot device memory definition
B7	1	Binary	Memory type field end
B8	8	ASCII	Memory
C0	12	ASCII	SOM secondary boot device memory
CC	1	Binary	Memory type field end
CD	8	ASCII	Memory
D5	12	ASCII	SOM PS DDR memory
E1	1	Binary	Memory type field end
E2	8	ASCII	Memory
EA	12	ASCII	SOM PL DDR memory
F6	1	Binary	Memory type field end

QSPI

The K26 includes a 512 Mb (64 MB) QSPI flash memory device. It supports interface clock speeds up to 40 MHz, and can be used as the primary boot device for the MPSoC processing subsystem. The QSPI device is left blank during SOM manufacturing.

eMMC

The K26 SOM includes a 16 GB eMMC flash memory device. It supports interface clock speeds up to 50 MHz, and can be used as the primary or secondary boot device for the MPSoC processing subsystem. The eMMC device is left blank during SOM manufacturing.

Mechanical and Thermal

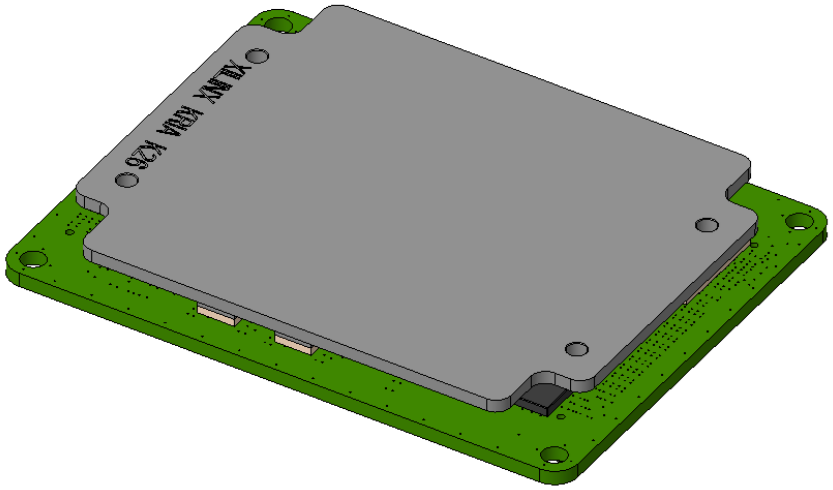
The production K26 SOM is available in both commercial and industrial temperature grades. The temperature specification is defined relative to the junction temperature of the MPSoC as measured by the integrated System Monitor. All the other components on the SOM should remain within their operating limits as long as temperature is maintained in the MPSoC. Your design is expected to have a thermal solution connected to the integrated heat spreader, this is to maintain the operating temperature within these limits under the operating conditions (i.e., ambient temperature, airflow, etc.) of your system.

Table 27: **K26 SOM Specifications**

K26 SOM	Operating Temperature
Commercial grade: K26C SOM	0°C to 85°C (as measured at MPSoC junction temperature)
Industrial grade: K26I SOM	–40°C to 100°C (as measured at MPSoC junction temperature)

The K26 SOM is supplied with an aluminum heat spreader. This heat spreader makes full contact with all the high-power active components, including the MPSoC, DDR4, eMMC, and power regulators. The primary function of the heat spreader is to transfer the non-uniform heat distribution of the module that is generated on the PCB assembly to the heat spreader, making the heat flux more uniform and spread over a larger surface area. This allows for more efficient heat transfer out of the package to an attached cooling device and simplifies thermal design. The user-defined system cooling solutions should be designed to directly attach to the heat spreader.

Figure 3: **K26 SOM**



IMPORTANT! *The thermal solution on your system must provide adequate cooling to maintain all the components on the PCB (including the K26 SOM) at below the maximum temperature specifications as detailed in Table 27: K26 SOM Specifications.*

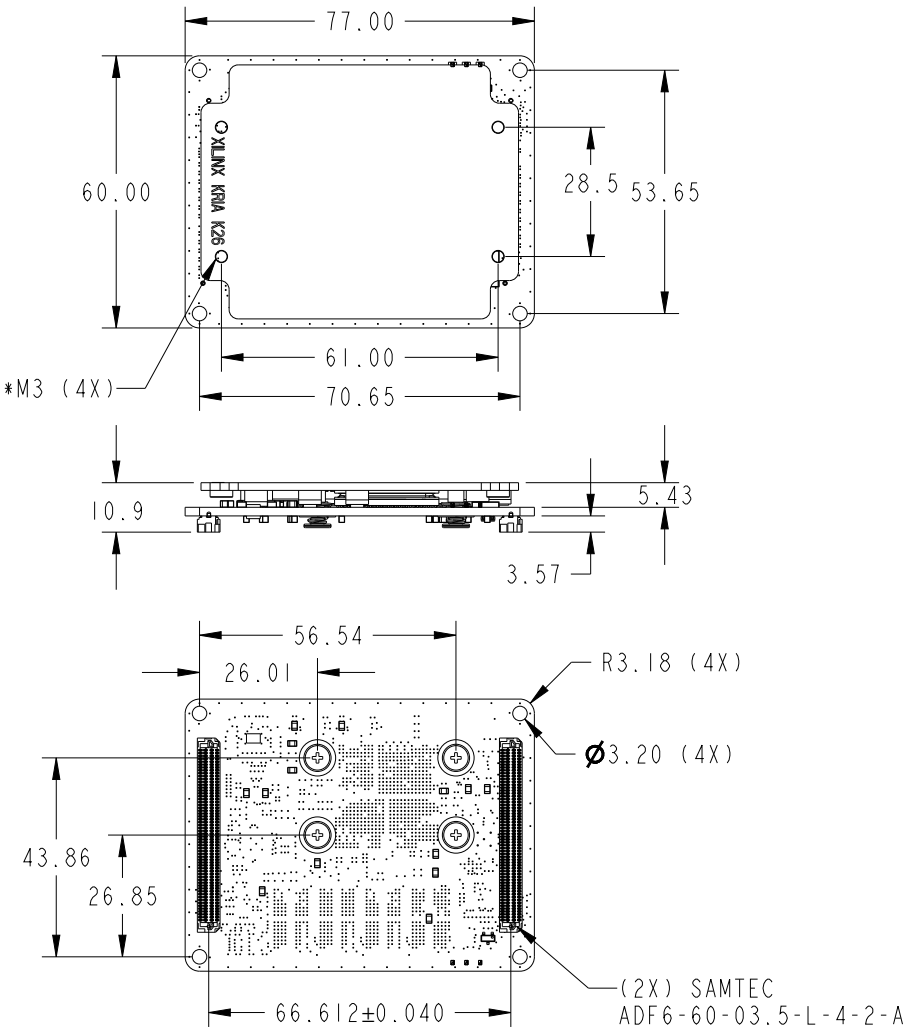
Mechanical Dimensions

The following table and figures define the mechanical specifications of the K26 SOM. The following mechanical drawing provides the detailed dimensions of the SOM.

Table 28: **K26 SOM Mechanical Specifications**

Parameter	Specification
SOM length	77 mm
SOM width	60 mm
SOM height (without a thermal solution)	10.9 mm
Mass	58 grams

Figure 4: **K26 SOM Dimensions**



Notes:

1. All dimensions in mm.
2. Mass: 58G.
3. Mounting holes (*) are reserved for customer's cooling installation.
4. Tolerance unless otherwise specified: ±0.13.

X26219-031522

The K26 SOM 3D CAD files are available for your platform or carrier design reference. These files are design aides in your cooling mechanical design, system assembly interference and clearance reviews, and board-to-board (B2B) connector placement alignment checks.

SOM PCB Assembly

Figure 5: **Top PCBA Views**

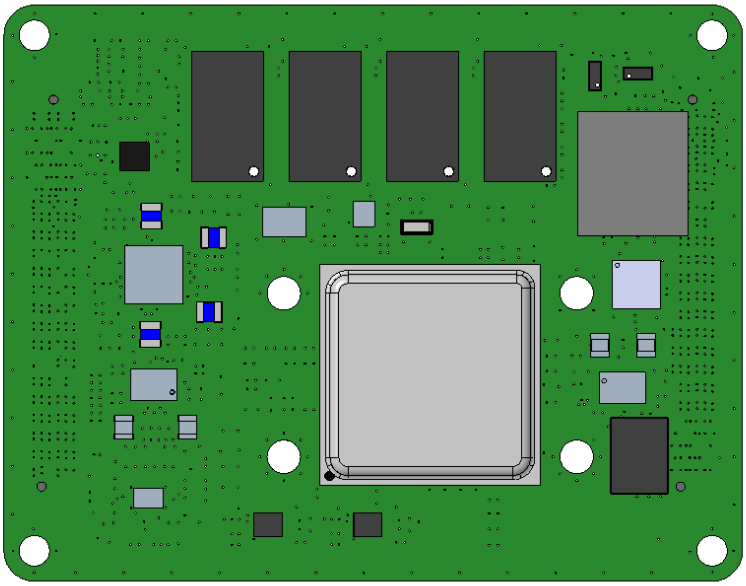
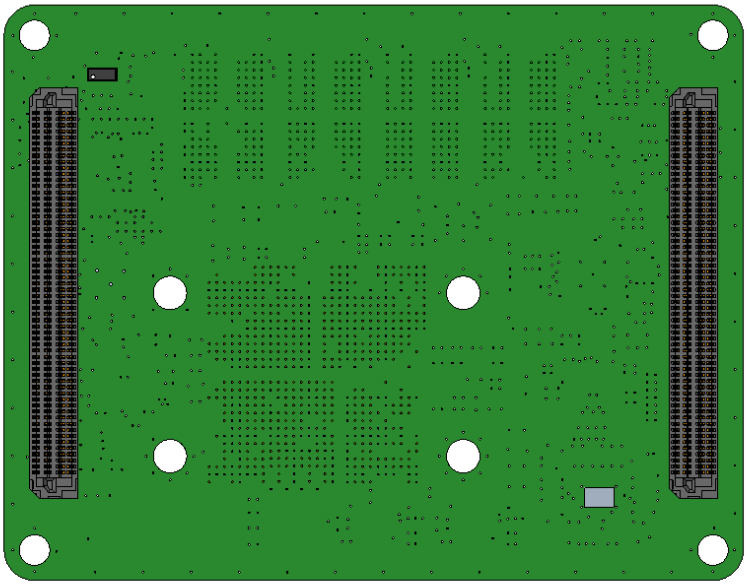


Figure 6: **Bottom PCBA Views**



Thermal

Operating Environment and Storage Temperature Conditions

The following table defines the temperature and humidity conditions for device operation and storage.

Table 29: **Operating Environment and Storage Temperatures and Humidity Conditions**

Specification	Condition
Operating environment temperature	Use case dependent
Storage temperature	–40°C to 75°C
Operating humidity, non-condensing	8% to 90%, and a dew point of –12°C
Storage humidity, non-condensing	5% to 95%

Thermal Design

The K26 SOM is built with a thermal interface plate that for most deployed applications is not a full thermal solution. It is your responsibility to integrate the SOM into a system-level thermal solution that can dissipate the application-specific thermal load of the SOM while maintaining it within specified temperature limits. The *Kria K26 SOM Thermal Design Guide* (UG1090) and the Power Design Manager (PDM) tool (download at www.xilinx.com/power) support the integration of the SOM into your application system thermal and mechanical solutions including thermal modeling and detailed design specifications.

K26 Reliability

The following table captures a summary of the reliability testing completed on the K26 SOM. All reliability testing was done with the production SOM assembly inclusive of the circuit card assembly and aluminum heat spreader. For the full K26 SOM reliability and qualification report request access to the *Kria SOM Qualification Report Lounge*.

Table 30: **Reliability Testing**

Reliability Test	K26C SOM (Commercial)	K26I SOM (Industrial)
Temperature cycling	JESD22-A104, Condition J (0°C to 100°C)	JESD22-A104, Condition T (–40°C to 100°C)
Power cycling	Ta = 50°C, RH = 80%; 55 min ON, 5 min OFF	Ta = 50°C, RH = 80%; 55 min ON, 5 min OFF
Strife power cycling	Power cycling, 0°C; 1 min ON, 1 min OFF	Power cycling, –40°C; 1 min ON, 1 min OFF
Temperature and humidity	Ta = 85°C, RH = 85%	Ta = 85°C, RH = 85%
Mechanical vibration	IEC 60068-2-64, 1.9 Grms	IEC 60068-2-64, 5.04 Grms
Mechanical shock	IEC 60068-2-27, 40 G	IEC 60068-2-27, 100 G
Connector insertion life	Room temperature, all the following connectors: dual 240-pin connectors.	Room temperature, all the following connectors: dual 240-pin connectors.

Notes:

1. Samtec has performed connector level testing following EIA-364-09C, while Xilinx has performed mechanical wellness testing of the bond between the PCB and the mating connector. Refer to the *Samtec website* for more information on connector reliability specifications.

Regulatory Compliance Statements

Safety

The following safety standards apply to all products listed in this document.

IEC 62368-1, 2nd Edition, 2014/A11:2017, *Information technology equipment – Safety, Part 1: General requirements*

EN 62368-1, 2nd Edition, 2014/A11:2017, *Information technology equipment – Safety, Part 1: General requirements*

FCC Class A Products

The following is a list of the products covered by this data sheet:

- SM-K26-XCL2GC
- SM-K26-XCL2GI
- SM-K26-XCL2GC-ED
- SM-K26-XCL2GI-ED

Regulatory Compliance Statements are valid for the production version of the K26 SOM.

Safety Compliance

The following safety standards apply to all products listed in this document.

UL 62368-1, 2nd Edition, 2014/A11:2017 (Information Technology Equipment - Safety - Part 1: General Requirements)

UL 62368-1, 2nd Edition, 2014-12-01, *Information technology equipment – Safety, Part 1: General requirements*

CSA C22.2 No. 60950-1-07, 2nd Edition, 2014/A11:2017 (Information Technology Equipment - Safety - Part 1: General Requirements)

CSA C22.2 No. 62368-1-14, 2nd Edition, 2014-12-01, *Information Technology Equipment – Safety, Part 1: General Requirements*

EU LVD Directive 2014/35/EU

EN/IEC-62368-12014/A11:2017

EN 62368-1, 2nd Edition, 2014/A11:2017, *Information technology equipment – Safety, Part 1: General requirements*

IEC 62368-1, 2nd Edition, 2014/A11:2017, *Information technology equipment – Safety, Part 1: General requirements*

EMC Compliance

Class A Products

The following standards apply:

- FCC Part 15 – Radiated & Conducted Emissions (USA)
- CAN ICES-3(A)/NMB-3(A) – Radiated & Conducted Emissions (Canada)
- CISPR 32 – Radiated & Conducted Emissions (International)
- EN55032: 2015 – Radiated & Conducted Emissions (European Union)
- EN55035:2017 – Immunity (European Union)
- EMC Directive 2014/30/EU
- VCCI (Class A)– Radiated & Conducted Emissions (Japan)
- CNS13438 – Radiated & Conducted Emissions (Taiwan)
- CNS 15663 - RoHS (Taiwan)
- AS/NZS CISPR 32 – Radiated and Conducted Emissions (Australia/New Zealand)
- Article 58-2 of Radio Waves Act, Clause 3 (Korea)

Regulatory Compliance Markings

When required, these products are provided with the following product certification markings:

- UL Listed Accessories Mark for the USA and Canada
- CE mark
- FCC markings
- VCCI marking
- Australian RCM mark
- Korea MSIP mark
- Taiwan BSMI mark
- German GS mark

FCC Class A User Information

The Class A products listed above comply with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

CAUTION! *This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at their own expense.*

ATTENTION! *Cet équipement a été testé et jugé conforme à la Class A digital device, conformément à la règle 15 du standard FCC. Ces limites sont conçues pour fournir des protections contre des interférences nuisibles lorsque l'équipement est utilisé dans un environnement commercial. Cet équipement génère, utilise et peut émettre des énergies de radio-fréquence et, s'il n'est pas installé et utilisé conformément aux instructions, peut nuire aux communications radio. L'exploitation de cet équipement dans une zone résidentielle est susceptible de causer des interférences nuisibles, auquel cas l'utilisateur peut être tenu de prendre des mesures adéquates à ses propres frais.*

VORSICHT! *Dieses Gerät wurde getestet und entspricht den Grenzwerten für digitale Geräte der Klasse A gemäß Teil 15 der FCC-Bestimmungen. Diese Grenzwerte bieten einen angemessenen Schutz gegen schädliche Interferenzen, wenn das Gerät in einer gewerblichen Umgebung betrieben wird. Dieses Gerät erzeugt und verwendet Hochfrequenzenergie und kann diese abstrahlen. Wenn es nicht gemäß den Anweisungen installiert und verwendet wird, kann dies Funkstörungen verursachen. Der Betrieb dieses Geräts in einem Wohngebiet kann schädliche Interferenzen verursachen. In diesem Fall muss der Benutzer die Interferenz auf eigene Kosten beheben.*

CAUTION! *If the device is changed or modified without permission from Xilinx, the user may void their authority to operate the equipment.*

ATTENTION! *Si l'appareil est modifié sans l'autorisation de Xilinx, l'utilisateur peut annuler son abilité à utiliser l'équipement.*

VORSICHT! *Wenn das Gerät ohne Erlaubnis von Xilinx geändert wird, kann der Benutzer seine Berechtigung zum Betrieb des Geräts verlieren.*

Canadian Compliance (Industry Canada)

CAN ICES-3(A)/NMB-3(A)

RoHS Compliance

- RoHS Directive 2011/65/EU
- RoHS 3 Directive 2015/863
- SJ/T 11363-2006, 11364-2006, and GB/T 26572-2011 (China RoHS)

VCCI Class A Statement

この装置は、クラス A 情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。
この場合には使用者が適切な対策を構ずるよう要求されることがあります。 VCCI-A

KCC Notice Class A (Republic of Korea Only)

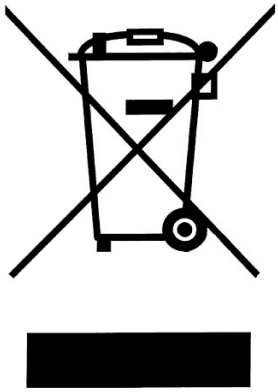
A급 기기 (업무용 방송통신기기) **CLASS A device** (commercial broadcasting and communication equipment	이 기기는 업무용(A급)으로 전자파적합등록을 한 기기이오니 판매자 또는 사용자는 이 점을 주의하시기 바라며, 가정외의 지역에서 사용하는 것을 목적으로 합니다. This device has been appoved by EMC registration. Distributors or users pay attention to this point. This device is usually aimed to be used in other area except at home

BSMI Class A Notice (Taiwan)

警告使用者:

此為甲類資訊技術設備，於居住環境中使用時，可能會造成射頻擾動，在此種情況下，使用者會被要求採取某些適對當的對策。

EU WEEE Logo



Manufacturer Declaration European Community

CE

Manufacturer Declaration

Xilinx declares that the equipment described in this document is in conformance with the requirements of the European Council Directives listed below:

- Low Voltage Directive 2014/35/EU
- EMC Directive 2014/30/EU
- RoHS 3 Directive 2011/65/EU, 2015/863
- China RoHS Declaration: Standards SJ/T 11363-2006, 11364-2006, and GB/T 26572-2011
- REACH Regulation 1907/2006
- POP Regulation 2019/1021

These products follow the provisions of the European Directive 2014/53/EU.

Dette produkt er i overensstemmelse med det europæiske direktiv 2014/53/EU.

Dit product is in navolging van de bepalingen van Europees Directief 2014/53/EU.

Tämä tuote noudattaa EU-direktiivin 2014/53/EU määräyksiä.

Ce produit est conforme aux exigences de la Directive Européenne 2014/53/EU.

Dieses Produkt entspricht den Bestimmungen der Europäischen Richtlinie 2014/53/EU.

Þessi vara stenst reglugerð Evrópska Efnahags Bandalagsins númer 2014/53/EU.

Questo prodotto è conforme alla Direttiva Europea 2014/53/EU.

Dette produktet er i henhold til bestemmelsene i det europeiske direktivet 2014/53/EU.

Este produto cumpre com as normas da Diretiva Européia 2014/53/EU.

Este producto cumple con las normas del Directivo Europeo 2014/53/EU.

Denna produkt har tillverkats i enlighet med EG-direktiv 2014/53/EU.

EN 55032 (CISPR 32 Class A) RF Emissions Control

EN 55035:2017 (CISPR 35) Electromagnetic compatibility of multimedia equipment – Immunity requirements

EN 62368-1, 2nd Edition, 2014/A11:2017 *Information technology equipment – Safety, Part 1: General Requirements*

EN 50581:2012 - Technical documentation for the assessment of electrical and electronic products with respect to the restriction of hazardous substances.

CAUTION! *In a domestic environment, Class A products could cause radio interference, in which case the user may be required to take adequate measures.*

ATTENTION! *Dans un environnement domestique, les produits de Classe A peuvent causer des interférences radio, auquel cas l'utilisateur peut être tenu de prendre des mesures adéquates.*

VORSICHT! *In einer häuslichen Umgebung können Produkte der Klasse A Funkstörungen verursachen. In diesem Fall muss der Benutzer möglicherweise geeignete Maßnahmen ergreifen.*

Responsible Party

Xilinx, Inc.
2100 Logic Drive, San Jose, CA 95124
United States of America
Phone: (408) 559-7778

References

These documents provide supplemental material useful with this guide:

1. *Kria K26 SOM Thermal Design Guide* (UG1090)
2. Power Design Manager (PDM) tool (download at www.xilinx.com/power)
3. *Power Design Manager User Guide* (UG1556)
4. *Kria SOM Carrier Card Design Guide* (UG1091)
5. *Zynq UltraScale+ Device Technical Reference Manual* (UG1085)
6. *Zynq UltraScale+ Device Packaging and Pinouts Product Specification User Guide* (UG1075)
7. *UltraScale Architecture GTH Transceivers User Guide* (UG576)
8. *UltraScale Architecture and Product Data Sheet: Overview* (DS890)
9. *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925)
10. *UltraScale Architecture SelectIO Resources User Guide* (UG571)
11. *UltraScale Architecture PCB Design User Guide* (UG583)
12. *Zynq UltraScale+ MPSoC: Software Developers Guide* (UG1137)

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
7/26/2022 Version 1.3	
General	Added reference to the REF-226081 Samtec connector throughout data sheet.
PL Power Domain Control	Added Software Controlled Power Down
Vivado Device Model	Added the new section that includes Commercial Grade (K26C) Specifications and Industrial Grade (K26I) Specifications.
3/15/2022 Version 1.2	
Functional Overview and Block Diagram	Updated the programmable logic in Figure 2: K26 SOM Block Diagram to remove unused blocks.
Functional Interfaces	Added physical location column to Table 2: Interfaces Summary and updated rest of section for clarity.
Processing System	Updated the section and the MIO Banks table.
Security Features	Removed PUF feature and updated TPM reset discussion.
Supported I/O Standards	Moved section and added power-up and configuration information.
Signal Naming Conventions	Added Table 9: Legend for Pin Types.
SOM240_1 Signal Names and Descriptions	Added the pin type column.
SOM240_2 Connector Pinout	Updated A4 description in the table.
SOM240_2 Signal Names and Descriptions	Added the pin type column.
Power Management Signals	Updated information about the PWRGD signals.
K26 Reliability	Added section.
FCC Class A Products	Updated the Safety Compliance section.

Section	Revision Summary
Manufacturer Declaration European Community	Updated the section.
References	Added links to the *Power Design Manager User Guide* (UG1556) and the Power Design Manager (PDM) tool (download at www.xilinx.com/power).
7/23/2021 Version 1.1	
Functional Overview and Block Diagram	Clarifying edits to DDR4 memory and Figure 2: K26 SOM Block Diagram.
Processing System	Added F_{MAX} details for APU, RPU, and GPU.
Supported I/O Standards	Added description of XCK26 device.
SOM240_1 Connector Pinout	Updated MIO35_WD_OUT and MIO26.
SOM240_1 Signal Names and Descriptions	Updated descriptions in table.
SOM240_2 Connector Pinout	Corrected errors in table.
SOM240_2 Signal Names and Descriptions	Updated descriptions in table.
Sideband Signals	Added PS_REF_CLK and PS_PAD_I/O.
SOM Connector Power Pins	Updated the V_{BATT} recommended conditions Table 17: SOM Power Rails. Added discussion on connecting unused I/O bank VCCO pins.
PS-GTR Transceivers	Added line rate support.
GTH Transceivers	Added line rate support.
SOM Connector Power Pins	Updated the V_{BATT} recommended conditions Table 17: SOM Power Rails.
PL Power Domain Control	Added PL power domain information.
Absolute Maximum Specifications	Added table.
EEPROM	Corrected MAC address multi-record end value to `0x88`.
Mechanical Dimensions	Updated Figure 4: K26 SOM Dimensions to add the distance between connectors.
Thermal	Added link to *Kria K26 SOM Thermal Design Guide* (UG1090).
References	
4/20/2021 Version 1.0	
Initial release.	N/A

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