AM26LS31 Quadruple Differential Line Driver

1 Features

- Meets or exceeds the requirements of ANSI TIA/EIA-422-B and ITU
- Operates from a single 5V supply
- TTL-compatible
- Complementary outputs
- High output impedance in power-off conditions
- Complementary output-enable inputs
- Available MIL-PRF-38535-qualified options (M)
  - All parameters are tested unless otherwise noted
  - On all other products, production processing does not necessarily include testing of all parameters

2 Applications

- Motor encoders
- Field transmitters: pressure sensors and temperature sensors
- Military and avionics imaging
- Temperature sensors or controllers using modbus

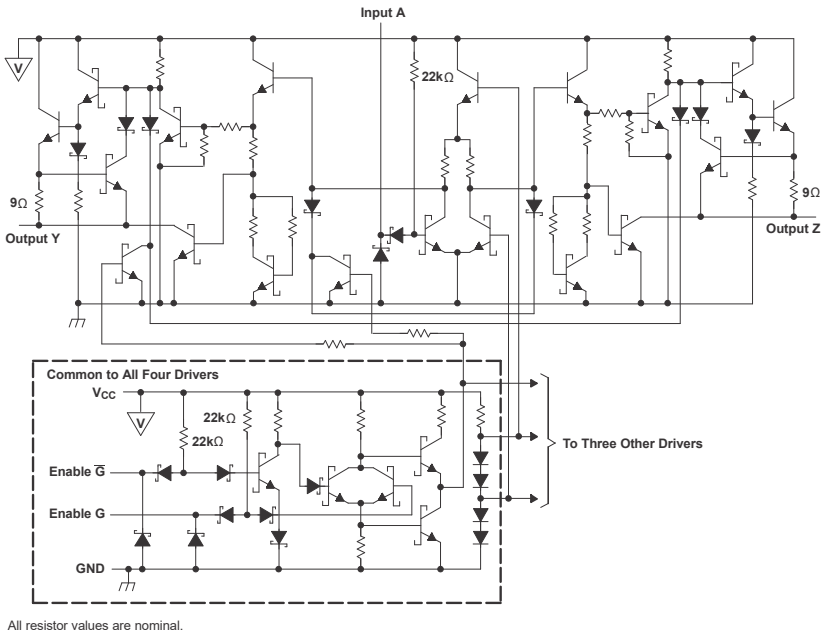
3 Description

The AM26LS31CN-E family of devices is a quadruple complementary-output line driver designed to meet the requirements of ANSI TIA/EIA-422B and ITU (formerly CCITT) Recommendation V.11. The 3-state outputs have high-current capability for driving balanced lines such as twisted-pair or parallel-wire transmission lines, and are in the high-impedance state in the power-off condition. The enable function is common to all four drivers and offers the choice of an active-high or active-low enable (G, $\overline{G}$) input. Low-power Schottky circuitry reduces power consumption without sacrificing speed.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
AM26LS31MFK	LCCC (20)	8.89mm × 8.89mm
AM26LS31MJ	CDIP (16)	19.6mm × 6.92mm
AM26LS31MW	CFP (16)	10.3mm × 6.73mm
AM26LS31CD	SOIC (16)	9.9mm × 3.91mm
AM26LS31CDB	SSOP (16)	6.2mm × 5.3mm
AM26LS31CN-E	PDIP (16)	19.3mm × 6.35mm
AM26LS31xNS	SO (16)	10.3mm × 5.3mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Schematic (Each Driver)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

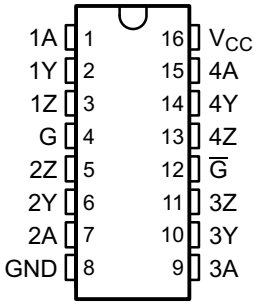

Figure 4-1. D (SOIC), DB (SSOP), N (PDIP), NS (SO), J (CDIP), or W (CFP) Packages (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1A	1	I	Logic Data Input to RS422 Driver number 1
1Y	2	O	RS-422 Data Line (Driver 1)
1Z	3	O	RS-422 Data Line (Driver 1)
G	4	I	Driver Enable (active high)
2Z	5	O	RS-422 Data Line (Driver 2)
2Y	6	O	RS-422 Data Line (Driver 2)
2A	7	I	Logic Data Input to RS422 Driver number 2
GND	8	–	Device Ground Pin
3A	9	I	Logic Data Input to RS422 Driver number 3
3Y	10	O	RS-422 Data Line (Driver 3)
3Z	11	O	RS-422 Data Line (Driver 3)
$\overline{G}$	12	I	Driver Enable (active Low)
4Z	13	O	RS-422 Data Line (Driver 4)
4Y	14	O	RS-422 Data Line (Driver 4)
4A	15	I	Logic Data Input to RS422 Driver number 4
V_{CC}	16	–	Power Input. Connect to 5V Power Source.

(1) I = input, O = output

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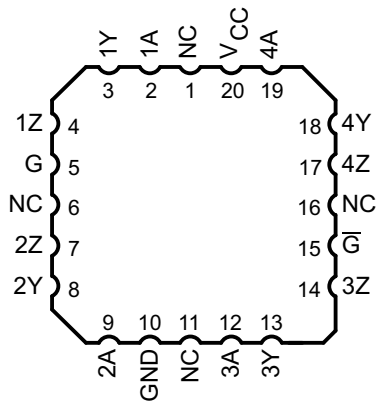

Figure 4-2. FK (LCCC) 20-Pin Package (Top View)

Table 4-2. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
NC	1	I	Logic Data Input to RS422 Driver number 1
1A	2	I	Logic Data Input to RS422 Driver number 1
1Y	3	O	RS-422 Data Line (Driver 1)
1Z	4	O	RS-422 Data Line (Driver 1)
G	5	I	Driver Enable (active high)
NC	6	I	Logic Data Input to RS422 Driver number 1
2Z	7	O	RS-422 Data Line (Driver 2)
2Y	8	O	RS-422 Data Line (Driver 2)
2A	9	I	Logic Data Input to RS422 Driver number 2
GND	10	I	Driver Enable (active high)
NC	11	I	Logic Data Input to RS422 Driver number 1
3A	12	I	Logic Data Input to RS422 Driver number 3
3Y	13	O	RS-422 Data Line (Driver 3)
3Z	14	O	RS-422 Data Line (Driver 3)
$\overline{G}$	15	I	Driver Enable (active Low)
NC	16	I	Logic Data Input to RS422 Driver number 1
4Z	17	O	RS-422 Data Line (Driver 4)
4Y	18	O	RS-422 Data Line (Driver 4)
4A	19	I	Logic Data Input to RS422 Driver number 4
V_{CC}	20	I	Power Input. Connect to 5V Power Source.

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)			7	V
V_I	Input voltage			7	V
	Output off-state voltage			5.5	V
	Lead temperature 1,6mm (1/16 in) from case for 10s			260	°C
	Lead temperature 1,6mm (1/16 in) from case for 60s	J package		300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential output voltage V_{OD}, are with respect to network GND.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	AM26LS31C	4.75	5	5.25	V
		AM26LS31M	4.5	5	5.5	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–20	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature	AM26LS31C	–40		85	°C
		AM26LS31I	–40		85	
		AM26LS31M	–55		125	

5.4 Thermal Information

THERMAL METRIC(1)		AM26LS31x				UNIT
		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	84.6	82	60.6	88.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	–	48.1	46.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	–	40.6	50.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	–	27.5	13.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	–	40.3	50.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

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5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = –18mA				–1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = –20mA		2.5			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 20mA				0.5	V
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MIN,	V_O = 0.5V			–20	µA
			V_O = 2.5V			20	
I_I	Input current at maximumimum input voltage	V_{CC} = MAX, V_I = 7V				0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V				–0.36	mA
I_{OS}	Short-circuit output current(3)	V_{CC} = MAX		–30		–150	mA
V_{POR}	Power-on-reset voltage threshold	V_{CC} rising PDIP, SO, SOIC, and SSOP packages		2.27	2.48	3.04	V
V_{BOR}	Brown-out reset voltage threshold	V_{CC} falling PDIP, SO, SOIC, and SSOP packages		2.03	2.13	2.26	V
V_{RES_HYS}	Hysteresis between power-on-reset (VP_{OR}) and brown-out reset (V_{BOR})	PDIP, SO, SOIC, and SSOP packages			350		mV
I_{CC}	Supply current	V_{CC} = MAX, all outputs disabled PDIP, SO, SOIC, and SSOP packages			1.7	3	mA
		V_{CC} = MAX, all outputs disabled All other packages			32	80	

(1) For C-suffix devices, V_{CC} minimum = 4.75V and V_{CC} maximum = 5.25V. For M-suffix devices, V_{CC} minimum = 4.5V and V_{CC} maximum = 5.5V.
(2) All typical values are at V_{CC} = 5V and T_A = 25°C.
(3) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

5.6 Switching Characteristics – AM26LS31

T_A = 25°C, V_{CC} = 5V (see Figure 6-1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 30pF, S1 and S2 open			14	20	ns
t_{PHL}	Propagation delay time, high- to low-level output				14	20	
t_{PZH}	Output enable time to high level	C_L = 30pF	R_L = 75Ω		25	40	ns
t_{PZL}	Output enable time to low level		R_L = 180Ω		37	45	
t_{PHZ}	Output disable time from high level	C_L = 10pF, S1 and S2 closed			21	30	ns
t_{PLZ}	Output disable time from low level				23	35	
t_{SKEW}	Output-to-output skew	C_L = 30pF, S1 and S2 open			1	6	ns

5.7 Switching Characteristics – AM26LS31M

T_A = 25°C, V_{CC} = 5V (see Figure 6-1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 30pF, S1 and S2 open		30	ns
t_{PHL}	Propagation delay time, high- to low-level output			30	

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5.7 Switching Characteristics – AM26LS31M (continued)

T_A = 25°C, V_{CC} = 5V (see Figure 6-1)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
t_{PZH}	Output enable time to high level	C_L = 30pF	R_L = 75Ω		60	ns
t_{PZL}	Output enable time to low level		R_L = 180Ω		68	
t_{PHZ}	Output disable time from high level	C_L = 10pF, S1 and S2 closed			45	ns
t_{PLZ}	Output disable time from low level				53	
t_{SKEW}	Output-to-output skew	C_L = 30pF, S1 and S2 open			9	ns

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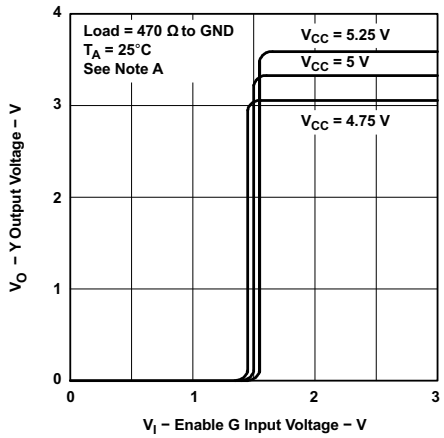
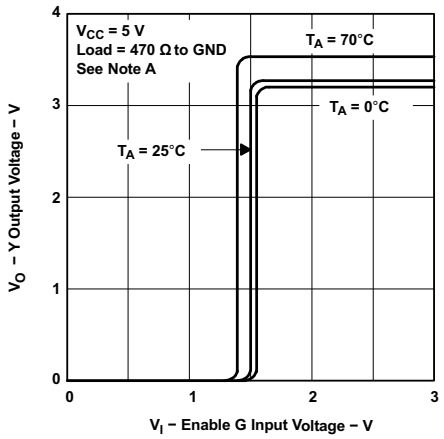
5.8 Typical Characteristics



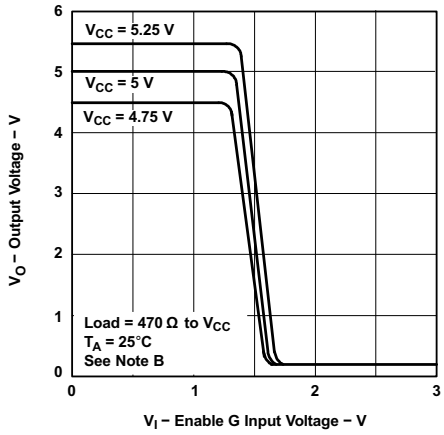
A. The A input is connected to V_{CC} during testing of the Y outputs and to ground during testing of the Z outputs.

Figure 5-1. Output Voltage vs Enable G Input Voltage



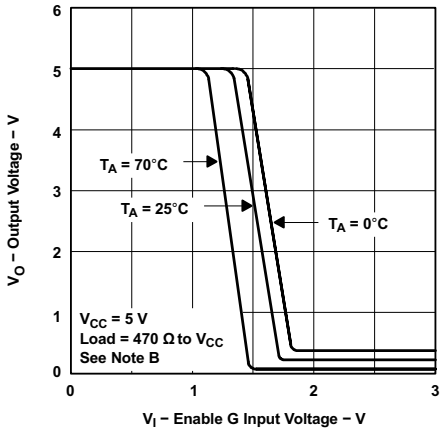
A. The A input is connected to V_{CC} during testing of the Y outputs and to ground during testing of the Z outputs.

Figure 5-2. Output Voltage vs Enable G Input Voltage



B. The A input is connected to ground during testing of the Y outputs and to V_{CC} during testing of the Z outputs.

Figure 5-3. Output Voltage vs Enable G Input Voltage



B. The A input is connected to ground during testing of the Y outputs and to V_{CC} during testing of the Z outputs.

Figure 5-4. Output Voltage vs Enable G Input Voltage

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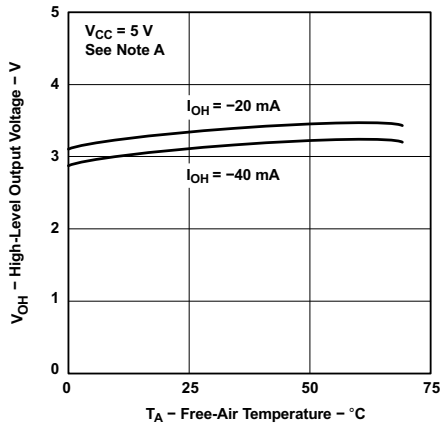
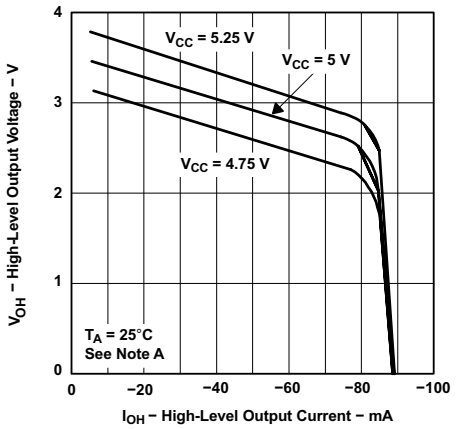
5.8 Typical Characteristics (continued)



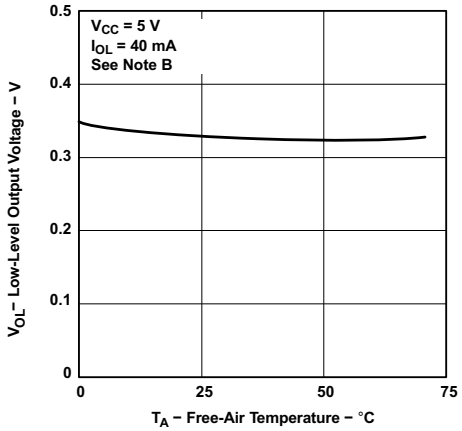
A. The A input is connected to V_{CC} during testing of the Y outputs and to ground during testing of the Z outputs.

Figure 5-5. High-Level Output Voltage vs Free-Air Temperature



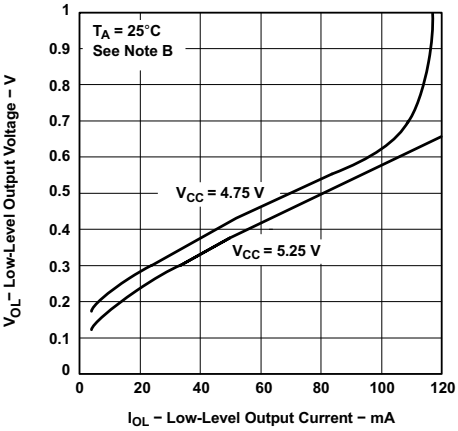
A. The A input is connected to V_{CC} during testing of the Y outputs and to ground during testing of the Z outputs.

Figure 5-6. High-Level Output Voltage vs High-Level Output Current



B. The A input is connected to ground during testing of the Y outputs and to V_{CC} during testing of the Z outputs.

Figure 5-7. Low-Level Output Voltage vs Free-Air Temperature



B. The A input is connected to ground during testing of the Y outputs and to V_{CC} during testing of the Z outputs.

Figure 5-8. Low-Level Output Voltage vs Low-Level Output Current

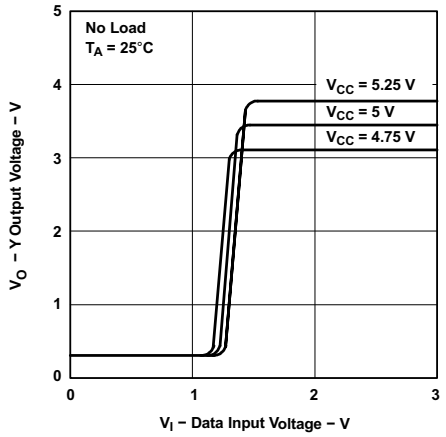


Figure 5-9. Y Output Voltage vs Data Input Voltage

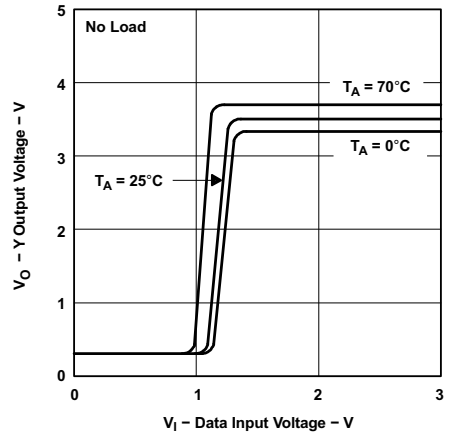


Figure 5-10. Y Output Voltage vs Data Input Voltage

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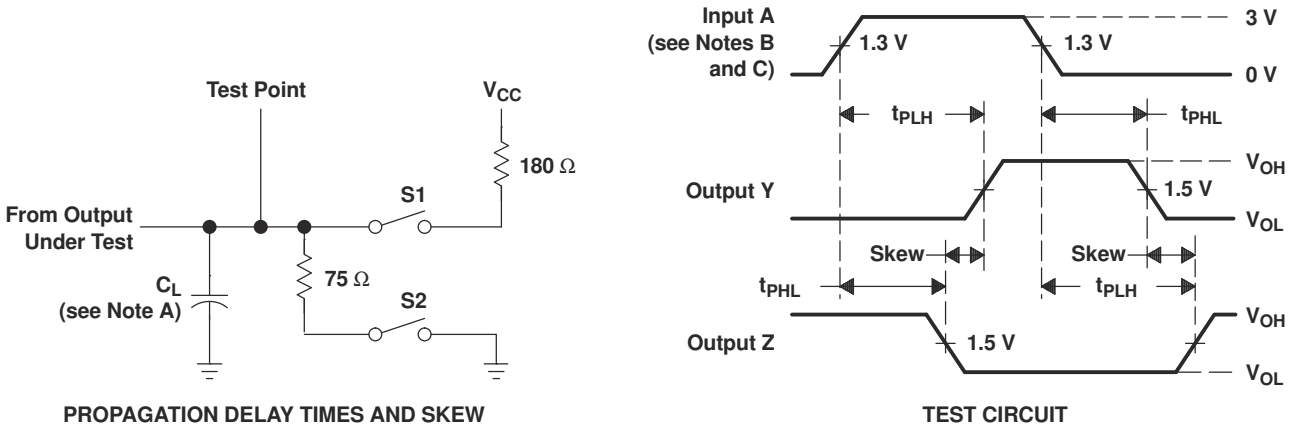
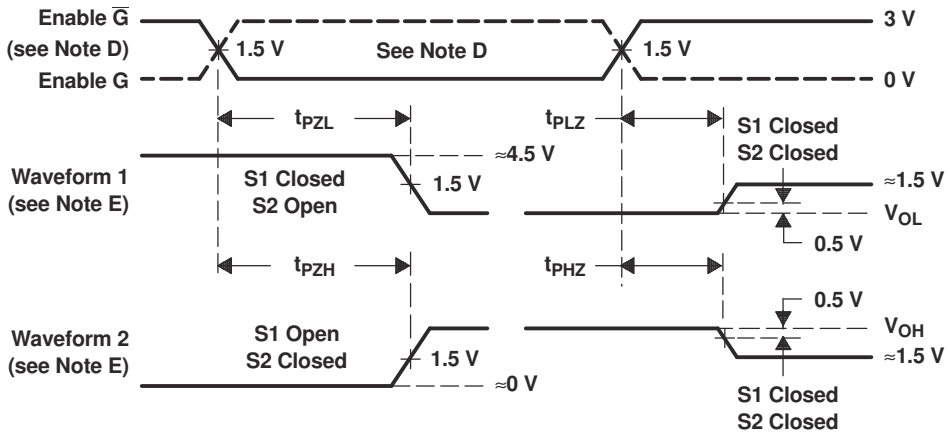
6 Parameter Measurement Information



PROPAGATION DELAY TIMES AND SKEW

TEST CIRCUIT



ENABLE AND DISABLE TIME WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω, t_r ≤ 15 ns, t_f ≤ 6 ns.
C. When measuring propagation delay times and skew, switches S1 and S2 are open.
D. Each enable is tested separately.
E. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

Figure 6-1. Test Circuit and Voltage Waveforms

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7 Detailed Description

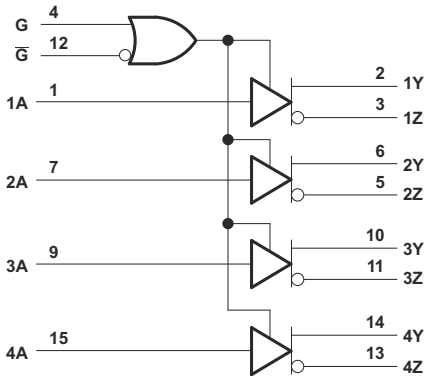
7.1 Overview

The AM26LS31x CN-E differential bus transmitter is a monolithic integrated circuit designed for unidirectional data communication on transmission lines. The device is designed for balanced transmission lines and meets ANSI Standard EIA/TIA-422B and ITU Recommendation V.11.

The AM26LS31x CN-E has a four 3-state differential line drivers that operate from a single 5V power supply. The driver also integrates active-high and active-low enables for precise device control.

The driver is designed to handle loads of a minimum of ±30mA of sink or source current. The driver features positive- and negative-current limiting for protection from line fault conditions.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Complementary Output-Enable Inputs

Configure the AM26LS31x using the G and $\overline{G}$ logic inputs to control transmitter outputs. Setting either G to a logic HIGH or $\overline{G}$ to an logic LOW enables the transmitter outputs. If G is set to logic LOW and $\overline{G}$ is set to logic HIGH, the transmitter outputs are disabled. See Table 7-1 for a complete truth table.

7.3.2 High Output Impedance in Power-Off Conditions

When the AM26LS31x transmitter outputs are disabled using G and $\overline{G}$, the outputs are set to a high-impedance state.

7.3.3 Complementary Outputs

The AM26LS31x is the driver half of a pair of devices, with the AM26LS32 being the complementary receiver. TI recommends using these devices together for peak performance, but any RS-422 compliant receive must establish proper RS-422 communication and logic level translation.

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the AM26LS31CN-E.

Table 7-1. Function Table (Each Driver)

INPUT A[1]	ENABLES		OUTPUTS	
	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

When designing a system that uses drivers, receivers, and transceivers that comply with RS-422 or RS-485, proper cable termination is essential for highly reliable applications with reduced reflections in the transmission line. Because RS-422 allows only one driver on the bus, if termination is used, it is placed only at the end of the cable near the last receiver. In general, RS-485 requires termination at both ends of the cable. Factors to consider when determining the type of termination usually are performance requirements of the application and the ever-present factor, cost. The different types of termination techniques discussed are unterminated lines, parallel termination, AC termination, and multipoint termination. Laboratory waveforms for each termination technique (except multipoint termination) show the usefulness and robustness of RS-422 (and, indirectly, RS-485). Obtain similar results when using 485-compliant devices and termination techniques. Laboratory experiments used 100 feet of 100Ω, 24-AWG, and a twisted-pair cable (Bertek). A single driver and receiver, TI AM26LS31CN-E and AM26LS32C, respectively, were tested at room temperature with a 5V supply voltage. Two plots per termination technique are shown. In each plot, the top waveform is the driver input and the bottom waveform is the receiver output. To show voltage waveforms related to transmission-line reflections, the first plot shows output waveforms from the driver at the start of the cable; the second plot shows input waveforms to the receiver at the far end of the cable.

8.2 Typical Application

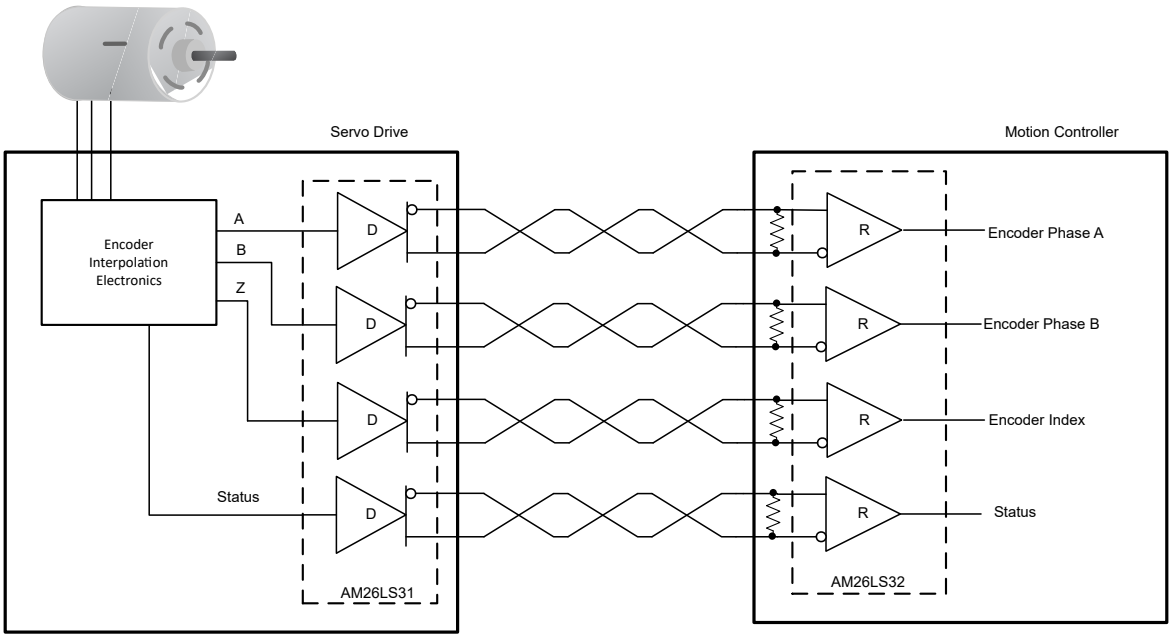

Figure 8-1. Encoder Application

8.2.1 Design Requirements

This example requires the following:

- 5V power source
- RS-485 bus operating at 10Mbps or less
- Connector that makes sure the correct polarity for port pins

8.2.2 Detailed Design Procedure

Place the device close to bus connector to keep traces (stub) short to prevent adding reflections to the bus line.

If desired, add external fail-safe biasing to establish 200mV on the A-B port, if the drive is in high-impedance state (see *Failsafe in RS-485 data buses*).

8.2.3 Application Curve

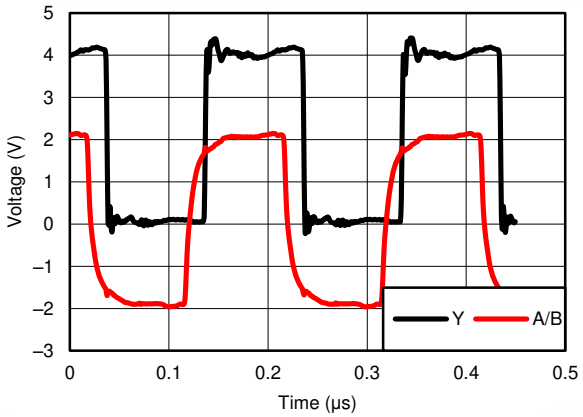

Figure 8-2. Differential 120Ω Terminated Output Waveforms (Cat 5E Cable)

8.3 Power Supply Recommendations

Place a 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can often propagate into analog circuitry through the power supply of the circuit. Use bypass capacitors to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.

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8.4.2 Layout Example

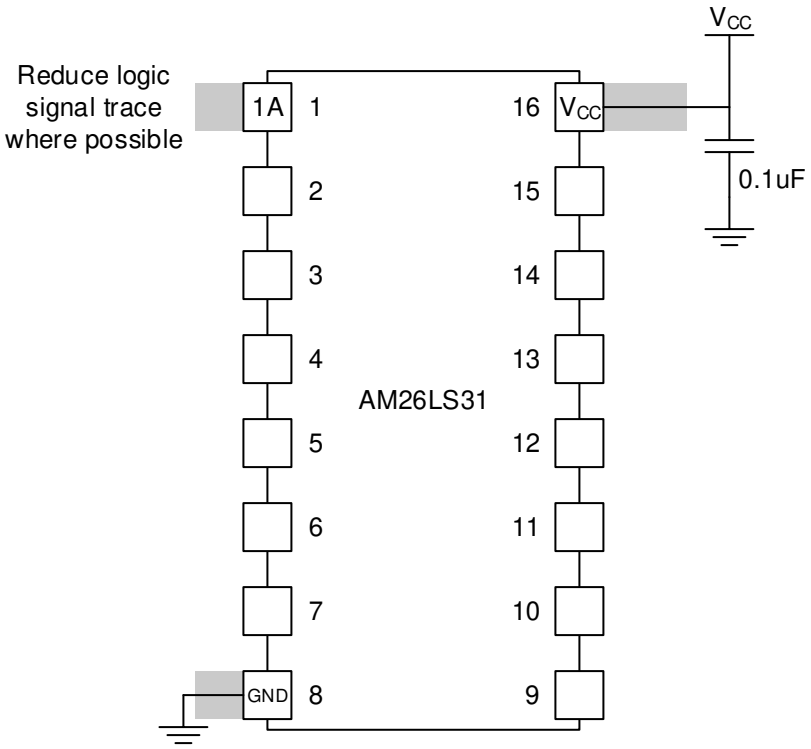

Figure 8-3. Layout Recommendation

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

Failsafe in RS-485 data buses (SLYT080)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (March 2024) to Revision N (June 2026)	Page
• Changed Table 4-2 to include 20 pins	3
• Changed recommended operating free-air temperature for AM26LS31C from 0°C (minimum) to -40°C (minimum) and from 70°C (maximum) to 85°C (maximum)	5
• Changed typical quiescent current from 32mA (typical) to 1.7mA (typical) and from 80mA (maximum) to 3mA (maximum) for PDIP, SO, SOIC, and SSOP packages	6
• Added power-on-reset, brown-out reset, and hysteresis specifications for PDIP, SO, SOIC, and SSOP packages	6

Changes from Revision L (October 2018) to Revision M (March 2024)	Page
• Changed the Device Information table to the *Package Information* table	1
• Changed the *Thermal Information* table	5

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-7802301M2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-7802301M2A AM26LS31 MFKB
5962-7802301MEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-7802301MEA AM26LS31MJB
5962-7802301MFA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-7802301MFA AM26LS31MWB
5962-7802301Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-7802301Q2A AM26LS31M
5962-7802301Q2A.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-7802301Q2A AM26LS31M
AM26LS31CD	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	AM26LS31C
AM26LS31CDBR	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SA31C
AM26LS31CDBR.A	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SA31C
AM26LS31CDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26LS31C
AM26LS31CDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LS31C
AM26LS31CDRG4	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	AM26LS31C
AM26LS31CN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	AM26LS31CN
AM26LS31CN.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	AM26LS31CN
AM26LS31CNSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26LS31
AM26LS31CNSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	26LS31
AM26LS31INSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26LS31
AM26LS31INSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26LS31
AM26LS31MFKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-7802301M2A AM26LS31 MFKB

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AM26LS31MFKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-7802301M2A AM26LS31 MFKB
AM26LS31MJB	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-7802301MEA AM26LS31MJB
AM26LS31MJB.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-7802301MEA AM26LS31MJB
AM26LS31MWB	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-7802301MFA AM26LS31MWB
AM26LS31MWB.A	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-7802301MFA AM26LS31MWB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF AM26LS31, AM26LS31M :

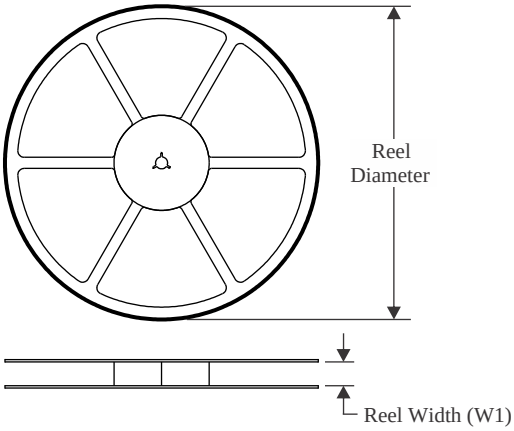
- Catalog : AM26LS31
- Military : AM26LS31M

NOTE: Qualified Version Definitions:

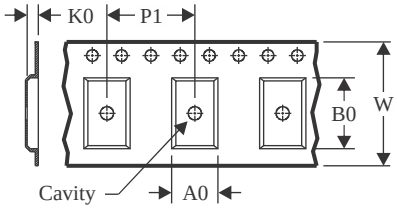
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

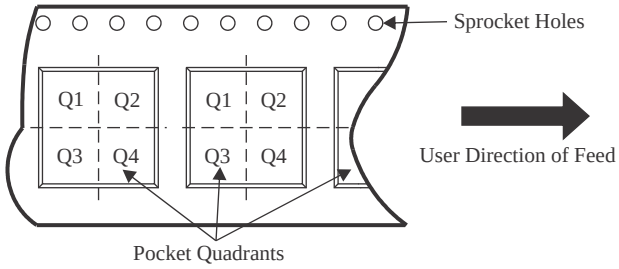


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

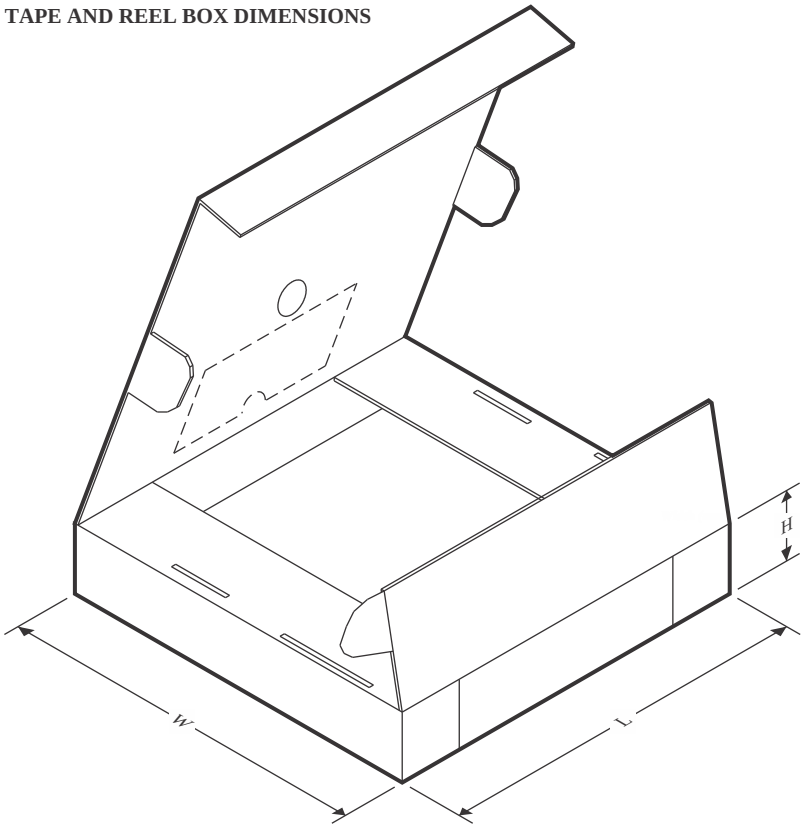
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26LS31CDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
AM26LS31CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LS31CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LS31CNSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
AM26LS31INSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

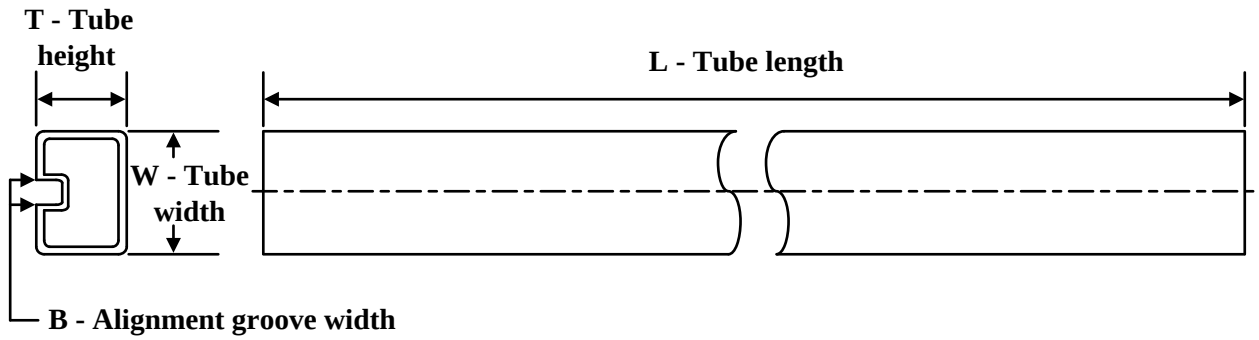
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26LS31CDBR	SSOP	DB	16	2000	353.0	353.0	32.0
AM26LS31CDR	SOIC	D	16	2500	340.5	336.1	32.0
AM26LS31CDR	SOIC	D	16	2500	353.0	353.0	32.0
AM26LS31CNSR	SOP	NS	16	2000	353.0	353.0	32.0
AM26LS31INSR	SOP	NS	16	2000	353.0	353.0	32.0

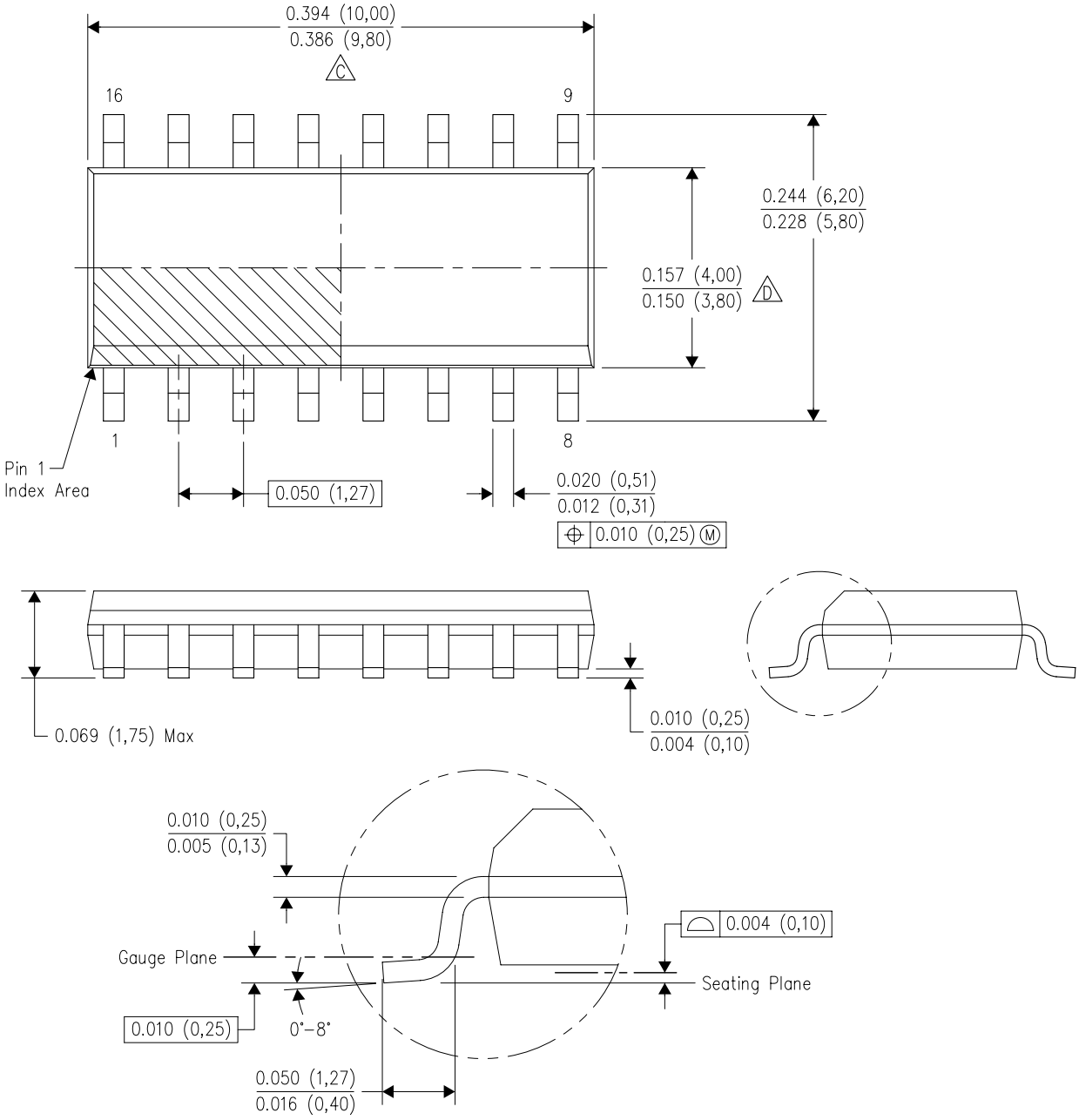
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-7802301M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-7802301MFA	W	CFP	16	25	506.98	26.16	6220	NA
5962-7802301Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-7802301Q2A.A	FK	LCCC	20	55	506.98	12.06	2030	NA
AM26LS31CN	N	PDIP	16	25	506	13.97	11230	4.32
AM26LS31CN.A	N	PDIP	16	25	506	13.97	11230	4.32
AM26LS31MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
AM26LS31MFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
AM26LS31MWB	W	CFP	16	25	506.98	26.16	6220	NA
AM26LS31MWB.A	W	CFP	16	25	506.98	26.16	6220	NA

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



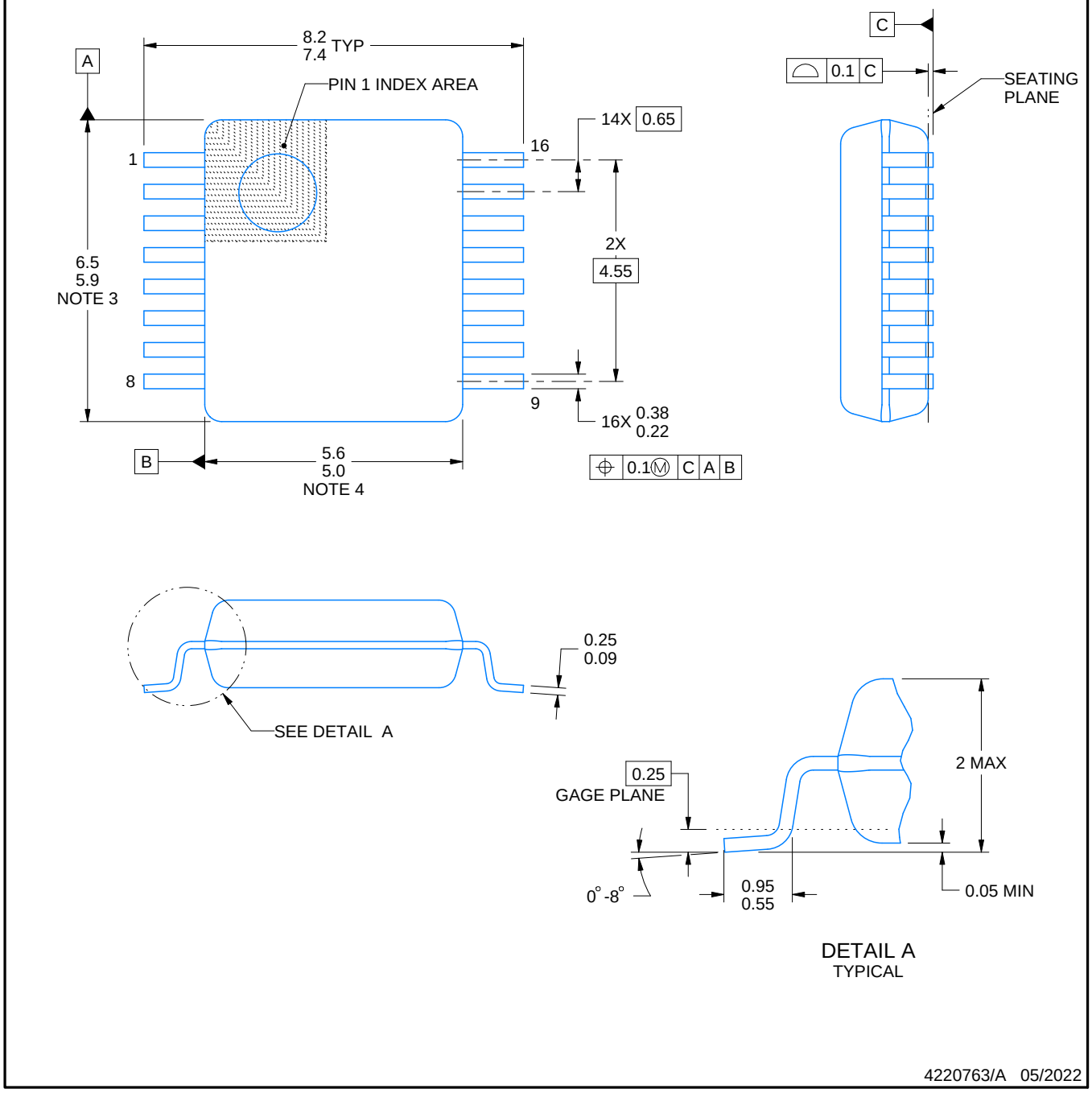
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

DB0016A

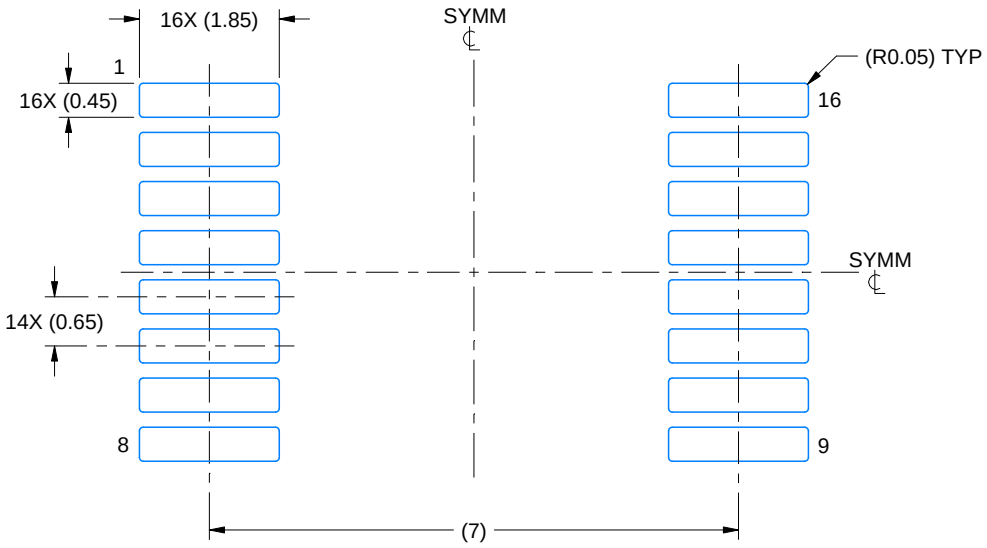
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

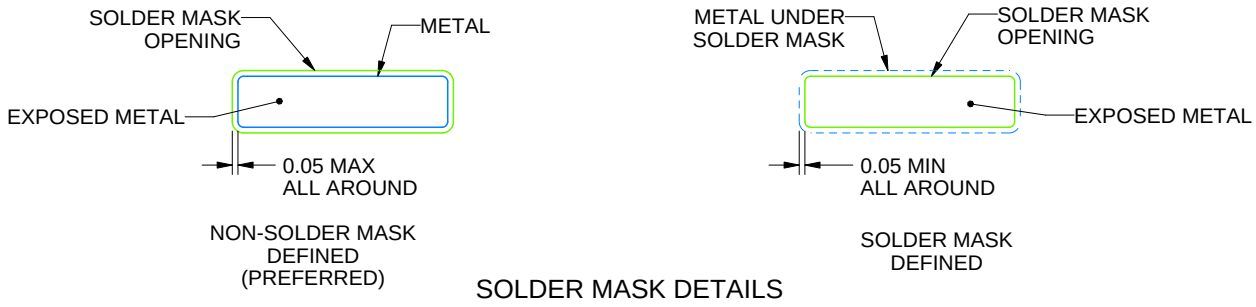


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

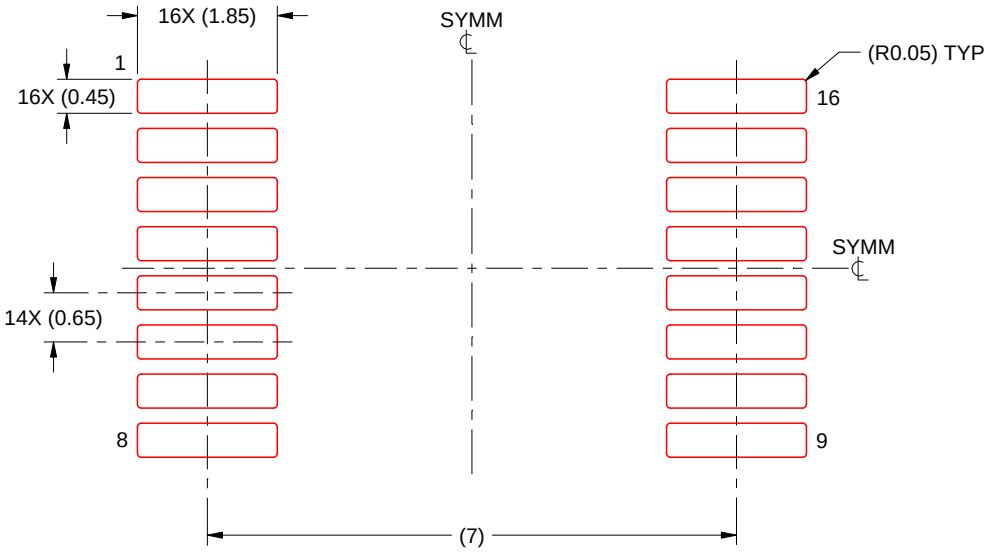
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



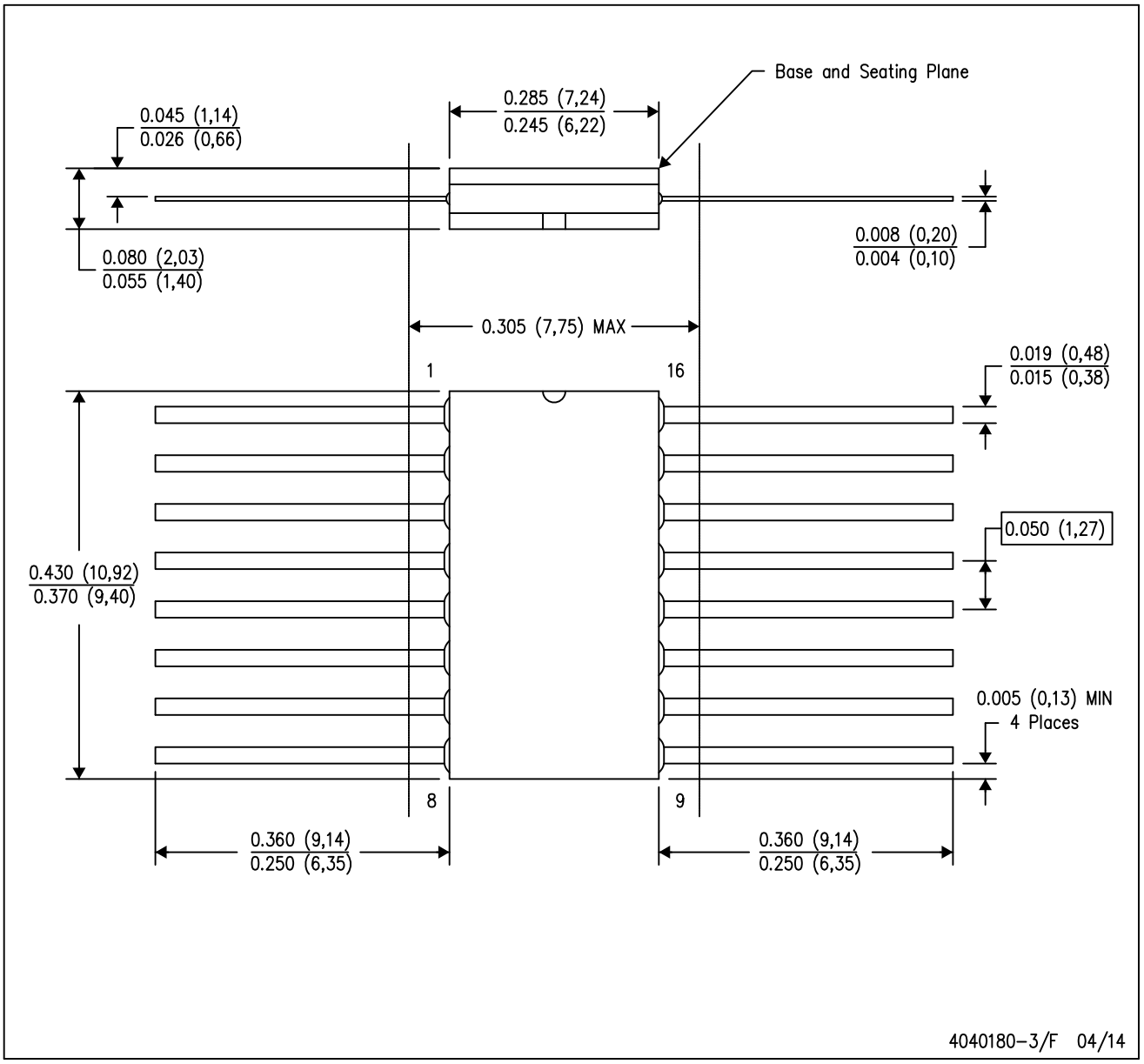
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

GENERIC PACKAGE VIEW

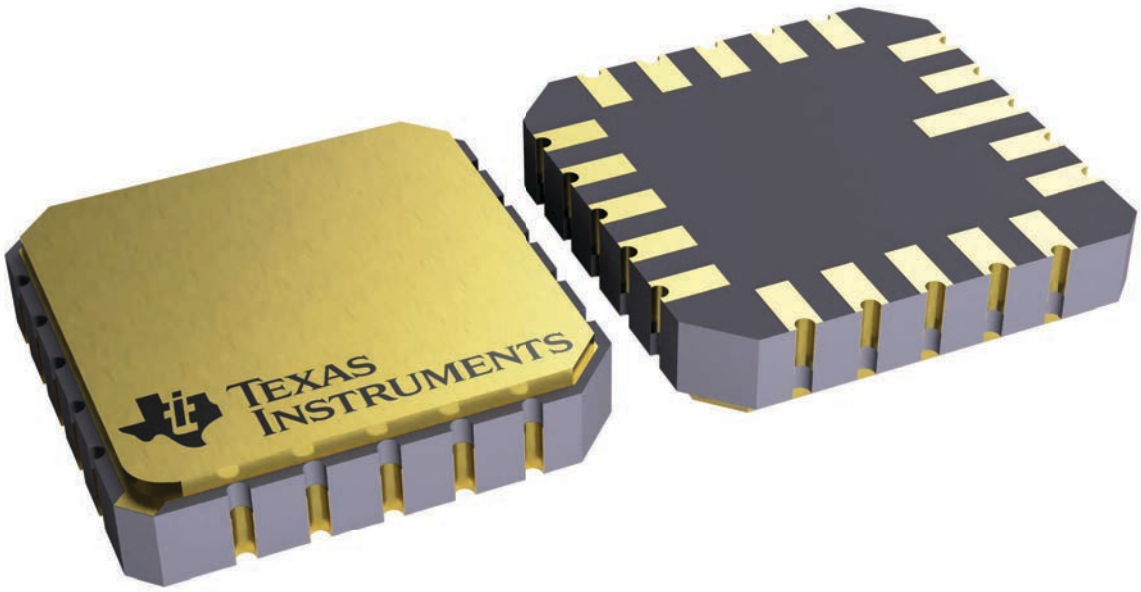
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

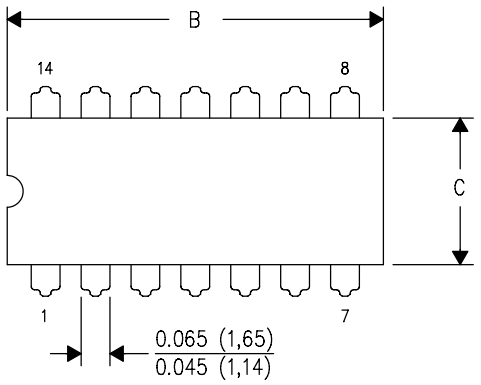


4229370VA\

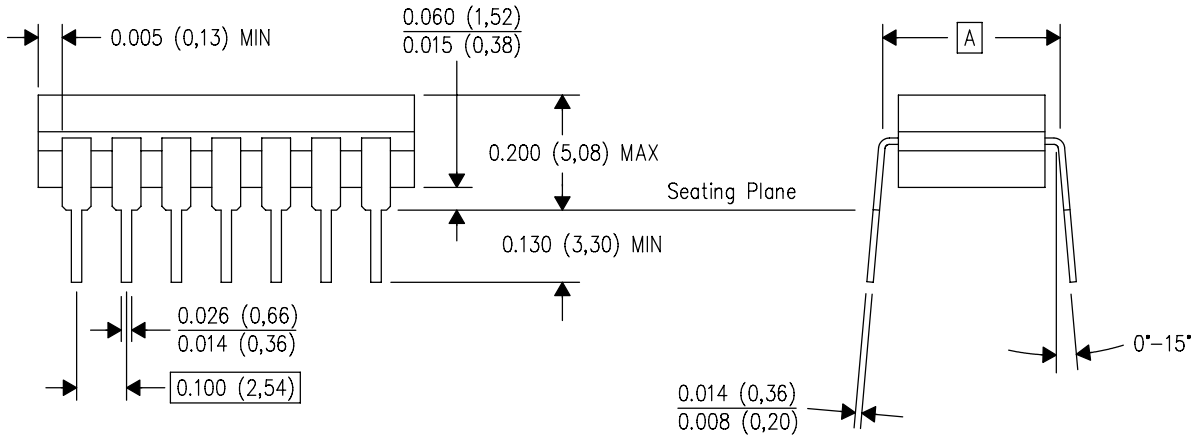
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



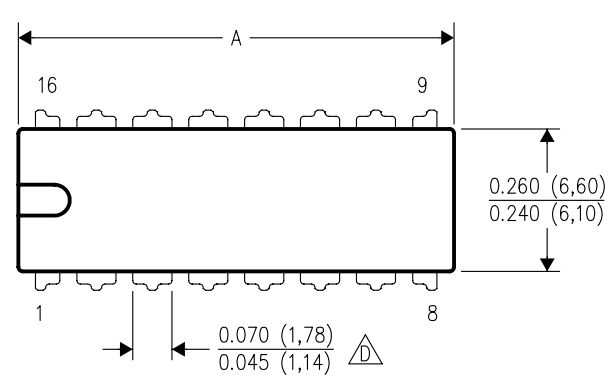
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

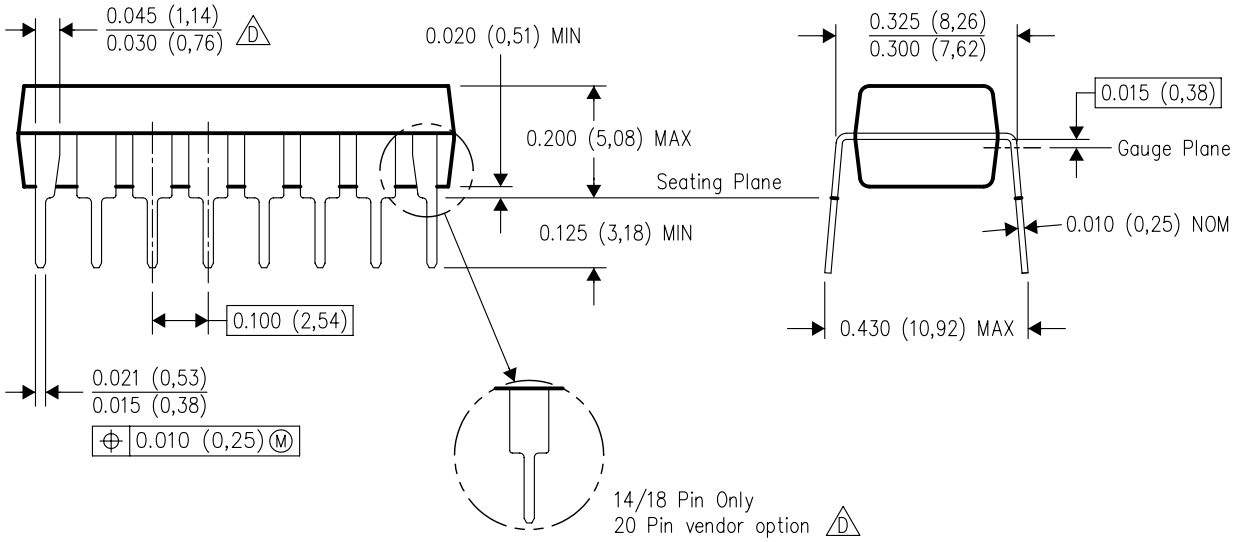
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

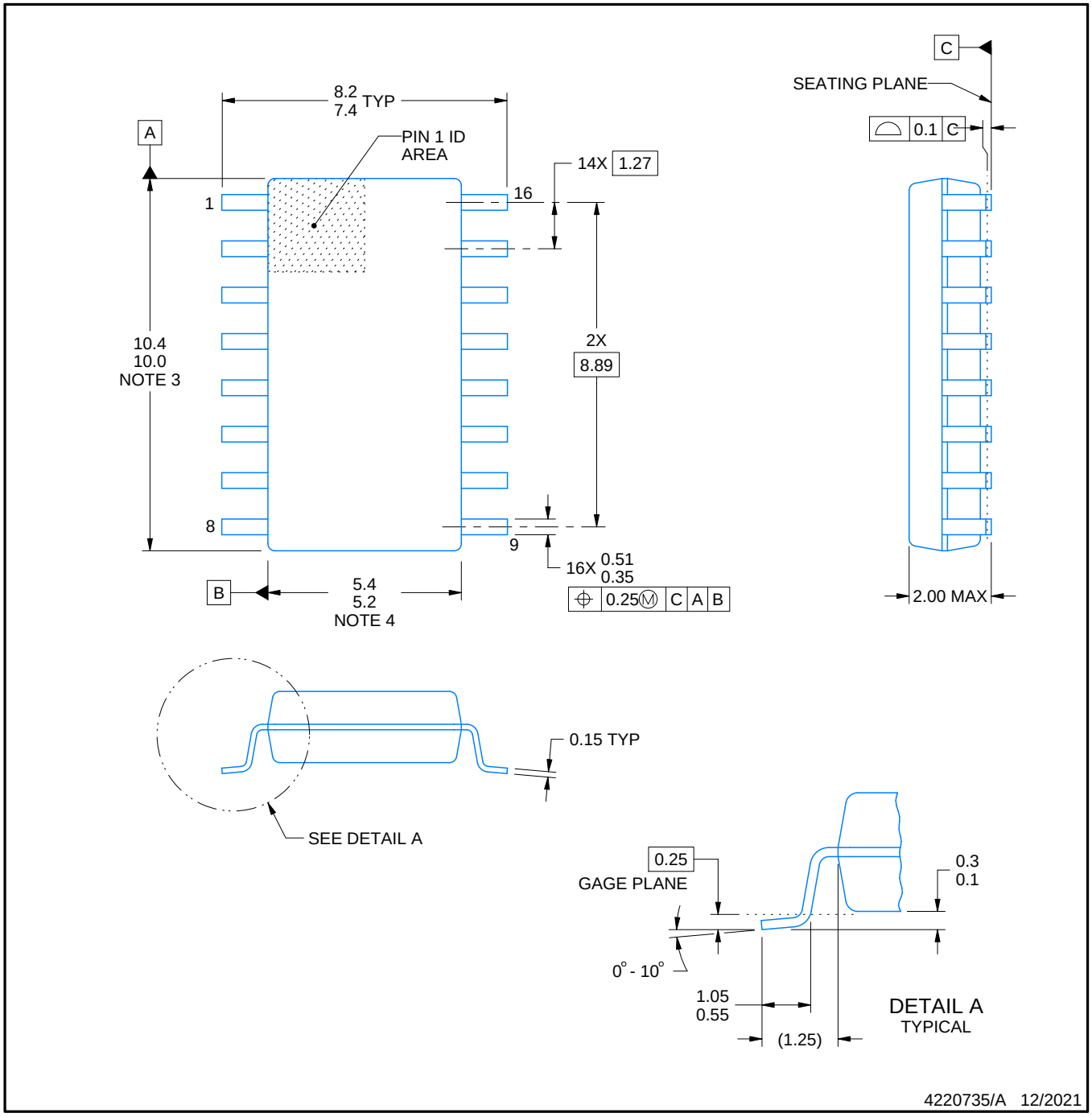


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



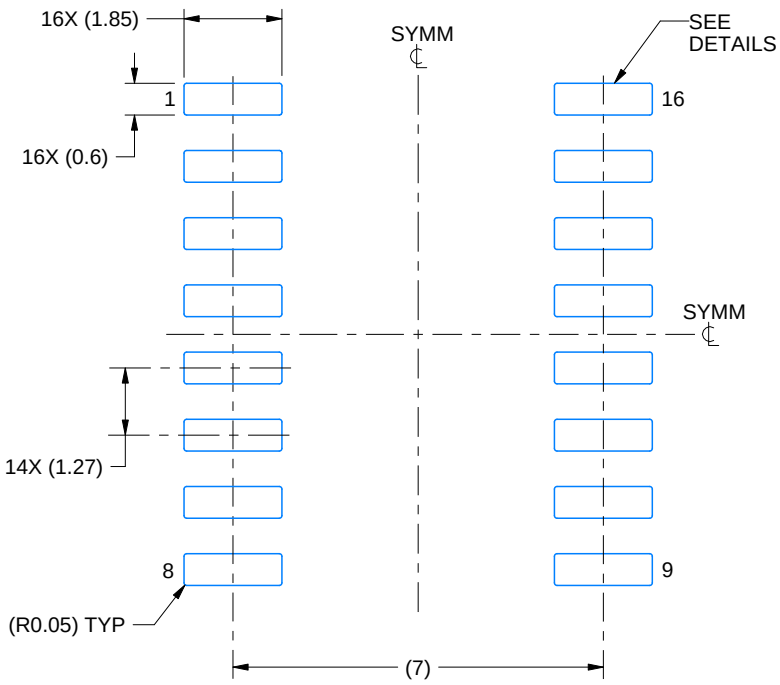
4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

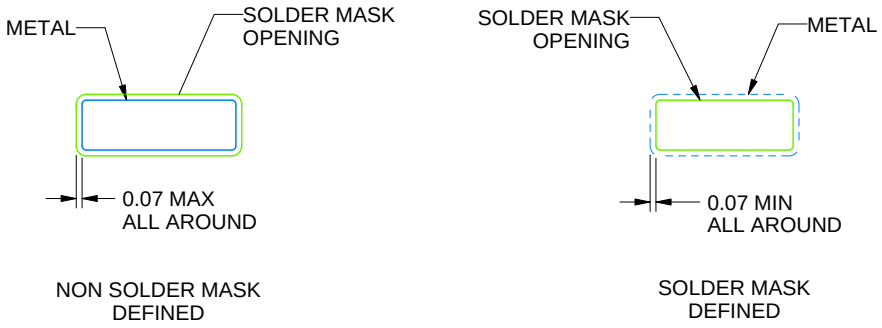


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

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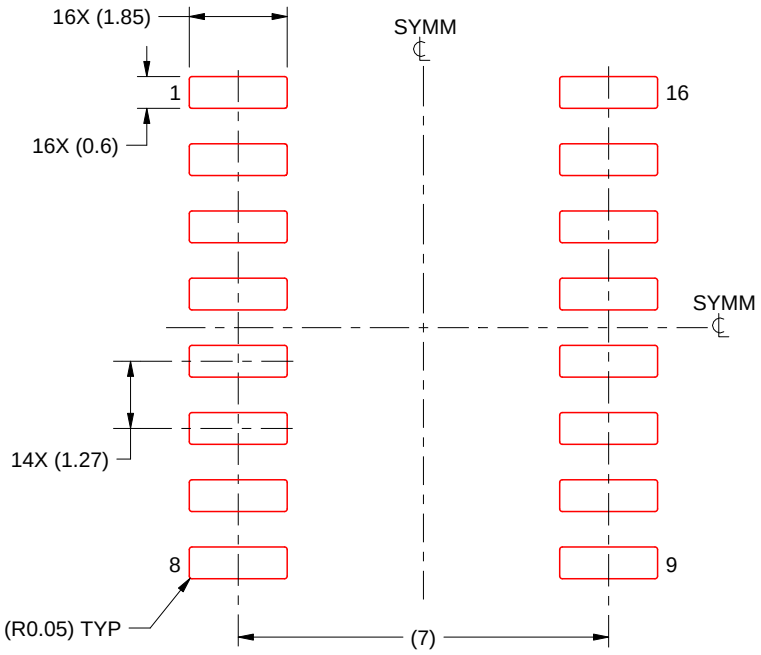
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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