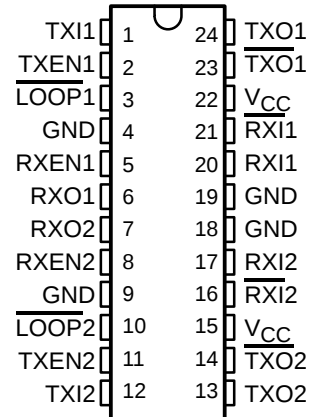


SN75ALS085 LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

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- Meets or Exceeds the Requirements of IOS 8802.3:1989 and ANSI/IEEE Std 802.3-1988
- Interdevice Loopback Paths for System Testing
- Squelch Function Implemented on the Receiver Inputs
- Drives a Balanced 78-Ω Load
- Transformer Coupling Not Required in System
- Power-Up/Power-Down Protection (Glitch Free)
- Isolated Ground Pins for Reduced Noise Coupling
- Fault-Condition Protection Built Into the Device
- Driver Inputs Are Level-Shifted ECL Compatible
- Package Options Include Plastic Small-Outline (DW) Package and Standard Plastic (NT) DIP

DW OR NT PACKAGE
(TOP VIEW)



description

The SN75ALS085 is a high-speed, advanced low-power Schottky, dual-channel driver/receiver device designed for use in the AUI of ANSI/IEEE Std 802.3-1988. The two drivers on the device drive a 78-Ω balanced, terminated twisted-pair transmission line up to a maximum length of 50 meters. In the off (idle) state, the drivers maintain minimal differential output voltage on the twisted-pair line and, at the same time, remain within the required output common-mode range.

With the driver enable (TXEN) high, upon receiving the first falling edge into the driver input, the differential outputs rise to full-amplitude output levels within 25 ns. The output amplitude is maintained for the remainder of the packet. After the last positive packet edge is transmitted into the driver, the driver maintains a minimum of 70% full differential output for a minimum of 200 ns, then decays to a minimum level for the reset (idle) condition within 8 μs. Disabling the driver by taking the driver enable low also forces the output into the idle condition after the normal 8-μs timeout. While operating, the drivers are able to withstand a set of fault conditions and not suffer damage due to the faults being applied. The drivers power up in the idle state to ensure that no activity is placed on the twisted-pair cable, which could be interpreted as network traffic.

The line receiver squelch function interfaces to a differential twisted-pair line terminated external to the device. The receiver squelch circuit allows differential receive signals to pass through, as long as the input amplitude and pulse duration are greater than the minimum squelch threshold. This ensures a good signal-to-noise ratio while the data path is active and prevents system noise from causing false data transitions during line shutdown and line-idle conditions. The receiver outputs (RXO) default to a high level and the receiver-enable (RXEN) outputs default to a low level while the squelch function is blocking the data path through the receiver (idle). The line receiver squelch becomes active within 50 ns when the input squelch threshold is exceeded. RXEN is driven high when the squelch circuit allows data to pass through the receiver. The receiver squelch circuit also can withstand a set of fault conditions while operating, without causing permanent damage to the device.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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description (continued)

The purpose of the loop functions is to provide a means by which system data-path verification can be done to isolate faulty interfaces and assist in network diagnosis. The LOOP pins are TTL compatible and must be held high for normal operation. When $\overline{\text{LOOP}}1$ is taken low, the output of driver 1 (TXO1) immediately goes into the idle state. Also, the input to receiver 1 is ignored, and a path from a transmit input (TXI1) to RXO1 is established. When $\overline{\text{LOOP}}1$ is taken back high, driver 1 and receiver 1 revert back to their normal operation. When $\overline{\text{LOOP}}2$ is taken low, a similar data path is established between TXI1 and RXO2. TXEN1 must be high for the loop functions to operate, and TXEN1 can be used to gate the loop function if desired. During loop operation, the respective RXEN reflects the status of TXEN1.

The SN75ALS085 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T _A	PACKAGED DEVICES	
	PLASTIC SMALL OUTLINE (DW)	PLASTIC DIP (NT)
0°C to 70°C	SN75ALS085DW	SN75ALS085NT

The DW package is available taped and reeled. Add the suffix R to device type (e.g., SN75ALS085DWR).

Function Tables

RECEIVER ($\overline{\text{LOOP}} = \text{H}$)

RXI	PREVIOUS RXEN	OUTPUTS	
		RXEN	RXO
$V_{ID} = 1315 \text{ mV to } -175 \text{ mV}, t_W < 25 \text{ ns}$	L	L	H
$V_{ID} = -275 \text{ mV to } -1315 \text{ mV}, t_W > 50 \text{ ns}$	X	H	L
$V_{ID} = 318 \text{ mV to } 1315 \text{ mV}, t_W < 142 \text{ ns}$	H	H	H
$V_{ID} = 318 \text{ mV to } 1315 \text{ mV}, t_W > 187 \text{ ns}$	X	L	H

H = high level, L = low level, X = don't care

DRIVER ($\overline{\text{LOOP}} = \text{H}$)

TXI	TXEN	PREVIOUS TXO	OUTPUT TXO
L	L	Idle	Idle
H	L	Idle	Idle
↓	H	Idle	L
L	H	Active	L
$H < 260 \mu\text{s}$	H	Active	H
$H > 8 \mu\text{s}$	H	Active	Idle
L	$L > 8 \mu\text{s}$	Active	Idle
$H < 260 \text{ ns}$	$L > 8 \mu\text{s}$	Active	Idle
$H < 260 \text{ ns}$	$L < 260 \text{ ns}$	Active	H
$H > 8 \mu\text{s}$	$L < 260 \text{ ns}$	Active	Idle
L	$L < 260 \text{ ns}$	Active	L

$H = V_I \geq V_T \text{ max}, L = V_I \leq V_T \text{ min}$



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Function Tables (continued)

LOOP										
INPUTS						OUTPUTS				
LOOP1	LOOP2	TXI1	TXEN1	RXI1	RXI2	RXO1	RXO2	RXEN1	RXEN2	TXO1
L	L	L	H	X	X	L	L	H	H	Idle
L	L	H	H	X	X	H	H	H	H	Idle
L	L	X	L	X	X	H	H	L	L	Idle
L	H	L	H	X	Normal	L	Normal	H	Normal	Idle
L	H	H	H	X	Normal	H	Normal	H	Normal	Idle
L	H	X	L	X	Normal	H	Normal	L	Normal	Idle
H	L	L	H	Normal	X	Normal	L	Normal	H	Idle
H	L	H	H	Normal	X	Normal	H	Normal	H	Idle
H	L	X	L	Normal	X	Normal	H	Normal	L	Idle
H	H	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal

H = high level, L = low level, X = don't care

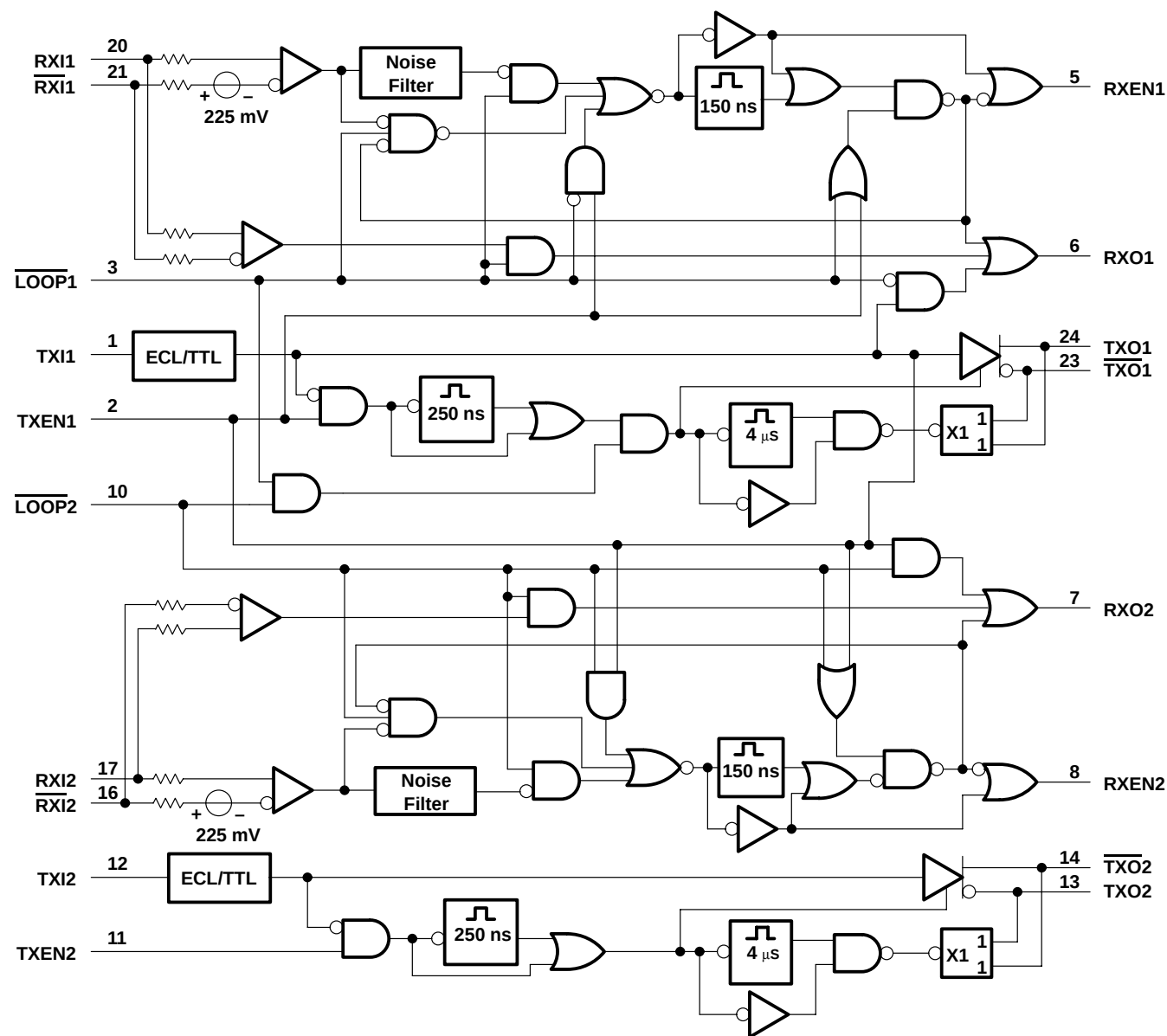


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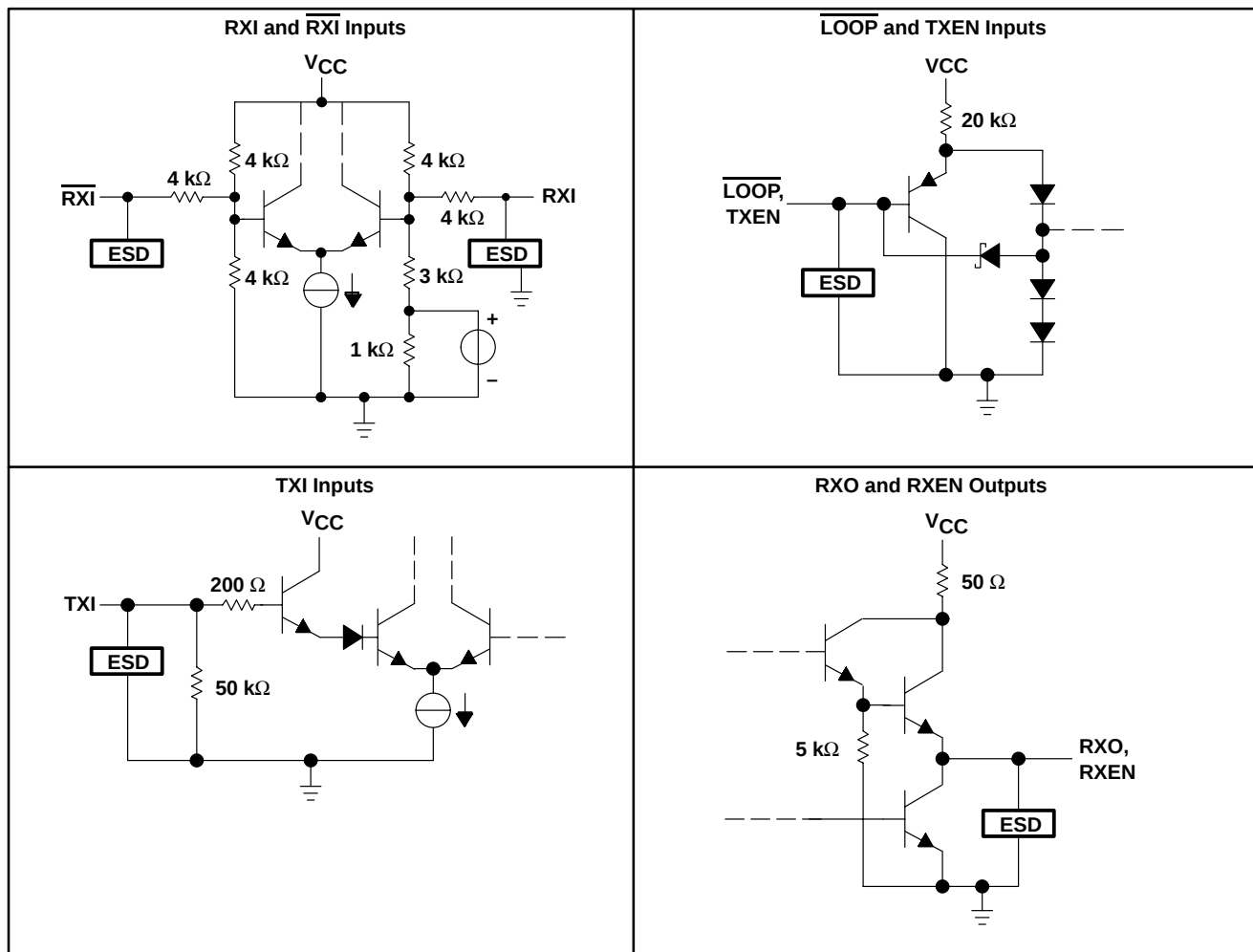
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logic diagram (positive logic)



schematics of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	6 V
TXI and $\overline{LOOP}$ input voltage, V_I	5.5 V
TXO and $\overline{TXO}$ output voltage, V_O	16 V
RXI and $\overline{RXI}$ input voltage, V_I	16 V
RXO and RXEN output voltage, V_O	5.5 V
Package thermal impedance, θ_{JA} (see Notes 2 and 3): DW package	46°C/W
(see Notes 2 and 4): NT package	67°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	–65 to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. Voltage values are with respect to network ground terminal.
 2. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-3.

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.75	5	5.25	V
V_{IC} Common-mode voltage at RXI inputs	1		4.2	V
V_{ID} Differential voltage between RXI inputs	±318		±1315	mV
V_{IH} High-level input voltage, $\overline{LOOP}$ and TXEN	2			V
V_{IL} Low-level input voltage, $\overline{LOOP}$ and TXEN			0.8	V
I_{OH} High-level output current, RXO and RXEN			– 0.4	mA
I_{OL} Low-level output voltage, RXO and RXEN			16	mA
t_{su1} Setup time, driver mode, TXEN high before TXI↓ (see Figure 7)	10			ns
t_{su2} Setup time, loop mode, $\overline{LOOP}$ low before TXEN↑ (see Figure 9)	15			ns
t_{su3} Setup time, loop mode, TXEN high before TXI↓ (see Figure 9)	10			ns
t_{h1} Hold time, loop mode, TXEN high after TXI↑ (see Figure 8)	10			ns
t_{h2} Hold time, loop mode, $\overline{LOOP}$ low after TXEN↓ (see Figure 8)	15			ns
T_A Operating free-air temperature	0		70	°C



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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT	
V _{IK}	Clamp voltage at all inputs		I _I = −18 mA		−1.5		V	
V _(TO)	Driver input (TXI) threshold voltage		T _A = 0°C	V _{CC} = 4.75 V	3.202	3.752	V	
				V _{CC} = 5 V	3.389	3.998		
				V _{CC} = 5.25 V	3.577	4.244		
			T _A = 25°C	V _{CC} = 4.75 V	3.213	3.797		V
				V _{CC} = 5 V	3.400	4.043		
				V _{CC} = 5.25 V	3.588	4.289		
			T _A = 70°C	V _{CC} = 4.75 V	3.239	3.849		V
				V _{CC} = 5 V	3.426	4.095		
				V _{CC} = 5.25 V	3.614	4.341		
Receiver differential input threshold voltage					−275		mV	
V _{OC}	Driver output (TXO) common-mode voltage		Idle	TXEN at 0.8 V, LOOP2 at 2 V, See Figure 1	1	4.2	V	
			Active	TXEN at 2 V, LOOP2 at 2 V, See Figure 1	1	4.2		
			Active	TXEN at 2 V, LOOP2 at 2 V, See Figure 1	1	4.2		
V _{OD}	Driver output (TXO) differential voltage		Idle	TXEN at 0.8 V, LOOP2 at 2 V, See Figure 1	±40		mV	
			Active	TXEN at 2 V, LOOP2 at 2 V, See Figure 1	−600	1315		
			Active	TXEN at 2 V, LOOP2 at 2 V, See Figure 1	600	1315		
V _{OH}	High-level output voltage		RXO, RXEN	I _{OH} = −0.4 mA	2.4		V	
V _{OL}	Low-level output voltage		RXO, RXEN	I _{OL} = 16 mA	0.5		V	
I _{IH}	High-level input current		TXEN, <u>LOOP</u>	V _I = 2 V	20		μA	
			TXI	V _I = 4.5 V	400			
			<u>RXI</u> , RXI	V _{ID} = −0.5 V, V _{IC} = 1 V to 4.2 V	1000			
I _{IL}	Low-level input current		TXEN, <u>LOOP</u>	V _I = 0.8 V	−200		μA	
			TXI	V _I = 3.1 V	100			
				V _I = 0.3 V	4 10			
			<u>RXI</u> , RXI	V _{ID} = 0.5 V, V _{IC} = 1 V to 4.2 V	1000			
I _{OD}	Driver differential output current		Idle	TXEN at 0.8 V, LOOP2 at 2 V, See Figure 2	±4		mA	
I _{OS}	Short-circuit output current [†]		RXO, RXEN	V _O at 0 V, RXI at 2 V	−40	−150	mA	
I _{CC}	Supply current			<u>LOOP2</u> at 2 V, TXI at 4.5 V, TXEN at 2 V, Outputs open	225		mA	

[†] Not more than one output should be shorted at a time, and the duration of the test should not exceed 1 second.



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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Driver fault condition current [‡]	TXO shorted to $\overline{\text{TXO}}$, Current measured in short		150	mA
	TXO at 0 V, $\overline{\text{TXO}}$ is open, Current measured at TXO		150	
	TXO is open, $\overline{\text{TXO}}$ at 0, Current measured at $\overline{\text{TXO}}$		150	
	TXO at 0 V, $\overline{\text{TXO}}$ at 0 V, Current measured at TXO and $\overline{\text{TXO}}$		150	
	TXO at 16 V, $\overline{\text{TXO}}$ is open, Current measured at TXO		150	
	TXO is open, $\overline{\text{TXO}}$ at 16 V, Current measured at TXO		150	
	TXO at 16 V, $\overline{\text{TXO}}$ at 16 V, Current measured at TXO and $\overline{\text{TXO}}$		150	
Receiver fault condition current [‡]	RXI shorted to $\overline{\text{RXI}}$, Current measured in short		10	mA
	RXI at 0 V, $\overline{\text{RXI}}$ is open, Current measured at RXI		3	
	RXI is open, $\overline{\text{RXI}}$ at 0 V, Current measured at RXI		3	
	RXI at 0 V, $\overline{\text{RXI}}$ at 0 V, Current measured at RXI and $\overline{\text{RXI}}$		3	
	RXI at 16 V, $\overline{\text{RXI}}$ at open, Current measured at RXI		10	
	RXI at open, $\overline{\text{RXI}}$ at 16 V, Current measured at $\overline{\text{RXI}}$		10	
	RXI at 16 V, $\overline{\text{RXI}}$ at 16 V, Current measured at RXI and $\overline{\text{RXI}}$		10	

[‡] Fault conditions should be measured on only one channel at a time.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

driver

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t _{PLH} Propagation delay time, low-to-high level output	TXI	TXO, $\overline{\text{TXO}}$	TXEN at 2 V, See Figure 3		15	ns
t _{PHL} Propagation delay time, high-to-low level output	TXI	TXO, $\overline{\text{TXO}}$	TXEN at 2 V, See Figure 3		15	ns
t _{PIL} Propagation delay time, idle-to-low level output	TXI	TXO, $\overline{\text{TXO}}$	TXEN at 2 V, See Figure 4		25	ns
t _{PIL} Propagation delay time, idle-to-low level output	TXEN	TXO, $\overline{\text{TXO}}$	TXI at 3.2 V, See Figure 5		25	ns
t _w Output pulse duration, from low-to-high level to 70% output level		TXO, $\overline{\text{TXO}}$	TXEN at 2 V, See Figure 6	260	8000	ns
V _{OD(U)} Driver output differential undershoot voltage	TXI	TXO, $\overline{\text{TXO}}$	TXEN at 2 V, See Figure 6		–100	mV
t _{sk} Driver caused signal skew t _{PLH} – t _{PHL}	TXI	TXO, $\overline{\text{TXO}}$	TXEN at 2 V, See Figure 3		±3	ns
t _r Rise time, TXO, $\overline{\text{TXO}}$			TXEN at 2 V, See Figure 3	1	5	ns
t _f Fall time, TXO, $\overline{\text{TXO}}$			TXEN at 2 V, See Figure 3	1	5	ns



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receiver

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high level output	$\overline{RXI}$, RXI	R XO	$V_{IC} = 1\text{ V to }4.2\text{ V}$, See Figure 10		15	ns
t_{PHL} Propagation delay time, high-to-low level output	$\overline{RXI}$, RXI	R XO	$V_{IC} = 1\text{ V to }4.2\text{ V}$, See Figure 10		15	ns
t_{PLH} Start-up delay time, low-to-high level output	$\overline{RXI}$, RXI	R XEN	$V_{IC} = 1\text{ V to }4.2\text{ V}$, $V_{ID} = -500\text{ mV}$, See Figure 12		55	ns
t_{PHL} Shutdown delay time, high-to-low level output	$\overline{RXI}$, RXI	R XEN	$V_{IC} = 1\text{ V to }4.2\text{ V}$, $V_{ID} = 500\text{ mV}$, See Figure 12	142	181	ns
t_{sk} Receiver caused signal skew ($t_{PLH} - t_{PHL}$)	$\overline{RXI}$, RXI	R XO	$V_{IC} = 1\text{ V to }4.2\text{ V}$, $V_{ID} = 500\text{ mV}$, See Figure 10		± 3	ns
t_w Pulse duration at $\overline{RXI}$ and RXI (to not activate squelch)			$V_{IC} = 1\text{ V to }4.2\text{ V}$, $V_{ID} = -175\text{ mV}$, See Figure 11	25		ns
t_w Pulse duration at $\overline{RXI}$ and RXI (to activate squelch)			$V_{IC} = 1\text{ V to }4.2\text{ V}$, $V_{ID} = -275\text{ mV}$, See Figure 11		50	ns
t_{r1} Rise time, R XO			$V_{IC} = 1\text{ V to }4.2\text{ V}$, $V_{ID} = \pm 500\text{ mV}$, See Figure 10	1	8	ns
t_{r2} Rise time, R XEN			$V_{IC} = 1\text{ V to }4.2\text{ V}$, $V_{ID} = \pm 500\text{ mV}$, See Figure 12	1	8	ns
t_{f1} Fall time, R XO			$V_{IC} = 1\text{ V to }4.2\text{ V}$, $V_{ID} = \pm 500\text{ mV}$, See Figure 10	1	8	ns
t_{f2} Fall time, R XEN			$V_{IC} = 2.5\text{ V}$, $V_{ID} = \pm 500\text{ V}$, See Figure 12	1	8	ns
t_v R XO valid after R XEN high			See Figure 10	-10	15	ns

loop

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high level output	TXI	R XO	$\overline{LOOP}$ at 0.8 V, TXEN at 2 V, See Figure 13		30	ns
t_{PHL} Propagation delay time, high-to-low level output	TXI	R XO	$\overline{LOOP}$ at 0.8 V, TXEN at 2 V, See Figure 13		30	ns
t_{PLH} Propagation delay time, low-to-high level output	TXEN	R XEN	$\overline{LOOP}$ at 0.8 V, See Figure 14		50	ns
t_{PHL} Propagation delay time, high-to-low level output	TXEN	R XEN	$\overline{LOOP}$ at 0.8 V, See Figure 14		50	ns



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PARAMETER MEASUREMENT INFORMATION

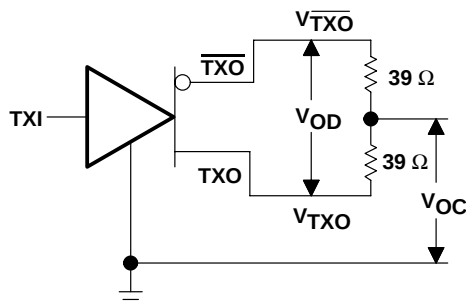


Figure 1. Driver Test Circuit

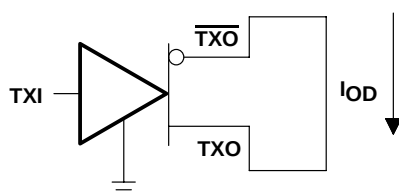
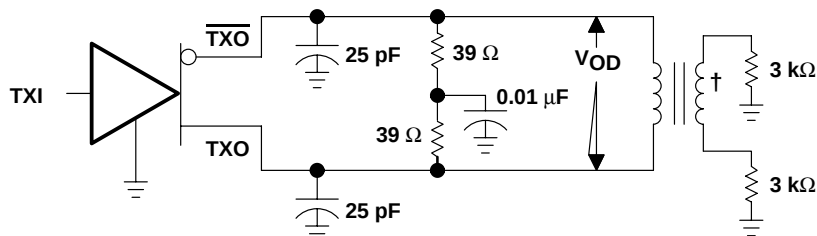
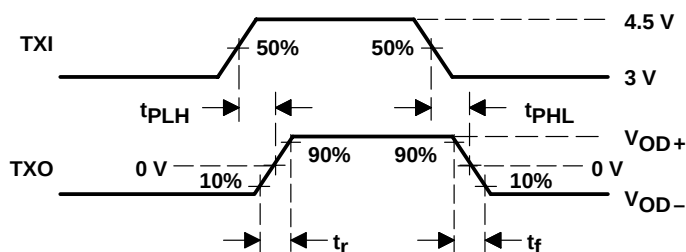


Figure 2. Driver Test Circuit



TEST CIRCUIT



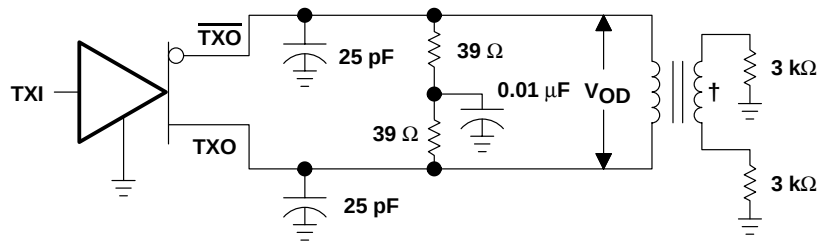
VOLTAGE WAVEFORMS

† Transformer specifications:

Turns ratio	1:1
Magnetizing inductance	26 to 30 μ H
Winding resistance	0.6 Ω Max
Rise time 10% to 90%	5 ns Max
Interwinding capacitance	25 pF
Leakage inductance	0.25 μ H Max
Inductive Q	1250 Min

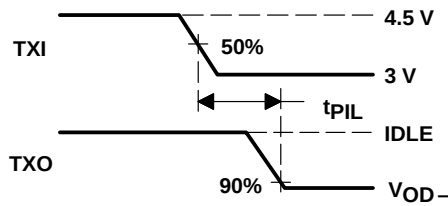
Figure 3. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

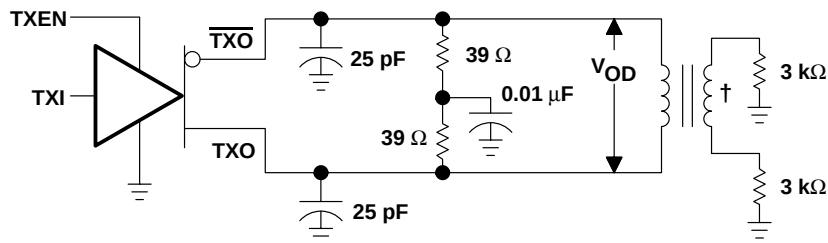
† See Figure 3



VOLTAGE WAVEFORMS

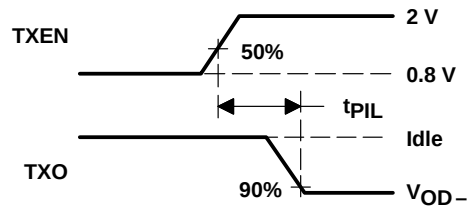
NOTE A: Input $t_r \leq 5$ ns; $t_f \leq 5$ ns

Figure 4. Test Circuit and Voltage Waveforms



TEST CIRCUIT

† See Figure 3



VOLTAGE WAVEFORMS

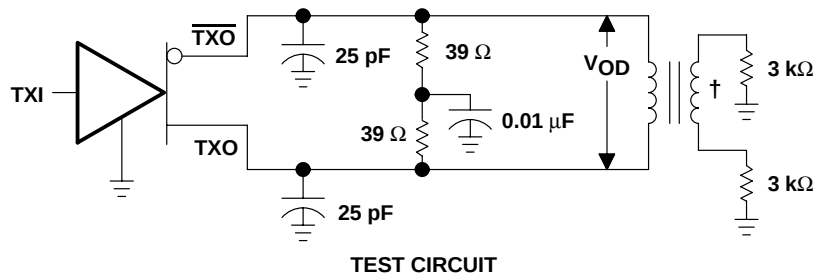
Figure 5. Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION



† See Figure 3

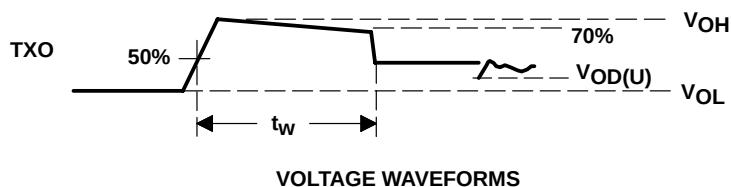


Figure 6. Test Circuit and Voltage Waveforms

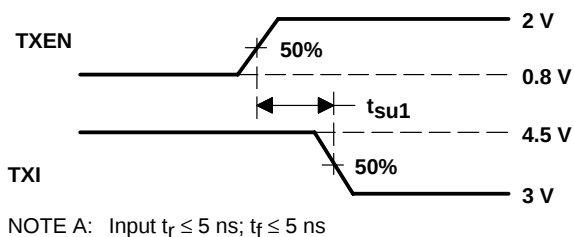


Figure 7

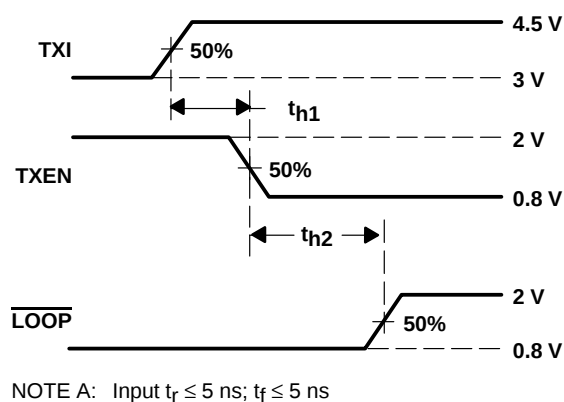


Figure 8

PARAMETER MEASUREMENT INFORMATION

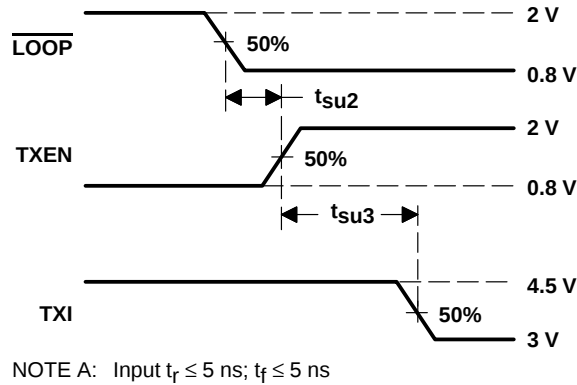


Figure 9

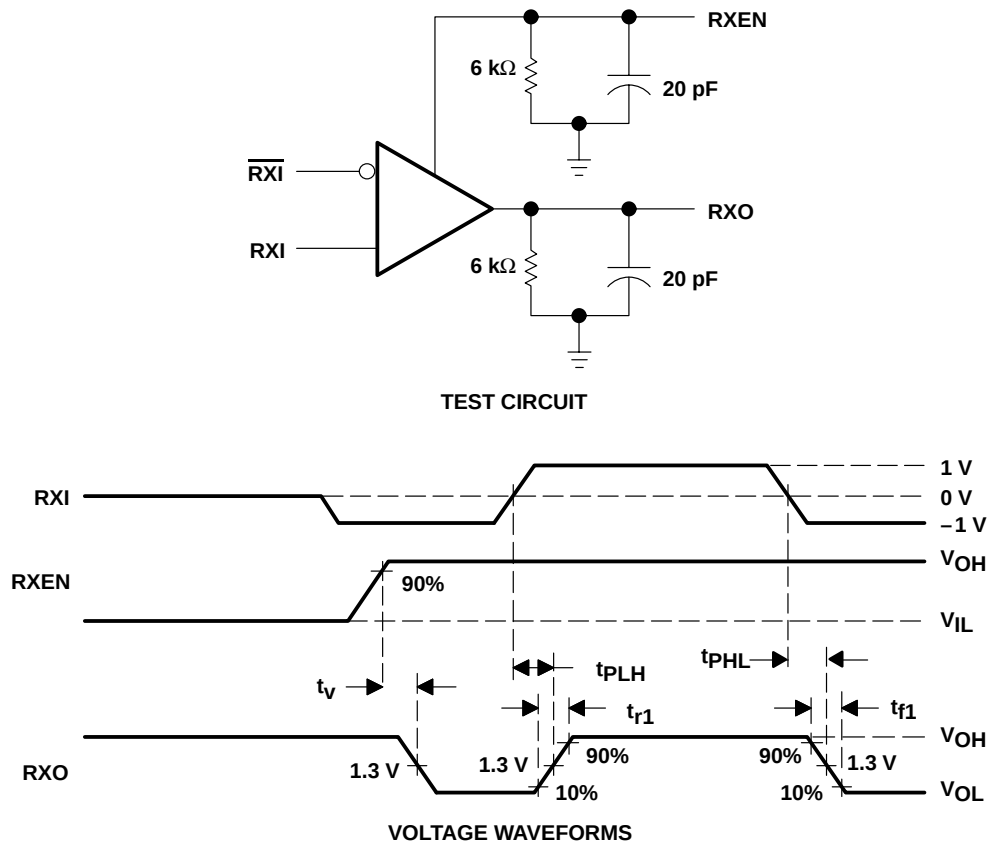
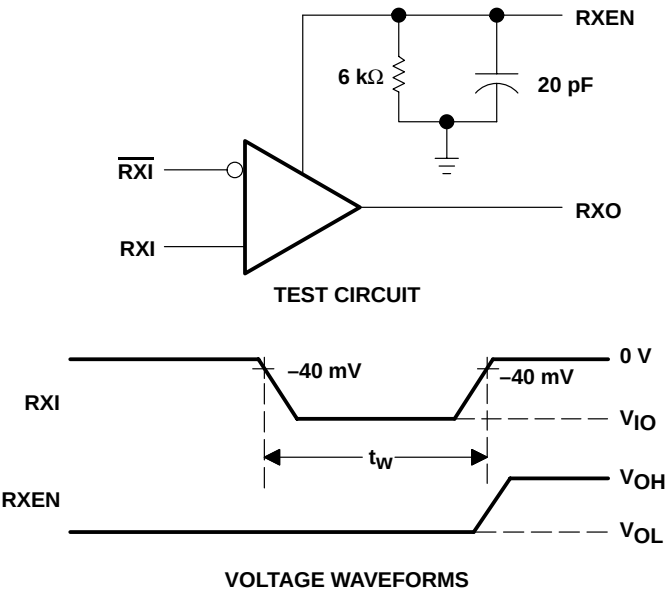


Figure 10. Test Circuit and Voltage Waveforms

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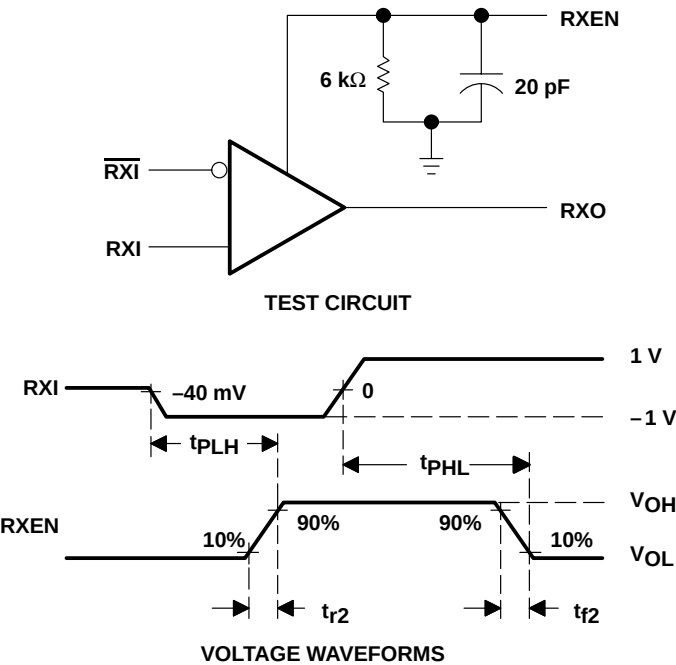
SLLS054D – APRIL 1989 – REVISED OCTOBER 2001

PARAMETER MEASUREMENT INFORMATION



NOTE A: Input $t_r \leq 5\text{ ns}$; $t_f \leq 5\text{ ns}$

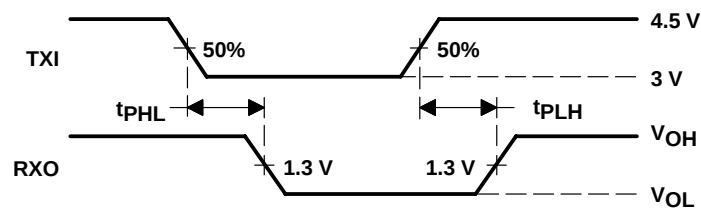
Figure 11. Test Circuit and Voltage Waveforms



NOTE A: Input $t_r \leq 5\text{ ns}$; $t_f \leq 5\text{ ns}$

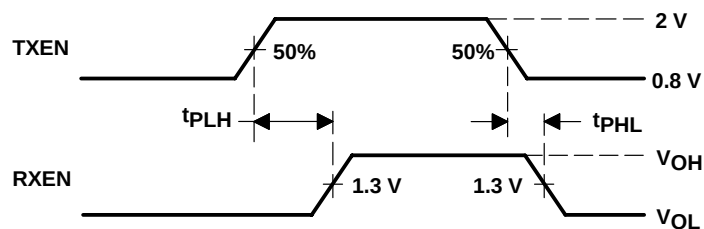
Figure 12. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: Input $t_r \leq 5$ ns; $t_f \leq 5$ ns

Figure 13



NOTE A: Input $t_r \leq 5$ ns; $t_f \leq 5$ ns

Figure 14

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75ALS085DW	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS085
SN75ALS085DW.A	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS085

- ⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).
- ⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- ⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- ⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- ⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- ⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE

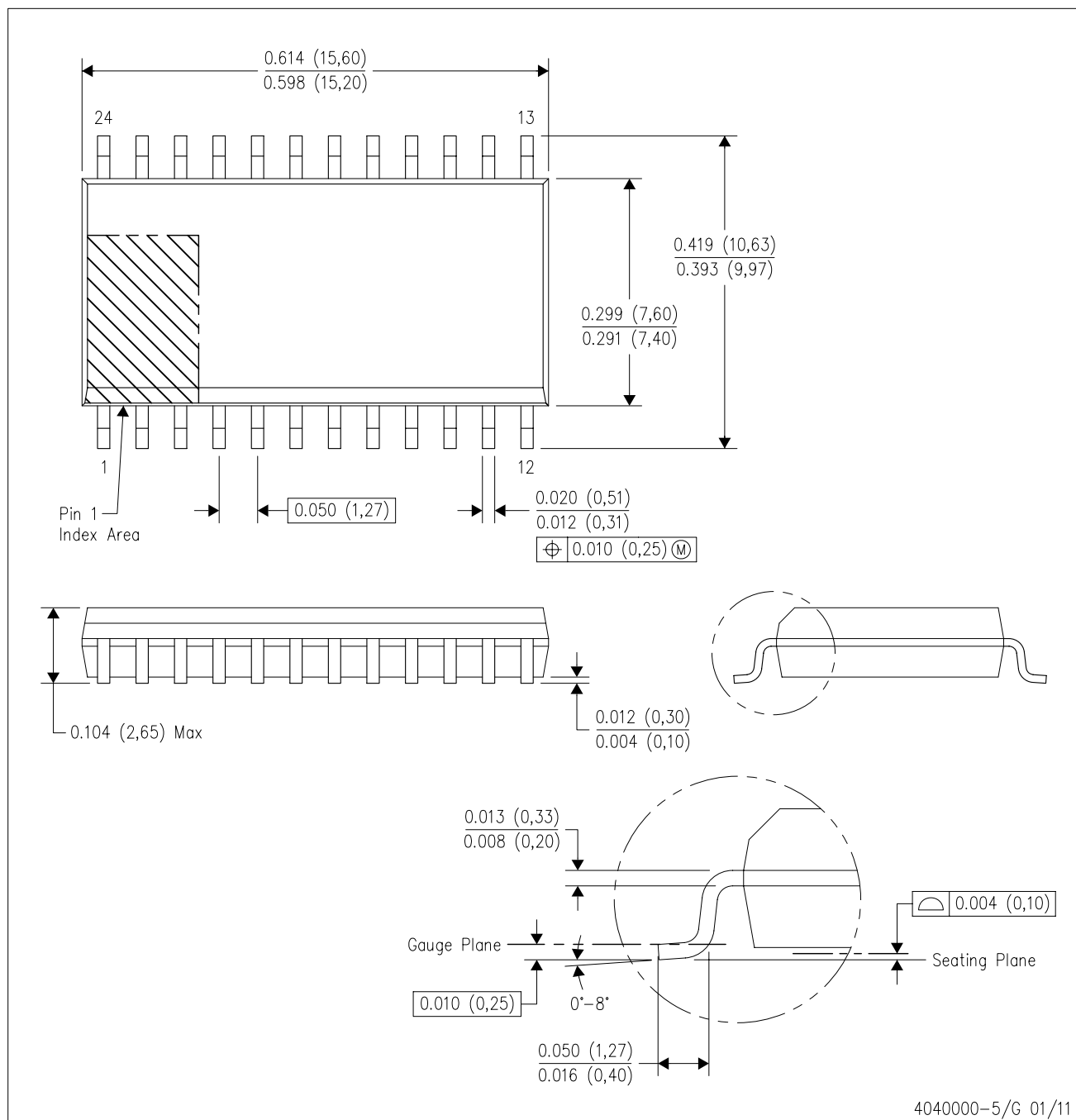


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75ALS085DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN75ALS085DW.A	DW	SOIC	24	25	506.98	12.7	4826	6.6

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

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