# 8P79208

Low Additive Jitter 2:8 Buffer with CMOS/ Differential Outputs

The 8P79208 is intended to take 1 or 2 reference clocks, select between them, using a pin selection and generate up to eight differential outputs or sixteen LVCMOS outputs that are the same as the reference frequency.

The 8P79208 supports two output banks, each with its own power supply. Each bank is separately controlled. Please refer to Table 4 for details.

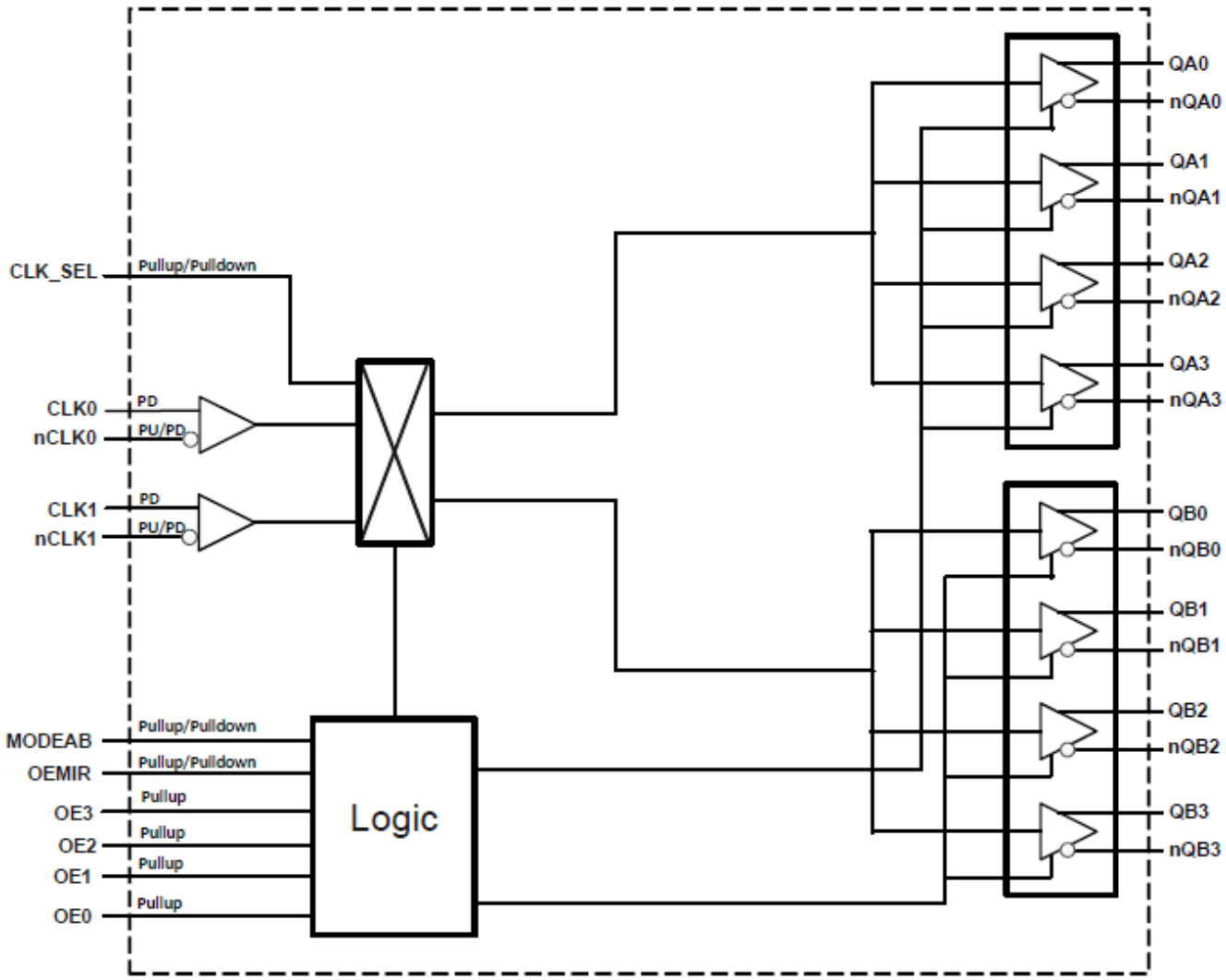
## Features

- Two differential inputs support LVPECL, LVDS, LVHSTL, HCSL or LVCMOS reference clocks
- Accepts input frequencies up to 700MHz
- Select which of the two input clocks is to be used as the reference clock for which bank via pin selection
- Generates 8 differential or 16 LVCMOS outputs
- Differential outputs LVPECL, LVDS
- Differential outputs support frequencies up to 700MHz
- LVCMOS outputs support frequencies up to 160MHz
- Each bank supports a separate power supply of 3.3V, 2.5V or 1.8V
- 1.5V output voltage is also supported for LVCMOS only
- Controlled by 3-level input pins
- Input mux selection control pin
- Output noise floor of -160dBc/Hz at 156.25MHz
- Core voltage supply of 3.3V, 2.5V or 1.8V
- Supports case temperature up to 105°C
- Lead-free (RoHS 6) packaging

# Contents

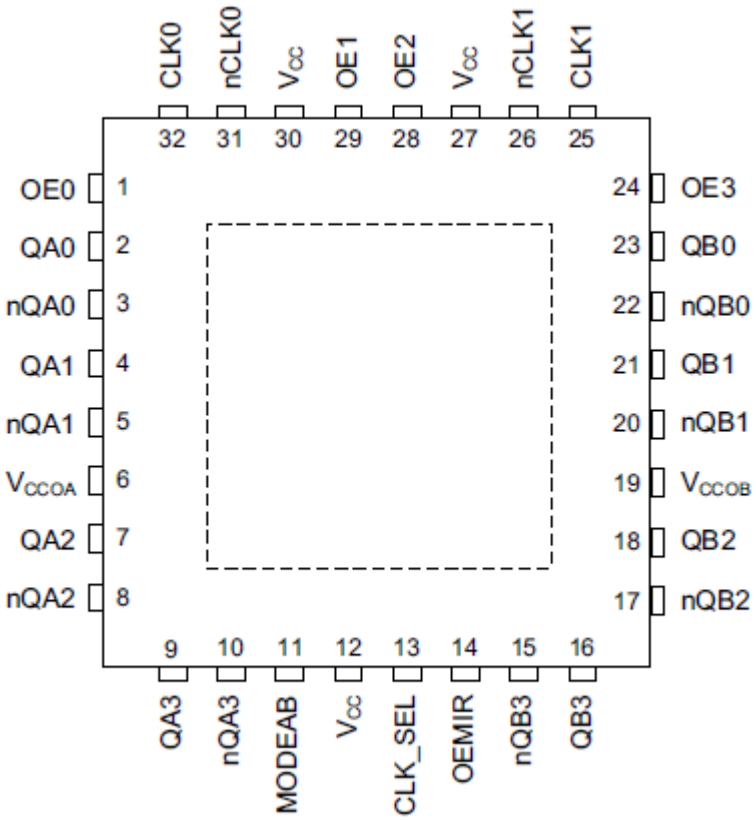
# 1. Overview

## 1.1 Block Diagram



# 2. Pin Information

## 2.1 Pin Assignments




**5 x 5 mm, 32- VFQFN Package, Top View**

## 2.2 Pin Descriptions

**Table 1. Pin Descriptions**

| Number | Name | Type[1] | | Description |
|---|---|---|---|---|
| 1 | OE0 | Input | Pull-up | Controls output enable for QA0 & QB0. LVCMOS/LVTTL input levels. |
| 2 | QA0 | Output | | Positive differential clock output. Included in Bank A. Refer to Output Drivers section for more details. |
| 3 | nQA0 | Output | | Negative differential clock output. Included in Bank A. Refer to Output Drivers section for more details. |
| 4 | QA1 | Output | | Positive differential clock output. Included in Bank A. Refer to Output Drivers section for more details. |
| 5 | nQA1 | Output | | Negative differential clock output. Included in Bank A. Refer to Output Drivers section for more details. |
| 6 | $V_{CCOA}$ | Power | | Output voltage supply for Output Bank A. |
| 7 | QA2 | Output | | Positive differential clock output. Included in Bank A. Refer to Output Drivers section for more details. |
| 8 | nQA2 | Output | | Negative differential clock output. Included in Bank A. Refer to Output Drivers section for more details. |

| Number | Name | Type[1] | | Description |
|---|---|---|---|---|
| 9 | QA3 | Output | | Positive differential clock output. Included in Bank A. Refer to Output Drivers section for more details. |
| 10 | nQA3 | Output | | Negative differential clock output. Included in Bank A. Refer to Output Drivers section for more details. |
| 11 | MODEAB | Input | Pull-up / Pull-down | Controls output mode functions for Bank A and B. 3-level input. |
| 12 | $V_{CC}$ | Power | | Core Logic voltage supply. |
| 13 | CLK_SEL | Input | Pull-up / Pull-down | Input Clock Selection Control pin. 3-level input. This pin's function is described in the Input Selection section. |
| 14 | OEMIR | Input | Pull-up / Pull-down | Controls output enable mode functions. 3-level input. |
| 15 | nQB3 | Output | | Negative differential clock output. Included in Bank B. Refer to Output Drivers section for more details. |
| 16 | QB3 | Output | | Positive differential clock output. Included in Bank B. Refer to Output Drivers section for more details. |
| 17 | nQB2 | Output | | Negative differential clock output. Included in Bank B. Refer to Output Drivers section for more details. |
| 18 | QB2 | Output | | Positive differential clock output. Included in Bank B. Refer to Output Drivers section for more details. |
| 19 | $V_{CCOB}$ | Power | | Output voltage supply for Output Bank B. |
| 20 | nQB1 | Output | | Negative differential clock output. Included in Bank B. Refer to Output Drivers section for more details. |
| 21 | QB1 | Output | | Positive differential clock output. Included in Bank B. Refer to Output Drivers section for more details. |
| 22 | nQB0 | Output | | Negative differential clock output. Included in Bank B. Refer to Output Drivers section for more details. |
| 23 | QB0 | Output | | Positive differential clock output. Included in Bank B. Refer to Output Drivers section for more details. |
| 24 | OE3 | Input | Pull-up | Controls output enable for QA3 and QB3. LVCMOS/LVTTL input levels. |
| 25 | CLK1 | Input | Pull-down | Non-inverting differential clock input. |
| 26 | nCLK1 | Input | Pull-up / Pull-down | Inverting differential clock input. VCC/2 when left floating (set by the internal pull-up and pull-down resistors). |
| 27 | VCC | Power | | Core Logic voltage supply. |
| 28 | OE2 | Input | Pull-up | Controls output enable for QA2 and QB2. LVCMOS/LVTTL input levels. |
| 29 | OE1 | Input | Pull-up | Controls output enable for QA1 and QB1. LVCMOS/LVTTL input levels. |
| 30 | VCC | Power | | Core Logic voltage supply. |
| 31 | nCLK0 | Input | Pull-up / Pull-down | Inverting differential clock input. VCC/2 when left floating (set by the internal pull-up and pull-down resistors). |
| 32 | CLK0 | Input | Pull-down | Non-inverting differential clock input. |
| EP | VEE | Ground | | Exposed pad must be connected to GND. |

1. Pull-up and Pull-down refer to internal input resistors. See Table 2 for typical values.

**Table 2. Pin Characteristics**

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | | 2 | | pF |
| $R_{PULLUP}$ | Input Pull-up Resistor | | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input Pull-down Resistor | | | | 51 | | kΩ |
| $C_{PD}$ | Power Dissipation Capacitance | | LVCMOS Output type selected $V_{CCOx}$ [1] = 3.3V ±5% | | 10 | | pF |
| | | | LVCMOS Output type selected $V_{CCOx}$[1] = 2.5V ±5% | | 14 | | pF |
| | | | LVCMOS Output type selected $V_{CCOx}$[1] = 1.8V±5% | | 10 | | pF |
| | | | LVCMOS Output type selected $V_{CCOx}$[1] = 1.5V ±5% | | 9 | | pF |
| $R_{OUT}$ | Output Impedance | QA[3:0], nQA[3:0], QB[3:0], nQB[3:0] | LVCMOS Output type selected $V_{CCOx}$[1] = 3.3V ±5% | | 22 | | Ω |
| | | | LVCMOS Output type selected $V_{CCOx}$[1] = 2.5V ±5% | | 29 | | Ω |
| | | | LVCMOS Output type selected $V_{CCOx}$[1] = 1.8V ±5% | | 22 | | Ω |
| | | | LVCMOS Output type selected $V_{CCOx}$[1] = 1.5V ±5% | | 41 | | Ω |

1. VCCOx refers to VCCOA for QA[3:0], nQA[3:0] or VCCOB for QB[3:0], nQB[3:0].

# 3. Principals of Operation

## 3.1 Input Selection

The 8P79208 supports two input references: CLK0 and CLK1 that may be driven with differential or single-ended clock signals. Either may be used as the source frequency for either or both output banks under control of the CLK_SEL input pin.

**Table 3. Input Selection Control**

| CLK_SEL | Description |
|---|---|
| High | Banks A and B Both Driven from CLK1 |
| Middle[1] | Bank A Driven from CLK0 and Bank B Driven from CLK1 |
| Low | Banks A and B Both Driven from CLK0 |

1. A '"middle" voltage level is defined in Table 10. Leaving the input pin open will also generate this level via a weak internal resistor network.

## 3.2 Output Drivers

The QA[0:3] and QB[0:3] clock outputs are provided with pin-controlled output drivers. The following table shows how each bank can be controlled.

**Table 4. Output Mode and Enable Control**

| OEMIR | MODEAB | OEn[1] | Bank A Mode | Bank B Mode |
|---|---|---|---|---|
| High | High | High | LVCMOS | LVCMOS |
| High | High | Low | Hi-Z | Hi-Z |
| High | Middle | High | LVPECL | LVPECL |
| High | Middle | Low | Hi-Z | Hi-Z |
| High | Low | High | LVDS | LVDS |
| High | Low | Low | Hi-Z | Hi-Z |
| Middle | High | High | LVDS | LVDS |
| Middle | High | Low | LVDS[2] | Hi-Z |
| Middle | Middle | High | LVCMOS | LVDS |
| Middle | Middle | Low | Hi-Z | Hi-Z |
| Middle | Low | High | LVCMOS | LVCMOS |
| Middle | Low | Low | Hi-Z | Hi-Z |
| Low | High | High | LVCMOS | LVPECL |
| Low | High | Low | LVCMOS[2] | Hi-Z |
| Low | Middle | High | LVPECL | LVPECL |
| Low | Middle | Low | LVPECL[2] | Hi-Z |
| Low | Low | High | LVDS | LVPECL |
| Low | Low | Low | LVDS[2] | Hi-Z |

1. OE0 affects QA0 and QB0, OE1 affects QA1 and QB1, OE2 affects QA2 and QB2, OE3 affects QA3 and QB3 as indicated in the Bank A and Bank B Mode columns.
2. In this case, Bank A outputs (QA[3:0]) will be enabled regardless of the state of the OE[3:0] pins.

### 3.2.1. LVCMOS Operation

When a given output is configured to provide LVCMOS levels, then both the Q and nQ outputs will toggle at the selected output frequency. All the previously described configuration and control apply equally to both outputs. Frequency, voltage levels and enable / disable status apply to both the Q and nQ pins. When configured as LVCMOS, the Q and nQ outputs are in-phase relative to one another. The maximum operating frequency in LVCMOS operation may differ for different VCCOX levels. Please consult Table 18 for details.

# 4. Specifications

## 4.1 Absolute Maximum Ratings

**CAUTION**: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

**Table 5. Absolute Maximum Ratings**

| Item | Rating |
|---|---|
| Supply Voltage, $V_{CCX}$ [1] to GND | 3.6V |
| Inputs OEMIR, OE[3:0], MODEAB, CLK_SEL, CLK0, nCLK0, CLK1, nCLK1 | -0.5V to 3.6V |
| Outputs, $I_O$ QA[0:3], nQA[0:3]; QB[0:3], nQB[0:3]<br>Continuous Current Surge Current | 40mA<br>60mA |
| Outputs, $V_O$ QA[0:3], nQA[0:3]; QB[0:3], nQB[0:3] | -0.5V to 3.6V |
| Operating Junction Temperature | 125°C |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |
| Lead Temperature (Soldering, 10s) | +260°C |

1. $V_{CCX}$ denotes $V_{CC}$, $V_{CCOA}$, or $V_{CCOB}$.

## 4.2 Supply Voltage Characteristics

**Table 6. Power Supply Characteristics, $V_{CC}$ = $V_{CCOA}$ = $V_{CCOB}$ = 3.3V ±5%, $V_{EE}$ = 0V, $T_A$ = -40°C to +85°C, $T_C$ ≤ +105°C**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{CC}$ | Core Supply Current | | | 18 | 26 | mA |
| $I_{EE}$ | Power Supply Current [1] | All Outputs Configured for LVDS Logic Levels; Outputs Unloaded | | 150 | 174 | mA |

1. Internal dynamic switching current at maximum $f_{OUT}$ is included.

**Table 7. Power Supply Characteristics, $V_{CC}$ = $V_{CCOA}$ = $V_{CCOB}$ = 2.5V ±5%, $V_{EE}$ = 0V, $T_A$ = -40°C to +85°C, $T_C$ ≤ +105°C**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $I_{CC}$ | Core Supply Current | | | 16 | 20 | mA |
| $I_{EE}$ | Power Supply Current [1] | All Outputs Configured for LVDS Logic Levels; Outputs Unloaded | | 148 | 170 | mA |

1. Internal dynamic switching current at maximum $f_{OUT}$ is included.

**Table 8. Power Supply Characteristics, $V_{CC}$ = $V_{CCOA}$ = $V_{CCOB}$ = 2.5V ±5%, $V_{EE}$ = 0V, $T_A$ = -40°C to +85°C, $T_C$ ≤ +105°C**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | | 1.71 | 1.8 | 1.89 | V |
| $I_{CC}$ | Core Supply Current | | | 13 | 17 | mA |
| $I_{EE}$ | Power Supply Current [1] | All Outputs Configured for LVDS Logic Levels; Outputs Unloaded | | 131 | 160 | mA |

1. Internal dynamic switching current at maximum $f_{OUT}$ is included.

**Table 9. Typical Output Supply Current, $V_{CC}$ = 3.3V, 2.5V or 1.8V, $V_{EE}$ = 0V, $T_A$ = 25°C**

| Symbol | Parameter [1] | Test Conditions [2] | $V_{CCOx}$[3] = 3.3V | | | $V_{CCOx}$[3] = 2.5V | | | $V_{CCOx}$[3] = 1.8V $V_{CCOx}$ | | | $V_{CCOx}$[3] = 1.5V | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | LVDS | LVPECL | LVCMOS | LVDS | LVPECL | LVCMOS | LVDS | LVPECL | LVCMOS | LVCMOS | |
| $I_{CCOB}$ | Bank B Output Supply Current | All Outputs Enabled | 67 | 45 | 88 | 66 | 44 | 60 | 59 | 39 | 50 | 35 | mA |
| | | 3 Outputs Enabled | 55 | 39 | 70 | 54 | 38 | 49 | 49 | 33 | 41 | 29 | mA |
| | | 2 Outputs Enabled | 43 | 32 | 52 | 42 | 31 | 38 | 38 | 28 | 33 | 22 | mA |
| | | 1 Output Enabled | 32 | 26 | 35 | 30 | 25 | 27 | 28 | 22 | 24 | 16 | mA |
| | | No Outputs Enabled | 20 | 20 | 18 | 18 | 18 | 16 | 17 | 17 | 15 | 9 | mA |
| $I_{CCOA}$ | Bank A Output Supply Current | All Outputs Enabled | 67 | 45 | 88 | 66 | 44 | 60 | 59 | 39 | 50 | 35 | mA |
| | | 3 Outputs Enabled | 55 | 39 | 70 | 54 | 38 | 49 | 49 | 33 | 41 | 29 | mA |
| | | 2 Outputs Enabled | 43 | 32 | 52 | 42 | 31 | 38 | 38 | 28 | 33 | 22 | mA |
| | | 1 Output Enabled | 32 | 26 | 35 | 30 | 25 | 27 | 28 | 22 | 24 | 16 | mA |
| | | No Outputs Enabled | 20 | 20 | 18 | 18 | 18 | 16 | 17 | 17 | 15 | 9 | mA |

1. Internal dynamic switching current at maximum $f_{OUT}$ is included.
2. Tested with outputs unloaded.
3. $V_{CCOx}$ denotes $V_{CCOA}$, $V_{CCOB}$.

## 4.3 DC Electrical Specifications

**Table 10. LVCMOS/LVTTL Control / Status Signals DC Characteristics for 3-Level Pins, $V_{CC}$ = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, $V_{EE}$ = 0V, $T_A$ = -40°C to +85°C, $T_C$ ≤ +105°C**

| Symbol | Parameter | Signals | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | CLK_SEL, OEMIR, MODEAB | $V_{CC}$ = 3.3V | 0.85* $V_{CC}$ | | 3.465 | V |
| | | | $V_{CC}$ = 2.5V | 0.85* $V_{CC}$ | | 2.625 | V |
| | | | $V_{CC}$ = 1.8V | 0.85* $V_{CC}$ | | 1.89 | V |
| $V_{IM}$ | Input Middle Voltage[1] | CLK_SEL, OEMIR, MODEAB | $V_{CC}$ = 3.3V | 0.45* $V_{CC}$ | | 0.55* $V_{CC}$ | V |
| | | | $V_{CC}$ = 2.5V | 0.45* $V_{CC}$ | | 0.55* $V_{CC}$ | V |
| | | | $V_{CC}$ = 1.8V | 0.45* $V_{CC}$ | | 0.55* $V_{CC}$ | V |
| $V_{IL}$ | Input Low Voltage | CLK_SEL, OEMIR, MODEAB | $V_{CC}$ = 3.3V | -0.3 | | 0.15* $V_{CC}$ | V |
| | | | $V_{CC}$ = 2.5V | -0.3 | | 0.15* $V_{CC}$ | V |
| | | | $V_{CC}$ = 1.8V | -0.3 | | 0.15* $V_{CC}$ | V |
| $I_{IH}$ | Input High Current | CLK_SEL, OEMIR, MODEAB | $V_{CC}$ = $V_{IN}$ = 3.465V or 2.625V or 1.89V | | | 150 | µA |
| $I_{IM}$ | Input Middle Current | CLK_SEL, OEMIR, MODEAB | $V_{CC}$ = 3.465V or 2.625V or 1.89V, $V_{IN}$ = $V_{CC}$ /2 | | 0 | | µA |
| $I_{IL}$ | Input Low Current | CLK_SEL, OEMIR, MODEAB | $V_{CC}$ = 3.465V or 2.625V or 1.89V, $V_{IN}$ = 0V | -150 | | | µA |

1. For 3-level input pins, a mid-level voltage is used to select the 3rd state. This voltage will be maintained by a weak internal pull-up / pull-down network for each pin to select this state if the pin is left open. It is recommended that any external resistor networks used to select a middle-level input voltage be terminated to the device's core VCC voltage level.

**Table 11. LVCMOS/LVTTL Control / Status Signals DC Characteristics for 2-Level Pins, $V_{CC}$ = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, $V_{EE}$ = 0V, $T_A$ = -40°C to +85°C, $T_C$ ≤ +105°C**

| Symbol | Parameter | Signals | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | OE[3:0] | $V_{CC}$ = 3.3V | 2 | | 3.465 | V |
| | | | $V_{CC}$ = 2.5V | 1.7 | | 2.625 | V |
| | | | $V_{CC}$ = 1.8V | 0.65* $V_{CC}$ | | 1.89 | V |
| $V_{IL}$ | Input Low Voltage | OE[3:0] | $V_{CC}$ = 3.3V | -0.3 | | 0.8 | V |
| | | | $V_{CC}$ = 2.5V | -0.3 | | 0.7 | V |
| | | | $V_{CC}$ = 1.8V | -0.3 | | 0.35* $V_{CC}$ | V |
| $I_{IH}$ | Input High Current | OE[3:0] | $V_{CC}$ = $V_{IN}$ = 3.465V or 2.625V or 1.89V | | | 10 | µA |
| $I_{IL}$ | Input Low Current | OE[3:0] | $V_{CC}$ = $V_{IN}$ = 3.465V or 2.625V or 1.89V | -150 | | | µA |

**Table 12. Differential Input DC Characteristics, $V_{CC}$ = 3.3V ±5%, 2.5V ±5% or 1.8V±5%, $V_{EE}$ = 0V, $T_A$ = -40°C to +85°C, $T_C$ ≤ +105°C**

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | CLKx, nCLKx [1] | $V_{CC}$ = $V_{IN}$ = 3.465V or 2.625V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | CLKx [1] | $V_{CC}$ = 3.465V or 2.625V, $V_{IN}$ = 0V | -5 | | | µA |
| | | nCLKx [1] | $V_{CC}$ = 3.465V or 2.625V, $V_{IN}$ = 0V | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Voltage [2] | | | 0.15 | | 1.3 | V |
| $V_{CMR}$ | Common Mode Input Voltage [3] | | | $V_{EE}$ | | $V_{CC}$ -1.2 | V |

1. CLKx denotes CLK0, CLK1. nCLKx denotes nCLK0, nCLK1.
2. $V_{IL}$ should not be less than -0.3V. $V_{IH}$ should not be higher than $V_{CC}$.
3. Common mode voltage is defined as the crosspoint.

**Table 13. LVPECL DC and AC Characteristics, $V_{CC}$ = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, $V_{EE}$ = 0V, $T_A$ = -40°C to+85°C**

| Symbol | Parameter | | $V_{CCOx}$ [1] = 3.3V ±5% | | | $V_{CCOx}$ [1] = 2.5V ±5% | | | $V_{CCOx}$ [1] = 1.8V ±5% | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{OH}$ | Output High Voltage [2] | Qx, nQx[3] | $V_{CCOx}$ - 1.30 | | $V_{CCOx}$ - 0.80 | $V_{CCOx}$ - 1.35 | | $V_{CCOx}$ - 0.80 | $V_{CCOx}$ - 1.50 | | $V_{CCOx}$ - 0.90 | V |
| $V_{OL}$ | Output Low Voltage | Qx, nQx[3] | $V_{CCOx}$ - 2.00 | | $V_{CCOx}$ - 1.75 | $V_{CCOx}$ - 2.00 | | $V_{CCOx}$ - 1.75 | $V_{EE}$ | | 0.25 | V |
| $V_{OUT}$ | Output Voltage Swing, $f_{OUT}$ < 500MHz | Qx, nQx[3] | 0.5 | 0.8 | 1.2 | 0.5 | 0.8 | 1.2 | 0.35 | 0.6 | 1.0 | V |
| | Output Voltage Swing, $f_{OUT}$ < 700MHz | Qx, nQx[3] | 0.3 | 0.65 | 1.05 | 0.3 | 0.65 | 1.05 | 0.25 | 0.45 | 0.7 | V |

1. $V_{CCOx}$ denotes $V_{CCOA}$ and $V_{CCOB}$.
2. Outputs terminated with 50Ω to $V_{CCOx}$ – 2V when $V_{CCOx}$ = 3.3V ±5% or 2.5V ±5%. Outputs terminated with 50Ω to ground when VCCOx = 1.8V ±5%.
3. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3. nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

**Table 14. LVDS DC and AC Characteristics, $V_{CC}$ = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, $V_{CCOA}$ = $V_{CCOB}$ = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, $T_A$ = -40°C to +85°C**

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{OD}$ | Differential output voltage | Qx, nQx[1] | Terminated 100Ω across Qx and nQx | 247 | | 480 | mV |
| $\Delta V_{OD}$ | $V_{OD}$ magnitude change | Qx, nQx[1] | | | | 50 | mV |
| $V_{OS}$ | Offset voltage | Qx, nQx[1] | | 1.125 | | 1.375 | V |
| $\Delta V_{OS}$ | $V_{OS}$ magnitude change | Qx, nQx[1] | | | | 50 | mV |

1. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3.nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

**Table 15. LVCMOS Clock Outputs DC Characteristics, $V_{CC}$ = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, $V_{EE}$ = 0V, $T_A$ = -40°C to +85°C, $T_C$ ≤ +105°C**

| Symbol | Parameter | Test Conditions | $V_{CCOx}$[1]= 3.3V±5% | | | $V_{CCOx}$[1]= 2.5V±5% | | | $V_{CCOx}$[1] = 1.8V ±5% | | | $V_{CCOx}$[1] = 1.5V ±5% | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{OH}$ | Output High Voltage Qx, nQxz[2] | $I_{OH}$ = -8mA | 2.4 | | | 1.8 | | | $V_{CC}$-0.45 | | | $V_{CC}$ -0.38 | | | V |
| $V_{OL}$ | Output Low Voltage Qx, nQx[2] | $I_{OL}$ = 8mA | | | 0.8 | | | 0.6 | | | 0.45 | | | 0.38 | V |

1. $V_{CCOx}$ denotes $V_{CCOA}$, $V_{CCOB}$.
2. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3. nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

## 4.4 AC Electrical Characteristics

**Table 16. AC Characteristics, $V_{CC}$ = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, $V_{CCOx}$[1] = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, $V_{EE}$ = 0V, $T_A$ = -40°C to +85°C, $T_C$ ≤ +105°C**

| Symbol | Parameter[2] | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | LVDS, LVPECL | | | | 700 | MHz |
| $f_{OUT}$ | Output Frequency | LVCMOS | $V_{CCOx}$ = 3.3V±5% or 2.5V±5% | | | 160 | MHz |
| | | | $V_{CCOx}$ = 1.8V±5% or 1.5V±5% | | | 130 | MHz |
| $t_R$ / $t_F$ | Output Rise and Fall Times | LVPECL | 20% to 80% | 100 | | 750 | ps |
| | | LVDS | 20% to 80%, $V_{CCOx}$ = 3.3V | 140 | | 550 | ps |
| | | | 20% to 80%, $V_{CCOx}$ = 2.5V | 100 | | 600 | ps |
| | | | 20% to 80%, $V_{CCOx}$ = 1.8V | 150 | | 650 | ps |
| | | LVCMOS | 20% to 80%, $V_{CCOx}$ = 3.3V | 240 | | 550 | ps |
| | | | 20% to 80%, $V_{CCOx}$ = 2.5V | 260 | | 550 | ps |
| | | | 20% to 80%, $V_{CCOx}$ = 1.8V | 320 | | 750 | ps |
| | | | 20% to 80%, $V_{CCOx}$ = 1.5V | 450 | | 1100 | ps |
| tsk(b) | Bank Skew[3][4] | LVPECL[5] | | | 10 | 45 | ps |
| | | LVDS[5] | | | 15 | 45 | ps |
| | | LVCMOS[6] | | | 40 | 85 | ps |
| $t_{sk}$(bb) | Bank-to-Bank Skew[3] [4] | LVPECL | Both banks with LVPECL outputs | | | 120 | ps |
| | | LVDS | Both banks with LVDS outputs | | | 100 | ps |
| odc | Output Duty Cycle[7] | LVPECL, LVDS | | 45 | | 55 | % |
| | | LVCMOS | $f_{OUT}$ ≤ 130MHz | 45 | | 55 | % |
| | | LVCMOS | 130MHz < $f_{OUT}$ ≤ 160MHz | 40 | | 60 | % |
| $MUX_{ISOL}$ | Mux Isolation | | | | 70 | | dB |
| | Noise Floor | | Offset >10MHz from 156.25MHz Carrier | | -160 | | dBc/Hz |
| $t_{startup}$ | Startup Time | | | | | 25 | ms |
| $t_{PD}$ | Propagation Delay | LVPECL | $V_{CCOx}$ = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% | 0.97 | | 1.76 | ns |
| | | LVDS | | 0.96 | | 1.73 | ns |
| | | LVCMOS | | 0.41 | | 4 | ns |

1. $V_{CCO}x$ denotes $V_{CCOA}$, $V_{CCOB}$.
2. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions
3. This parameter is confirmed by characterization. Not tested in production.
4. This parameter is defined in accordance with JEDEC Standard 65.
5. Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
6. Measured at the output differential crosspoint.
7. Measured at $V_{CCOx}$/2 of the rising edge.
8. Measured using 50% duty cycle on input reference.

**Table 17. Typical Additive Jitter, $V_{CC}$ = $V_{CCOx}$[1] = 3.3V, $V_{EE}$ = 0V, $T_A$ = 25°C**

| Symbol | Parameter | Test Conditions[2] | LVPECL | LVDS | LVCMOS | Units |
|---|---|---|---|---|---|---|
| $t_{jit}(f)$ | RMS Additive Jitter (Random) | $f_{OUT}$ = 122.88MHz, Integration Range: 12kHz–20MHz | 72 | 90 | 86 | fs |
| | | $f_{OUT}$ = 156.25MHz, Integration Range: 12kHz–20MHz | 50 | 64 | 64 | fs |
| | | $f_{OUT}$ = 622.08MHz, Integration Range: 12kHz–20MHz | 32 | 32 | N/A | fs |

1. $V_{CCO}x$ denotes $V_{CCOA}$, $V_{CCOB}$.
2. All outputs configured for the specific output type, as shown in the table.

# 5. Applications Information

## 5.1 Recommendations for Unused Input and Output Pins

### 5.1.1. Inputs

#### CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

#### LVCMOS LVTTL Level Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

#### LVCMOS 3-Level I/O Control Pins

These pins are 3-level pins and if left unconnected this is interpreted as a valid input selection option (Middle).

### 5.1.2. Outputs

#### LVCMOS Outputs

All unused LVCMOS outputs can be left floating. It is recommended that there is no trace attached.

#### LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

#### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100□ across. If they are left floating, there should be no trace attached

## 5.2 Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1$= $V_{CC}$/2 is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V1in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{CC}$ = 3.3V, R1 and R2 value should be adjusted to set $V_1$ at 1.25V. The values below are for when both the single ended swing and $V_{CC}$ are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced while maintaining an edge rate faster than 1V/ns. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however VIL cannot be less than -0.3V and $V_{IH}$ cannot be more than $V_{CC}$ + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

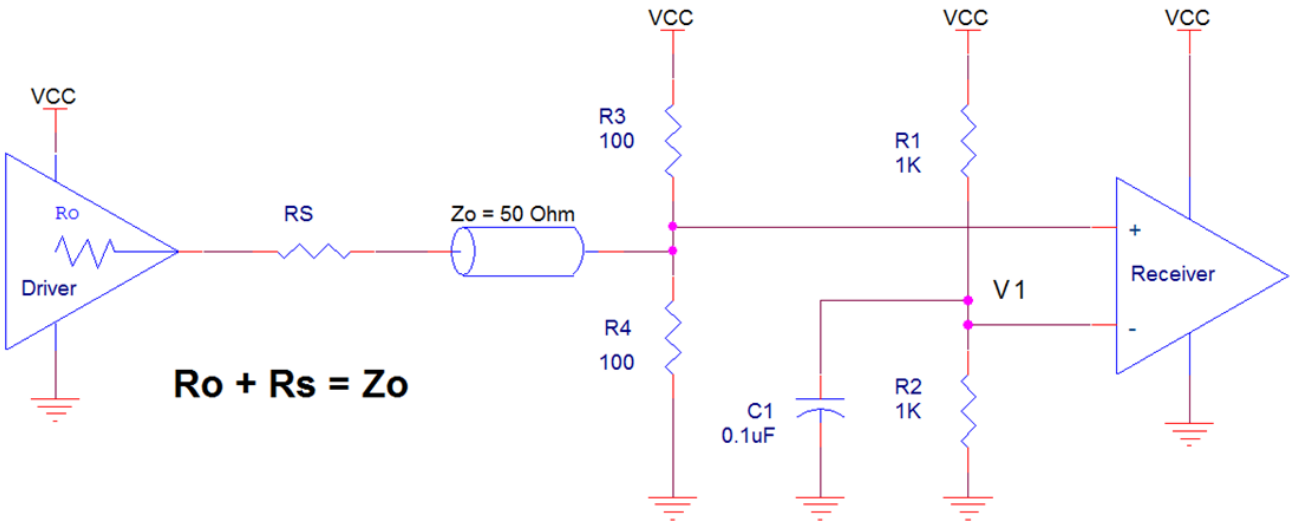



**Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-Ended Levels**

## 5.3 3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both VSWING and VOH must meet the VPP and VCMR input requirements. Figure 2 to Figure 5 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

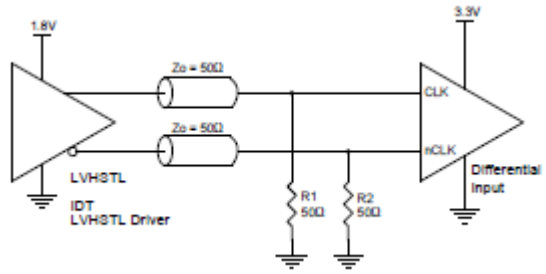



**Figure 2. CLK/nCLK Input Driven by an Open Emitter LVHSTL Driver**

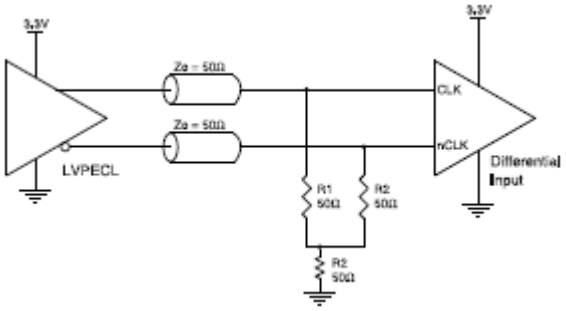



**Figure 3. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**

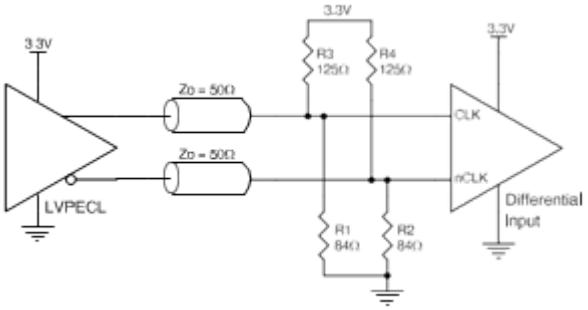



**Figure 4. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**

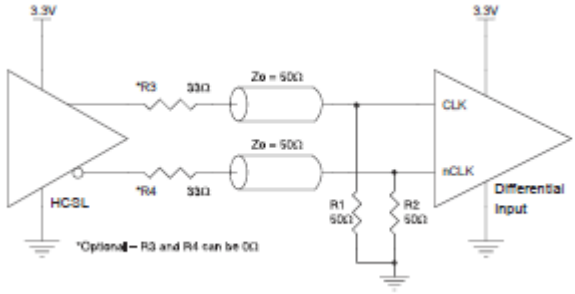



**Figure 5. CLK/nCLK Input Driven by a 3.3V HCSL Driver**

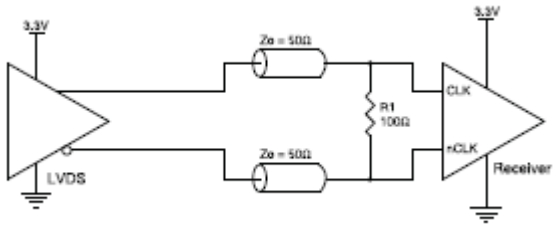



**Figure 6. CLK/nCLK Input Driven by a 3.3V LVDS Driver**

## 5.4 2.5V Differential Clock Input Interface

CLKx/nCLKx accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both $V_{SWING}$ and $V_{OH}$ must meet the VPP and VCMR input requirements. Figure 7 to Figure 10 show interface examples for the CLKx/nCLKx input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 7, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation

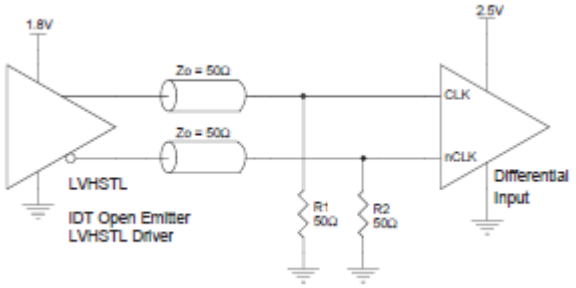



**Figure 7. CLKx/nCLKx Input Driven by an IDT Open Emitter LVHSTL Driver**

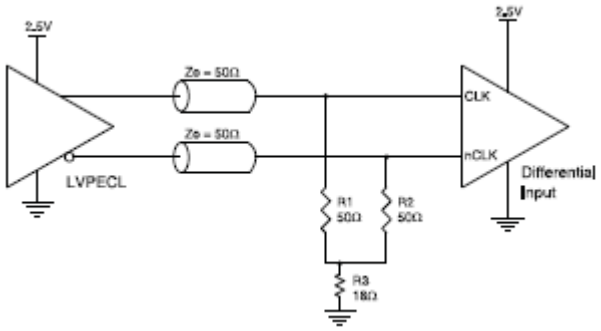



**Figure 8. CLKx/nCLKx Input Driven by a 2.5V LVPECL Driver**

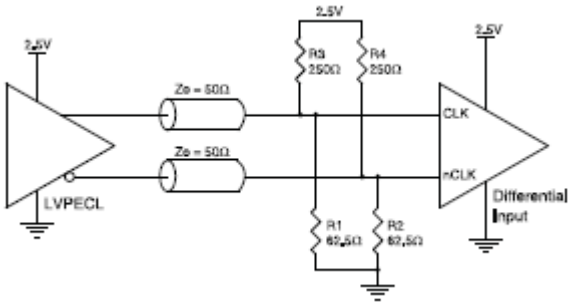



**Figure 9. CLKx/nCLKx Input Driven by a 2.5V LVPECL Driver**

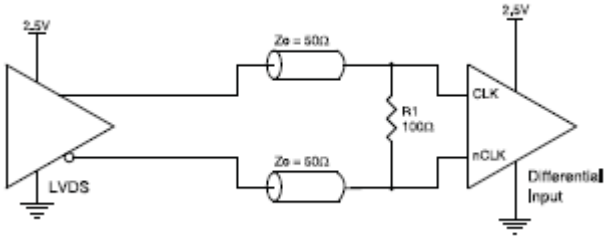



**Figure 10. CLKx/nCLKx Input Driven by a 2.5V LVDS Driver**

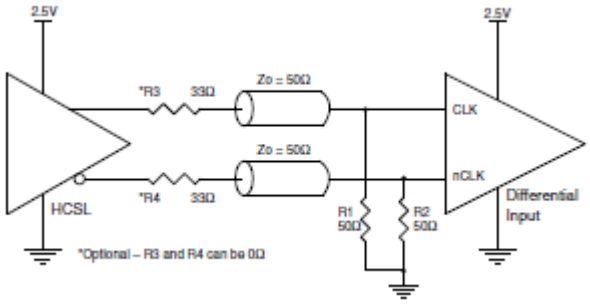



**Figure 11. CLKx/nCLKx Input Driven by a 2.5V HCSL Driver**

## 5.5 LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance ($Z_T$) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance ($Z_0$) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. Renesas offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 12 can be used with either type of output structure. Figure 13, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

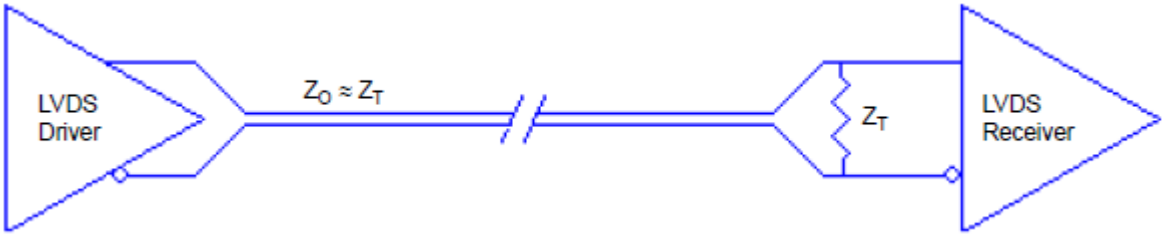



**Figure 12. Standard LVDS Termination**

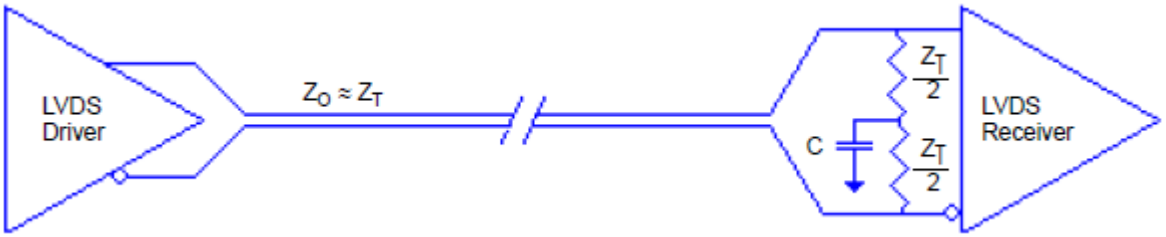



**Figure 13. Optional LVDS Termination**

## 5.6 Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential output is a low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines.

Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figure 14 and Figure 15 show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

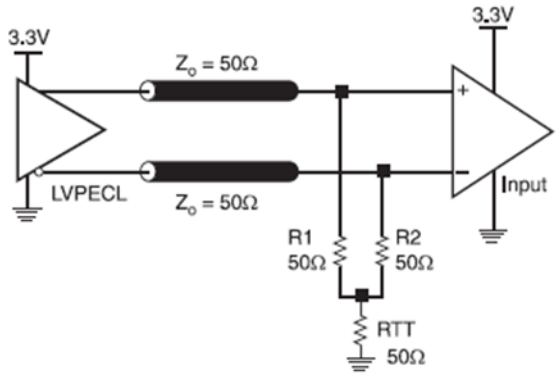



**Figure 14. 3.3V LVPECL Output Termination**

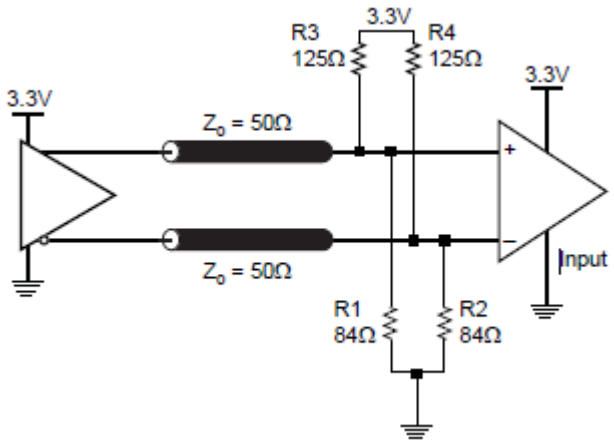



**Figure 15. 3.3V LVPECL Output Termination**

## 5.7 Termination for 2.5V LVPECL Outputs

Figure 16 and Figure 17 show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CCO}$ – 2V. For $V_{CCO}$ = 2.5V, the $V_{CCO}$ – 2V is very close to ground level. The R3 in Figure 17 can be eliminated and the termination is shown in Figure 18.

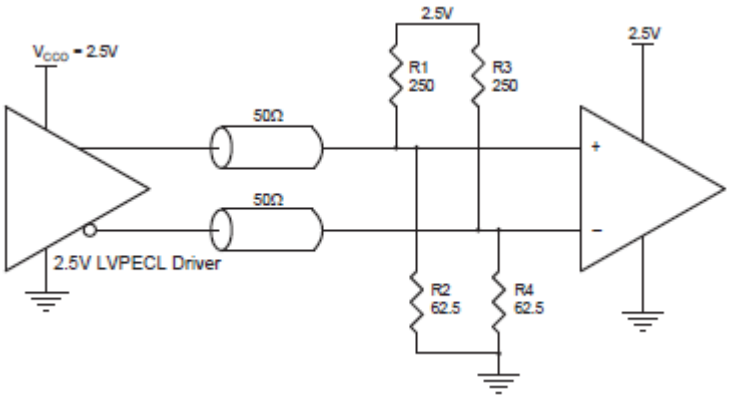



**Figure 16. 2.5V LVPECL Driver Termination Example**

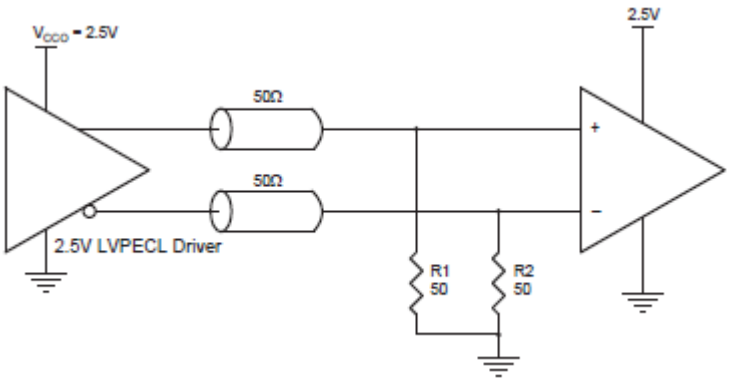



**Figure 17. 2.5V LVPECL Driver Termination Example**

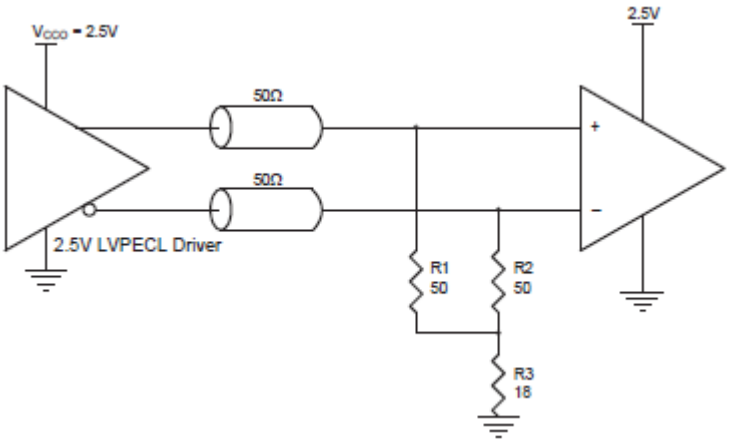



**Figure 18. 2.5V LVPECL Driver Termination Example**

# 6. Power Dissipation and Thermal Considerations

The 8P79208 is a multi-functional, high-speed device that targets a wide variety of clock frequencies and applications. Since this device is highly programmable with a broad range of features and functionality, the power consumption will vary as each of these features and functions is enabled.

The 8P79208 device was designed and characterized to operate within the ambient industrial temperature range of $T_A$ = -40°C to 85°C or $T_C$ ≤ 105°C. The ambient temperature represents the temperature around the device, not the junction temperature. When using the device in extreme cases, such as maximum operating frequency and high ambient temperature, external air flow may be required in order to ensure a safe and reliable junction temperature. Extreme care must be taken to avoid exceeding 125°C junction temperature.

The power calculation examples below were generated using a maximum ambient temperature and supply voltage. For many applications, the power consumption will be much lower. Please contact Renesas technical support for any concerns on calculating the power dissipation for your own specific configuration.

## 6.1 Power Domains

The 8P79208 device has a number of separate power domains that can be independently enabled and disabled via register accesses (all power supply pins must still be connected to a valid supply voltage). Figure 19 below indicates the individual domains and the associated power pins.

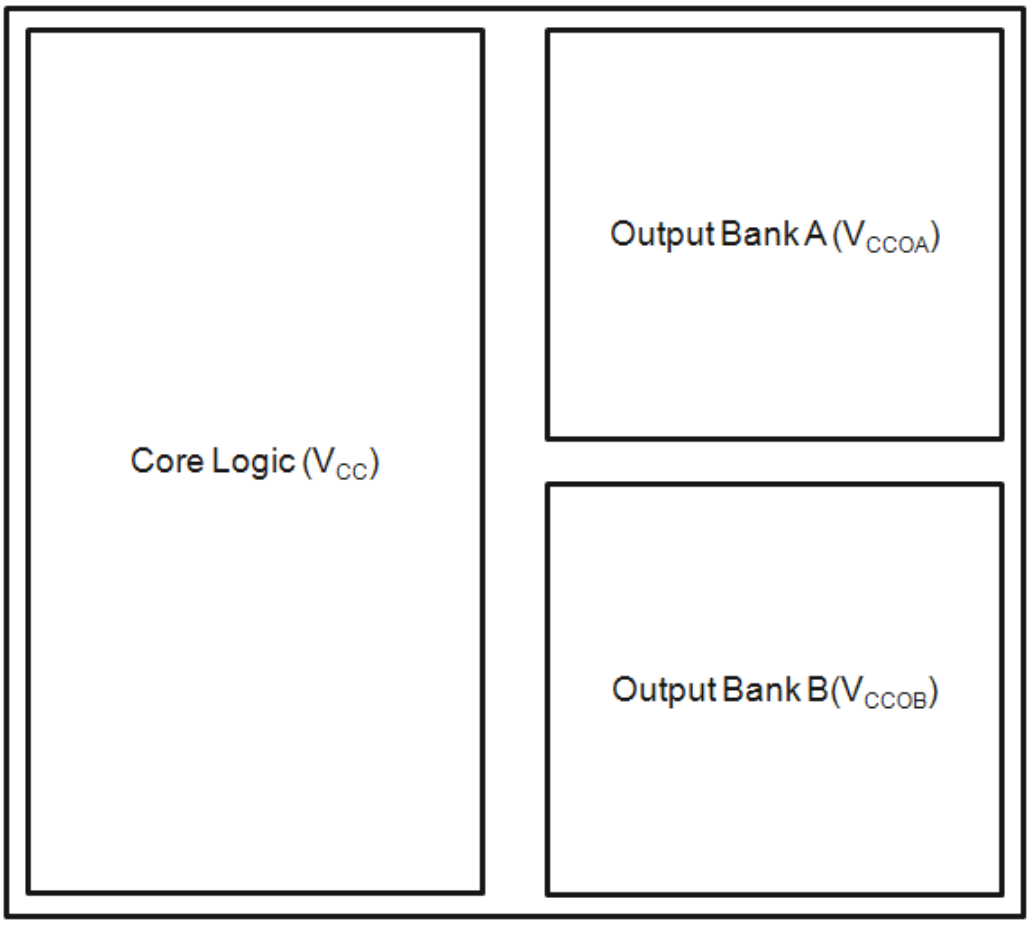



**Figure 19. 8P79208 Power Domains**

## 6.2 Power Consumption Calculation

Determining total power consumption involves several steps:

1. Determine the power consumption using maximum current values for core voltage from Table 6, Table 7, Table 8 and for the appropriate case of how many banks or outputs are enabled.
2. Determine the nominal power consumption of each enabled output path.
   a. This consists of a base amount of power that is independent of operating frequency, as shown in Table 18 through Table 27 (depending on the chosen output protocol).
   b. Then there is a variable amount of power that is related to the output frequency. This can be determined by multiplying the output frequency by the FQ_Factor shown in Table 18 through Table 27.
3. All of the above totals are then summed.

## 6.3 Thermal Considerations

Once the total power consumption has been determined, it is necessary to calculate the maximum operating junction temperature for the device under the environmental conditions it will operate in. Thermal conduction paths, air flow rate and ambient air temperature are factors that can affect this. The thermal conduction path refers to whether heat is to be conducted away via a heat-sink, via airflow or via conduction into the PCB through the device pads (including the ePAD). Thermal conduction data is provided for typical scenarios in Table 31. Please contact Renesas for assistance in calculating results under other scenarios.

## 6.4 Current Consumption Data and Equations

**Table 18. 3.3V LVDS Output Calculation Table**

| LVDS | FQ_Factor (mA/MHz) | Base_Current (mA) |
|---|---|---|
| Bank A | 0.063 | 23 |
| Bank B | 0.063 | 23 |

**Table 19. 3.3V LVDS Output Calculation Table**

| LVDS | FQ_Factor (mA/MHz) | Base_Current (mA) |
|---|---|---|
| Bank A | 0.038 | 19 |
| Bank B | 0.038 | 19 |

**Table 20. 2.5V LVDS Output Calculation Table**

| LVDS | FQ_Factor (mA/MHz) | Base_Current (mA) |
|---|---|---|
| Bank A | 0.065 | 17 |
| Bank B | 0.065 | 17 |

**Table 21. 2.5V LVDS Output Calculation Table**

| LVDS | FQ_Factor (mA/MHz) | Base_Current (mA) |
|---|---|---|
| Bank A | 0.037 | 18 |
| Bank B | 0.037 | 18 |

**Table 22. 1.8V LVDS Output Calculation Table**

| LVDS | FQ_Factor (mA/MHz) | Base_Current (mA) |
|---|---|---|
| Bank A | 0.67 | 15 |
| Bank B | 0.67 | 15 |

**Table 23. 1.8V LVDS Output Calculation Table**

| LVDS | FQ_Factor (mA/MHz) | Base_Current (mA) |
|---|---|---|
| Bank A | 0.033 | 17 |
| Bank B | 0.033 | 17 |

**Table 24. 3.3V LVCMOS Output Calculation Table**

| LVCMOS | FQ_Factor (mA/MHz) | Base_Current (mA) |
|---|---|---|
| Bank A | 0.25 | 28 |
| Bank B | 0.25 | 28 |

**Table 25. 3.3V LVCMOS Output Calculation Table**

| LVCMOS | FQ_Factor (mA/MHz) | Base_Current (mA) |
|---|---|---|
| Bank A | 0.14 | 14 |
| Bank B | 0.14 | 14 |

**Table 26. 2.5V LVCMOS Output Calculation Table**

| LVCMOS | FQ_Factor (mA/MHz) | Base_Current (mA) |
|---|---|---|
| Bank A | 0.22 | 20 |
| Bank B | 0.22 | 20 |

**Table 27. 2.5V LVCMOS Output Calculation Table**

| LVCMOS | FQ_Factor (mA/MHz) | Base_Current (mA) |
|---|---|---|
| Bank A | 0.11 | 8 |
| Bank B | 0.11 | 8 |

Applying the values to the following equation will yield output current by frequency:

Qx Current (mA) = FQ_Factor * Frequency (MHz) + Base_Current

where:

Qx Current is the specific output current according to output type and frequency
FQ_Factor is used for calculating current increase due to output frequency
Base_Current is the base current for each output path independent of output frequency

The second step is to multiply the power dissipated by the thermal impedance to determine the maximum power gradient, using the following equation:

$T_J = T_A + (\theta_{JA} * Pdtotal)$

where:

$T_J$ is the junction temperature (°C)
TA is the ambient temperature (°C)
$\theta_{JA}$ is the thermal resistance value from Table 33, Page 30, dependent on ambient airflow (°C/W)
$Pd_{total}$ is the total power dissipation of the under usage conditions, including power dissipated due to loading (W)

Note that for LVPECL outputs the power dissipation through the load is assumed to be 27.95mW. When selecting LVCMOS outputs, power dissipation through the load will vary based on a variety of factors including termination type and trace length. For these examples, power dissipation through loading will be calculated using $C_{PD}$ (found in Table 2) and output frequency:

$Pd_{OUT} = C_{PD} * f_{OUT} * V_{CCO}$

where:

$Pd_{OUT}$ is the power dissipation of the output (W)
$C_{PD}$ is the power dissipation capacitance (pF)
$f_{OUT}$ is the output frequency of the selected output (MHz)
$V_{CCO}$ is the voltage supplied to the appropriate output (V)

## 6.5 Example Calculations

**Table 28. Example 1 – Common Customer Configuration (3.3V Core Voltage)**

| | Configuration | Frequency (MHz) | VCCO |
|---|---|---|---|
| Bank A | LVDS | 125 | 3.3V |
| Bank B | LVDS | | 3.3V |

- Core Supply Current, $I_{CC}$ = 26mA (maximum)

  Bank A Current = 0.063mA/MHz x 125MHz + 23mA = 30.875mA

  Bank B Current = 0.063mA/MHz x 125MHz + 23mA = 30.875mA

- Total Output Current = 30.875mA + 30.875mA = 61.75mA

  Total Device Current = 26mA + 61.75mA = 87.75mA

  Total Device Power = 3.465V * 87.75mA = 304.1mW or 0.3041W

With an ambient temperature of 85°C and no airflow, the junction temperature is:

$T_J$ = 85°C + 35.23°C/W * 0.3041W = 95.72°C.

## 6.6 Case Temperature Considerations

This device supports applications in a natural convection environment which does not have any thermal conductivity through ambient air. The printed circuit board (PCB) is typically in a sealed enclosure without any natural or forced air flow and is kept at or below a specific temperature. The device package design incorporates an exposed pad (ePad) with enhanced thermal parameters which is soldered to the PCB where most of the heat escapes from the bottom exposed pad. For this type of application, it is recommended to use the junction-to-board thermal characterization parameter $\Psi_{JB}$ (Psi-JB) to calculate the junction temperature ($T_J$) and ensure it does not exceed the maximum allowed junction temperature in the Absolute Maximum Rating table.

The junction-to-board thermal characterization parameter, $\Psi_{JB}$, is calculated using the following equation:

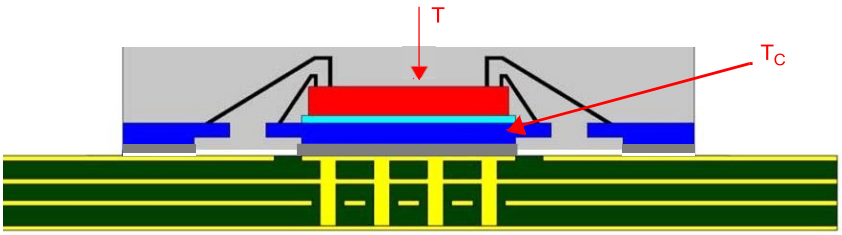
$T_J = T_{CB} + \Psi_{JB} \times P_d$, Where

$T_J$ = Junction temperature at steady state condition in (°C).

$T_{CB}$ = Case temperature (Bottom) at steady state condition in (°C).

$\Psi_{JB}$ = Thermal characterization parameter to report the difference between junction temperature and the temperature of the board measured at the top surface of the board.

$P_d$ = power dissipation (W) in desired operating configuration.




The ePad provides a low thermal resistance path for heat transfer to the PCB and represents the key pathway to transfer heat away from the IC to the PCB. It's critical that the connection of the exposed pad to the PCB is properly constructed to maintain the desired IC case temperature ($T_{CB}$). A good connection ensures that temperature at the exposed pad ($T_{CB}$) and the board temperature ($T_B$) are relatively the same. An improper connection can lead to increased junction temperature, increased power consumption and decreased electrical performance. In addition, there could be long-term reliability issues and increased failure rate.

Example Calculation for Junction Temperature ($T_J$): $T_J = T_{CB} + \Psi_{JB} \times P_d$

| | |
|---|---|
| **Package Type** | 32-Lead VFQFN |
| **Body Size** | 5 × 5 × 0.9 mm |
| **ePad Size** | 3.1mm x 3.1mm |
| **Thermal Via** | 4 × 4 matrix |
| **$\Psi_{JB}$** | 0.62 C/W |
| **$T_{CB}$** | 105°C |
| **$P_d$** | 0.71W |

For the variables above, the junction temperature is equal to 105.4°C. Since this is below the maximum junction temperature of 125°C, there are no long term reliability concerns.

# 7. LVPECL Power Considerations

This section provides information on power dissipation and junction temperature for the 8P79208. Equations and example calculations are also provided.

**LVPECL Power Considerations**

- **Power Dissipation**

The total power dissipation for the 8P79208 is the sum of the core power plus the power dissipated due to loading. The following is the power dissipation for $V_{CC}$ = 3.3V+5% = 3.465V, which gives worst case results.

The Maximum current at 85°C is as follows:

$I_{EE\_MAX}$ = 140mA

**Note**: Refer to the “Calculations and Equations” section for details on calculating power dissipated due to loading.

- Power $(core)_{MAX} = I_{EE\_MAX} * V_{CC\_MAX}$ = 3.465V * 140mA = **485.1mW**
- Power $(outputs)_{MAX}$ = **27.95mW/Loaded Output pair**

  If all outputs are loaded, the total power is 8 * 27.95mW = **223.6mW**

Total $Power\_{MAX}$ = 485.1mW + 223.6mW = **708.7mW**

- **Junction Temperature.**

Junction temperature, $T_J$, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, $T_J$, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for $T_J$ is as follows: $T_J = \Theta_{JA} * Pd\_total + T_A$

$T_J$ = Junction Temperature

$\Theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\Theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 35.23°C/W per Table 29 below.

Therefore, $T_J$ for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.709W * 35.23°C/W = 110°C. This is below the limit of 125°C.

This calculation is only an example. $T_J$ will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 29. Thermal Resistance $\Theta_{JA}$ for 32 Lead VQFN, Forced Convection**

| $\Theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Meters per Second | 0 | 1 | 2 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 35.23°C/W | 31.6°C/W | 30.0°C/W |

- **Calculations and Equations.**

The purpose of this section is to calculate the power dissipation for the LVPECL output pair. LVPECL output driver circuit and termination are shown in Figure 26.

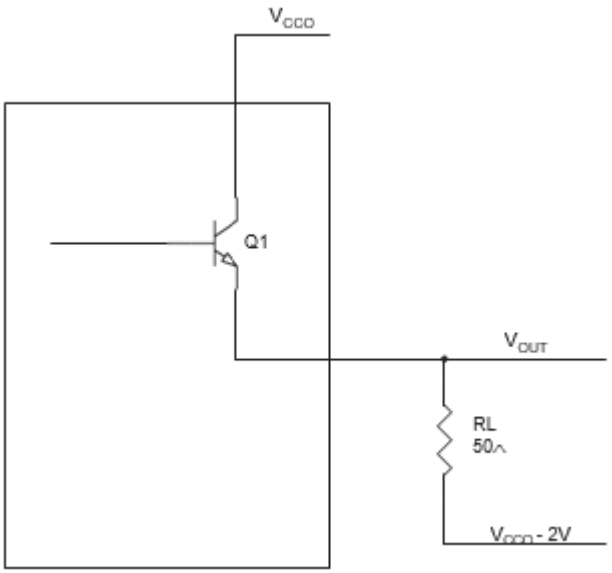



**Figure 20. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO}$ – 2V.

For logic high, $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX}$ – **0.8V**

($V_{CCO\_MAX} – V_{OH\_MAX}$) = **0.8V**

For logic low, $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX}$ – **1.75V**

($V_{CCO\_MAX} – V_{OL\_MAX}$) = **1.75V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

Pd_H = [($V_{OH\_MAX}$ – ($V_{CCO\_MAX}$ – 2V))/$R_L$] * ($V_{CCO\_MAX}$ – $V_{OH\_MAX}$) = [(2V – ($V_{CCO\_MAX} – V_{OH\_MAX}$))/$R_L$] * ($V_{CCO\_MAX} – V_{OH\_MAX}$) = [(2V – 0.8V)/50Ω] * 0.8V = **19.2mW**

Pd_L = [($V_{OH\_MAX}$ – ($V_{CCO\_MAX}$ – 2V))/$R_L$] * ($V_{CCO\_MAX}$ – $V_{OH\_MAX}$) = [(2V – ($V_{CCO\_MAX} – V_{OH\_MAX}$))/$R_L$] * ($V_{CCO\_MAX} – V_{OH\_MAX}$) = [(2V – 1.75V)/50Ω] * 1.75V = **8.75mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **27.95mW**

# 8. LVDS Power Considerations

This section provides information on power dissipation and junction temperature for the 8P79208. Equations and example calculations are also provided.

**LVDS Power Considerations**

- **Power Dissipation**

The total power dissipation for the 8P79208 is the sum of the core power plus the power dissipated due to loading. The following is the power dissipation for $V_{CC}$ = 3.3V +5% = 3.465V, which gives worst case results.

The Maximum current at 85°C is as follows

$I_{EE\_MAX}$ = 174mA

Power (core) Max = $V_{CC\_MAX}$ * $I_{EE\_MAX}$ = 3.465V * 174mA = **602.91mW**

- **Junction Temperature**

Junction temperature, $T_j$, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, $T_j$, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for $T_j$ is as follows: $T_j = \Theta_{JA} * Pd\_total + TA$

$T_j$ = Junction Temperature

$\Theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is shown above in Power Disspation)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\Theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 35.23°C/W per Table 30 below.

Therefore, $T_j$ for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.603W * 35.23°C/W = 106.3°C. This is below the limit of 125°C.

This calculation is only an example. $T_j$ will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 30. Thermal Resistance $\Theta_{JA}$ for 32 Lead VQFN, Forced Convection**

| $\Theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Meters per Second | 0 | 1 | 2 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 35.23°C/W | 31.6°C/W | 30.0°C/W |

# 9. Reliability Information

**Table 31. $\Theta_{JA}$ vs. Air Flow Table for a 32-lead 5 x 5 mm VFQFN**

| $\Theta_{JA}$ vs. Air Flow | | | |
|---|---|---|---|
| Meters per Second | 0 | 1 | 2 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 35.23°C/W | 31.6°C/W | 30.0°C/W |

# 10. Transistor Count

The 8P79208 transistor count is: 10,396

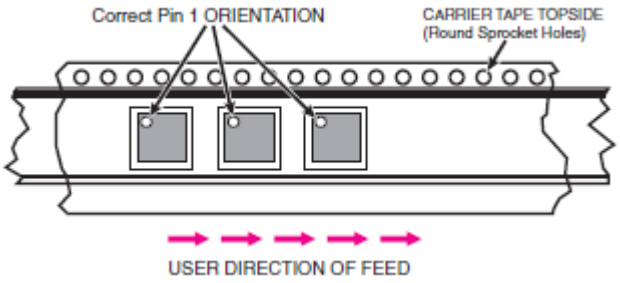
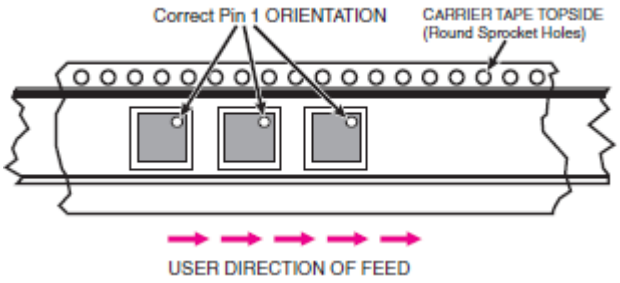
# 11. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

# 12. Ordering Information

| Part Number | Marking | Package Description | Carrier Type | Temperature Range |
|---|---|---|---|---|
| 8P79208NLGI | IDT8P79208NLGI | 32-VFQFPN, 5 × 5 mm | Tray | -40°C to +105°C |
| 8P79208NLGI8 | | | Tape & Reel, Pin 1 Orientation: EIA-481-C | |
| 8P79208NLGI/W | | | Tape & Reel, Pin 1 Orientation: EIA-481-D | |

## 12.1 Pin 1 Orientation in Tape and Reel Packaging

| Part Number Suffix | Pin 1 Orientation | Illustration |
|---|---|---|
| NLGI8 | Quadrant 1 (EIA-481-C) |  |
| NLGI/W | Quadrant 2 (EIA-481-D) |  |

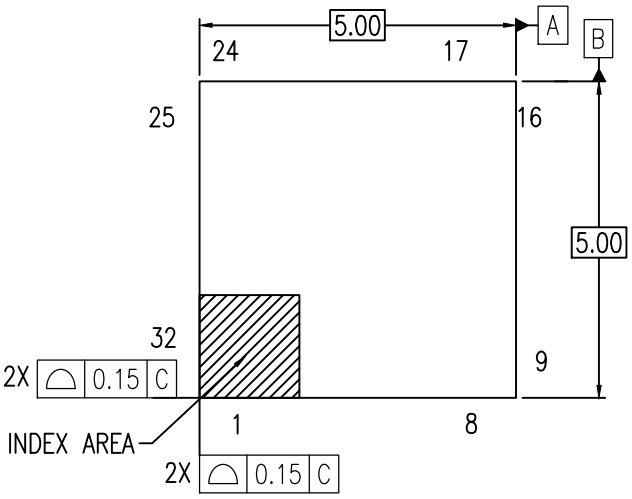
# 13. Revision History

| Revision | Date | Description |
|---|---|---|
| 1.00 | Nov 17, 2021 | Initial release of rebranded/reformatted datasheet. |

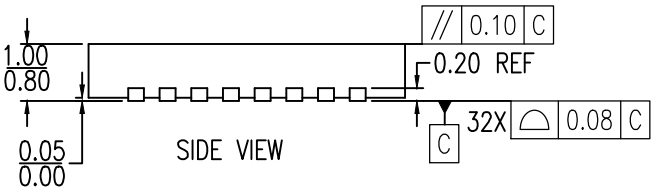
# 32-VFQFPN, Package Outline Drawing

5.0 x 5.0 x 0.90 mm Body, Epad 3.15 x 3.15 mm.

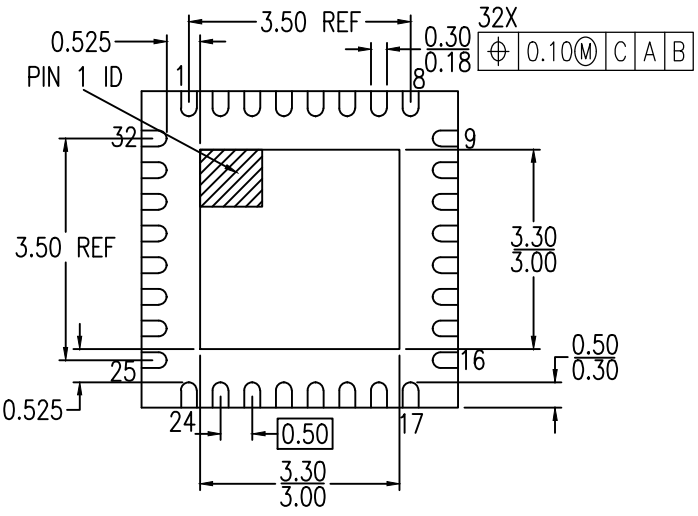
NLG32P1, PSC-4171-01, Rev 03, Page 1



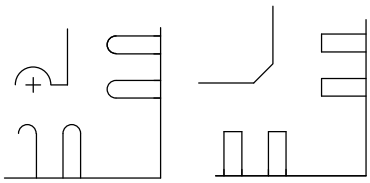

TOP VIEW




SIDE VIEW



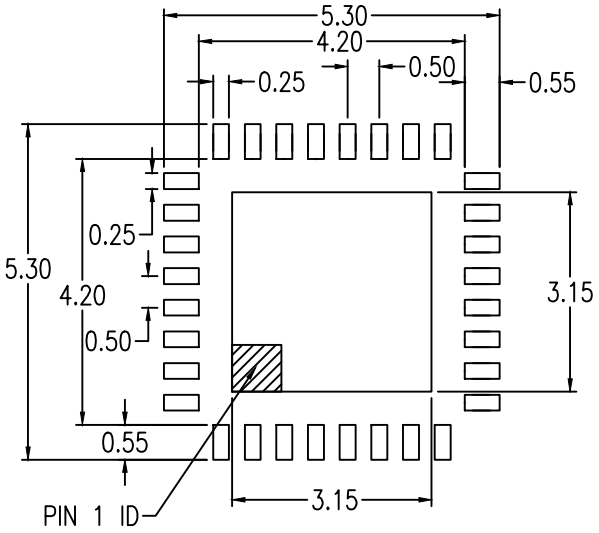

BOTTOM VIEW



PIN #1 ID OPTION

NOTE:

1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. COPLANARITY APPLIE TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 MM.
3. WARPAGE SHALL NOT EXCEED 0.10 MM.
4. PIN LOCATION IS UNDENTIFIED BY EITHER CHAMFER OR NOTCH.




RECOMMENDED LAND PATTERN DIMENSION

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| Package Revision History | | |
|---|---|---|
| Date Created | Rev No. | Description |
| Nov 8, 2021 | Rev 03 | Update from IDT format to Renesas Format |
| April 12, 2018 | Rev 02 | New Format |
| Feb 8, 2016 | Rev 01 | Added "k: Value |

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)


### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/


### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.