AD8316 Evaluation Boards

EVAL-AD8316EB

BOARD DESCRIPTION

Figures 1 and 2 show the schematics of the AD8316 MSOP and LFCSP evaluation boards. Note that uninstalled components are marked as open. The layout and silkscreen of the MSOP evaluation board are shown in Figures 3 and 4. Apart from the slightly smaller device footprint and number of pins, the LFCSP evaluation board is identical to the MSOP board. The boards are powered by a single supply in the 2.7 V to 5.5 V range. The power supply is decoupled by a single 0.1 µF capacitor. Table I details the various configuration options of the evaluation boards.

For operation in controller mode, both jumpers, LK1 and LK2, should be removed. OUT1 and OUT2 can be selected with SW3 in Position A and Position B, respectively. The setpoint voltage is applied to VSET, RFIN is connected to the RF source (PA output or directional coupler), and OUT1 or OUT2 is connected to the gain control pins of each PA. When the AD8316 is used in controller mode, a capacitor and a resistor must be installed in C4, C6 and R10, R11 for loop stability. For GSM/DCS handset power amplifiers, this capacitor should typically range from 150 pF to 300 pF. The series resistor improves the system phase margin at low power levels, which in turn improves the step response in the circuit. Typically, this resistor value should be about 1.5 kΩ.

A quasi-measurement mode (in which the AD8316 delivers an output voltage proportional to the log of the input signal) can be implemented to establish the relationship between VSET and RFIN with the installation of two jumpers, LK1 and LK2. This mimics an AGC loop. To establish the transfer function of the log amp, the RF input should be swept while the voltage on VSET is measured; that is, the SMA connector labeled VSET acts as an output. This is the simplest method for validating operation of the evaluation board. When operated in this mode, a large capacitor (0.01 µF or greater) must be installed in C4 or C6 (set R10, R11 to 0 Ω) to ensure loop stability.

ORDERING GUIDE

Model	Package Description
AD8316-EVAL	MSOP Evaluation Board
AD8316ACP-EVAL	LFCSP Evaluation Board

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the EVAL-AD8316EB features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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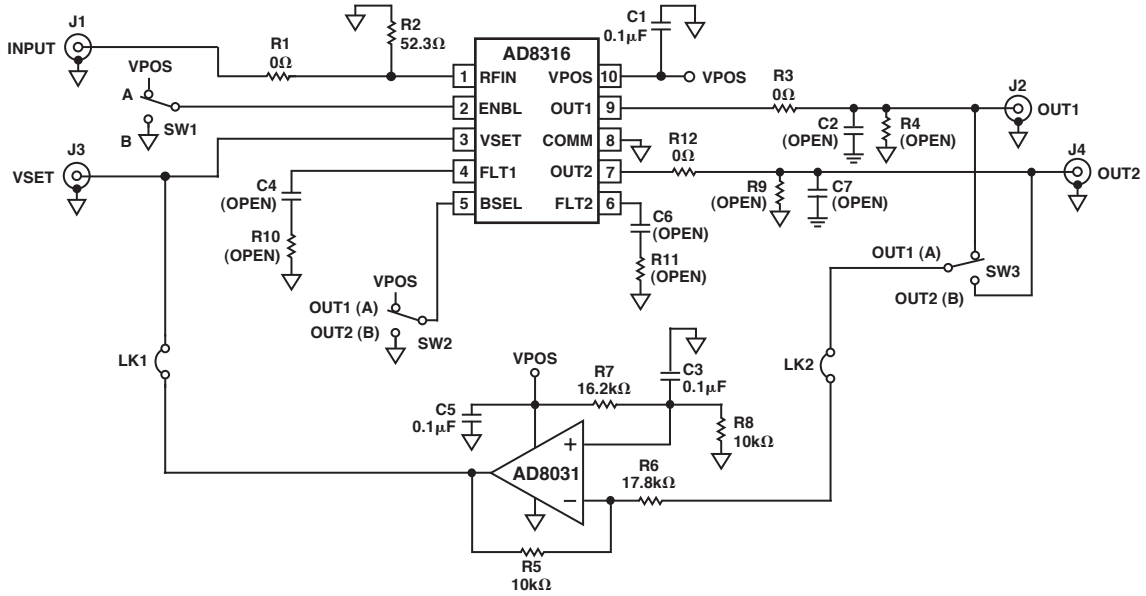

Figure 1. Schematic of Evaluation Board (MSOP)

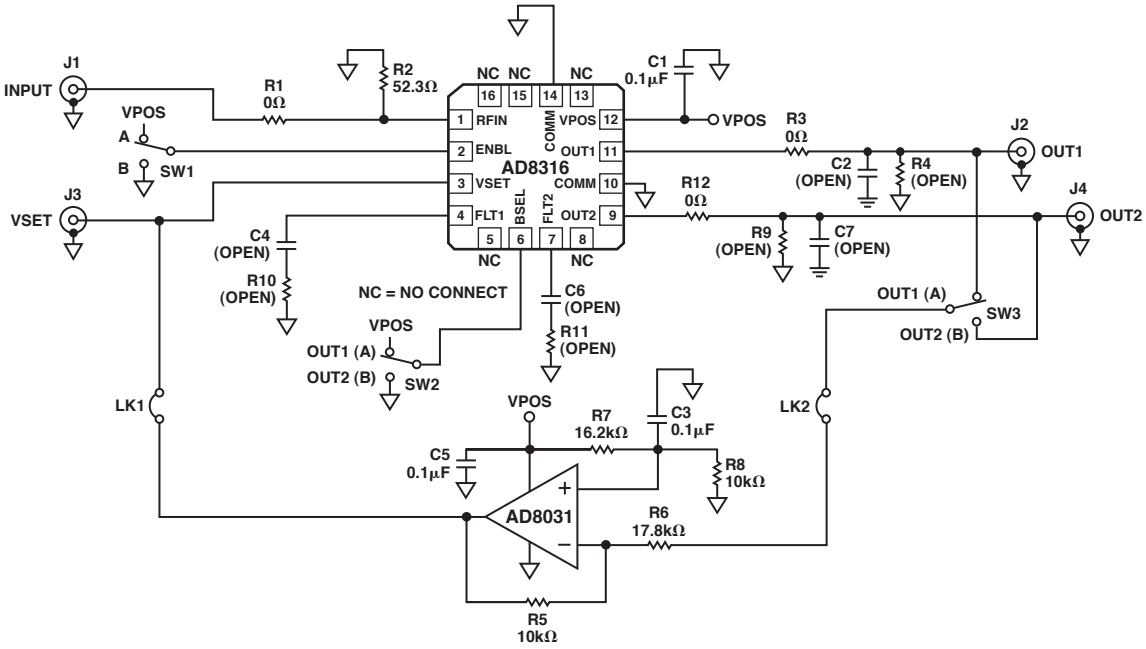

Figure 2. Schematic of Evaluation Board (LFCSP)

Table I. Evaluation Board Configuration Options

Component	Function	Default Condition
TP1, TP2	Supply and Ground Vector Pins.	Not Applicable
SW1	Device Enable. When in Position A, the ENBL pin is connected to VPOS and the AD8316 is in operating mode. In Position B, the ENBL pin is grounded, putting the device into power-down mode.	SW1 = A
SW2	Band Select. When in Position A (OUT1), the BSEL pin is connected to VPOS and the AD8316 OUT1 is in operation mode. In Position B (OUT2) the BSEL pin is grounded, and the AD8316 OUT2 is in operation while OUT1 pin is shut down.	SW2 = OUT1
R1, R2	Input Interface. The 52.3 Ω resistor in position R2 combines with the AD8316's internal input impedance to provide a broadband input impedance of around 50 Ω. A reactive match can be implemented by replacing R2 with an inductor and R1 (0 Ω) with a capacitor. In addition, the RF microstrip line has been provided with a clean mask ground plane to provide additional matching. Note that the AD8316's RF input is internally ac-coupled.	R2 = 52.3 Ω (Size 0603) R1 = 0 Ω (Size 0402)
R3, R4, R12, R9, C2, C7	Output Interface. R4, C2, and R9, C7 can be used to check the response capacitive and resistive loading, respectively. R3, R4 and R12, R9 can be used to reduce the slope of OUT1 and OUT2.	R4 = C2 = Open (Size 0603) R9 = C7 = Open (Size 0603) to R3 = R12 = 0 Ω (Size 0603)
C1, C5	Power Supply Decoupling. The nominal supply decoupling consists of a 0.1 μF capacitor.	C1 = C5 = 0.1 μF (Size 0603)
C4, C6 R10, R11	Filter Capacitors/Resistors. The response time of OUT1, OUT2 can be modified by placing the capacitors between FLTR1, FLT2 and resistors R10, R11 to ground.	C4 = C6 = Open (Size 0603) R10 = R11 = Open (Size 0603)
LK1, LK2	Measurement Mode. A quasi-measurement mode can be implemented by installing LK1 and LK2 (connecting an inverted OUT1 or OUT2 to VSET) to yield the nominal relationship between RFIN and VSET. In this mode ,a large capacitor (0.01 μF or greater) must be installed in C4 and C6 and 0 Ω resistors to ground in R10 and R11. To select OUT1 or OUT2, SW3 must be in the OUT1 position or the OUT2 position, respectively.	LK1, LK2 = Installed
SW3	Measurement Mode Output Select. When in measurement mode, Output 1 or Output 2 can be selected by positioning SW3 to the OUT1 position or the OUT2 position, respectively.	SW3 = OUT1

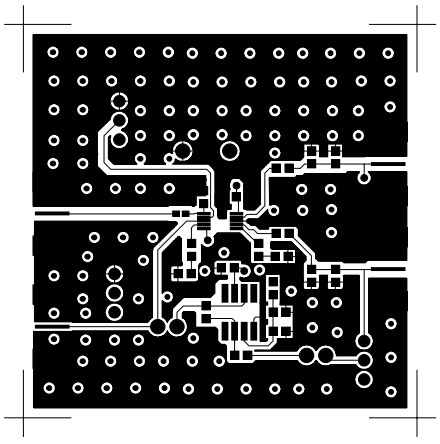

Figure 3. Layout of Component Side (MSOP)

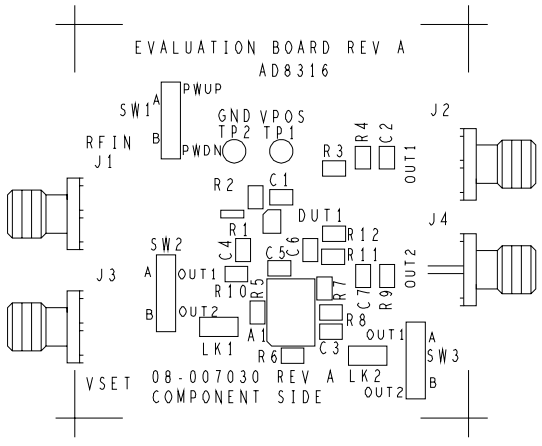

Figure 4. Silkscreen of Component Side (MSOP)