PE42540

Product Specification

UltraCMOS® SP4T RF Switch, 10 Hz–8 GHz

Features

- HaRP™ technology enhanced:
  - Fast settling time
  - Eliminates gate and phase lag
  - No drift in insertion loss and phase
- High linearity: 58 dBm IIP3
- Low insertion loss:
  - 0.8 dB at 3 GHz
  - 1.0 dB at 6 GHz
  - 1.2 dB at 8 GHz
- High isolation:
  - 45 dB at 3 GHz
  - 39 dB at 6 GHz
  - 31 dB at 8 GHz
- Maximum power handling: 30 dBm at 8 GHz
- High ESD tolerance:
  - 2 kV HBM on RFC
  - 1 kV HBM on all other pins
- Packaging: 32-lead 5 × 5 mm LGA

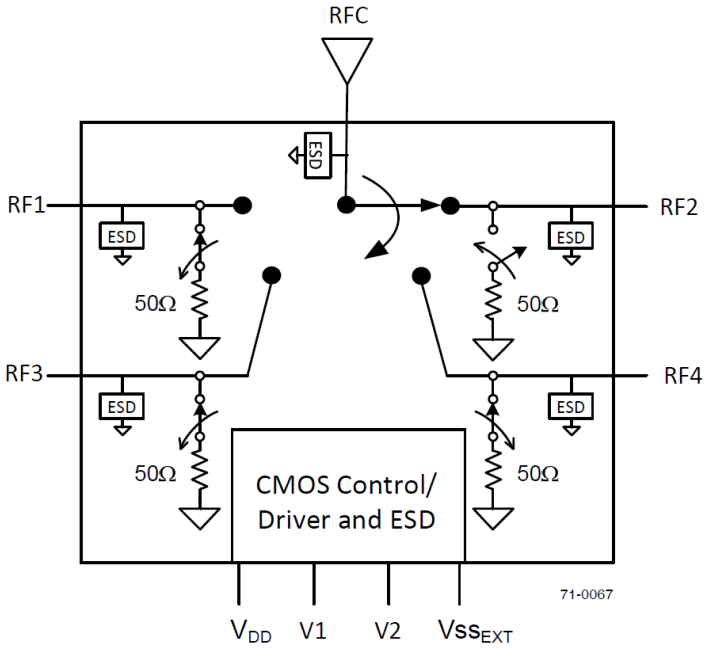

Figure 1. PE42540 functional diagram

Product description

The PE42540 is a HaRP™ technology-enhanced absorptive SP4T RF switch developed on UltraCMOS® process technology. This switch is specifically designed to support the requirements of the test equipment and ATE market. It consists of four symmetric RF ports and has high isolation. An on-chip CMOS decode logic facilitates a two-pin, low-voltage CMOS control interface and an optional external V_{SS} feature. High ESD tolerance and no blocking capacitor requirements make the PE42540 the ultimate in integration and ruggedness.

The PE42540 is manufactured on pSemi's UltraCMOS process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

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Headquarters: 9369 Carroll Park Dr, San Diego, CA 92121
DOC-77985-6.01 — (07/2026)

Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. Absolute maximum ratings

Parameter or condition	Min	Max	Unit
Maximum junction temperature	–	+150	°C
Storage temperature range, T_{ST}	-60	+150	°C
Supply voltage, V_{DD}	-0.3	4	V
Control voltage (V1, V2)	–	4	V
P_{IN} thru path (50Ω, RF power in):(2) - 9 kHz–1 GHz - 1 GHz–8 GHz - (85 °C, V_{SS_EXT} = -3.0V) - (85 °C, V_{SS_EXT} = 0.0V) - (85 °C, V_{SS_EXT} = -3.5V)	–	See Figures 2–4 30 30 28 27.5	dBm
Maximum power, into termination (50Ω): - 9 kHz ≤ 6 MHz(1) - 6 MHz–8 GHz	–	See Figures 2–4 20	dBm
ESD voltage, HBM(2) - RFC - All pins	–	2000 1000	V
ESD voltage CDM, all pins(3)	–	450	V
ESD voltage MM, all pins(4)	–	100	V

Notes:
1. Do not exceed 20 dBm.
2. Human body model (MIL-STD 883 Method 3015)
3. Charged device model (JEDEC JESD22–C101)
4. Machine model (JEDEC JESD22-A115-A)

Recommended operating conditions

Table 2 lists the PE42540 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. Operating conditions

Parameter	Min	Typ	Max	Unit
Supply voltage, V_{DD}	3.0	3.3	3.55	V
Negative power supply voltage, V_{SS_EXT}[1]	-3.6	-3.3	-3.0	V
Negative supply current, I_{SS}	–	-10	-40	µA
Power supply current, I_{DD} V_{DD} = 3.3V, V_{SS_EXT} = 0V, and temperature = +85 °C	–	90	160	µA
Power supply current, I_{DD} V_{DD} = 3.6V, V_{SS_EXT} used	–	–	50	µA
Control voltage high (V1, V2)	1.2	1.5	V_{DD}	V
Control voltage low (V1, V2)	0	0	0.4	V
Control current, I_{CTRL}	–	–	1	µA
P_{IN} thru path (50Ω, RF power in):[2] - 9 kHz–1 GHz - 1 GHz–8 GHz - (85 °C, V_{SS_EXT} = -3.0V) - (85 °C, V_{SS_EXT} = 0.0V) - (85 °C, V_{SS_EXT} = -3.5V)	–	–	See Figures 2–4 30 30 28 27.5	dBm
Maximum power, into termination (50Ω): - 9 kHz ≤ 6 MHz[2][3] - 6 MHz–8 GHz[2][3]	–	–	See Figures 2–4 20	dBm
Maximum power, hot switching (50Ω): - 9 kHz ≤ 6 MHz[2][3] - 6 MHz–8 GHz[2][3]	–	–	See Figures 2–4 20	dBm
Operating temperature range, T_{OP}	-40	–	+85	°C

Notes:
1. Applies only when the external V_{SS} power supply is used. Otherwise, V_{SS_EXT} = 0V.
2. 100% duty cycle (-40 to +85 °C, 1:1 VSWR).
3. Do not exceed 20 dBm.

Electrical specifications

Table 3 lists the PE42540 key electrical specifications at +25 °C, V_{DD} = 3.3V, and V_{SS_EXT} = 0V (Z_S = Z_L = 50Ω), unless otherwise specified.

Table 3. Electrical specifications

Parameter	Condition	Min	Typ	Max	Unit
Operating frequency	–	10 Hz	–	8 GHz	As shown
RFC–RFx insertion loss	10 Hz–9 kHz 3000 MHz 6000 MHz 7500 MHz 8000 MHz	–	0.7 0.8 1.0 1.1 1.2	1.0 1.1 1.3 1.5 1.6	dB
RFx–RFx isolation	10 Hz–9 kHz 3000 MHz 6000 MHz 7500 MHz 8000 MHz	70 40 34 27 25	80 45 39 32 31	–	dB
RFC–RFx isolation	10 Hz–9 kHz 3000 MHz 6000 MHz 7500 MHz 8000 MHz	74 40 28 24 21	84 45 33 29 27	–	dB
Return loss (RFC to active port)	10 Hz–9 kHz 3000 MHz 6000 MHz 7500 MHz 8000 MHz	–	24 23 18 14 13	–	dB
Return loss (terminated port)	10 Hz–9 kHz 3000 MHz 6000 MHz 7500 MHz 8000 MHz	–	35 18 13 11 10	–	dB
Settling time	50% CTRL to 0.05 dB final value (-40 to +85 °C) *rising* edge 50% CTRL to 0.05 dB final value (-40 to +85 °C) *falling* edge	–	14 15	18 45	µs
Switching time, T_{SW}(1)	50% CTRL to 90% or 10% RF	–	5	8	µs
P1dB input 1-dB compression point, RFx–RFC(2)	All bands at 1:1 VSWR and 100% duty cycle	31	33	–	dBm
Input IP3	8000 MHz	–	58	–	dBm
Input IP2	8000 MHz	–	100	–	dBm

Notes:
1. The PE42540 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (pin 31 = GND). The rate at which the PE42540 can switch is only limited to the switching time above if an external negative supply is provided (pin 31 = V_{SS_EXT}).
2. Table 2 shows the maximum operating P_{IN} (50Ω). When operating the part at low frequency, see Figures 2–4.

Spurious performance

The PE42540 typical spurious performance is -159 dBm/Hz when V_{SS_EXT} = 0V (pin 31 = GND). To improve performance, disable the internal negative voltage generator by setting $V_{SS_EXT} = -V_{DD}$.

Optional external V_{SS} control (V_{SS_EXT})

For proper operation, the V_{SS_EXT} pin must be grounded or tied to the V_{SS} voltage specified in Table 2. When the V_{SS_EXT} pin is grounded, FETs in the switch are biased with an internal voltage generator. For applications that require the lowest possible spurious performance, apply V_{SS_EXT} externally to bypass the internal negative voltage generator.

Thermal data

The junction top-of-package, Psi-JT (Ψ_{JT}), is a thermal metric to estimate the junction temperature of the device in an application PCB, per JEDEC JESD51-2:

$$\Psi_{JT} = (T_J - T_T)/P$$

where:

- Ψ_{JT} = Junction-to-top of package characterization parameter in °C/W
- T_J = Die junction temperature in °C
- T_T = Package temperature (top surface, in the center) in °C
- P = Power dissipated by the device in Watts

Table 4. Thermal data

Parameter	Typ	Unit
Junction top-of-package, Ψ_{JT}	79	°C/W
Junction-to-ambient thermal resistance, Θ_{JA}	128	°C/W

Control logic

Table 5. Truth table

State	V1	V2
RF1 on	0	0
RF2 on	1	0
RF3 on	0	1
RF4 on	1	1

Low-frequency operation

Table 6 lists the minimum and maximum voltage limits when operating the device under various V_{DD} and V_{SS_EXT} voltage conditions below 9 kHz. To determine the maximum operating power over the frequency range of the device, see Figures 2–4.

Table 6. Instantaneous RF voltage limits for operation below 9 kHz

V_{DD}	V_{SS_EXT}	Minimum peak voltage at RF port	Maximum peak voltage at RF port
≥ 3.0	0.0	-0.2	1.2
3.0	-3.0	-0.6	1.6
3.3	-3.3	-0.3	1.3
3.5	-3.5	-0.1	1.1
3.6	-3.6	0.0	1.0

Maximum operating power vs. frequency

Figures 2–4 show how the power limit of the device increases with frequency. As the frequency increases, the contours and maximum power limit increase as shown.

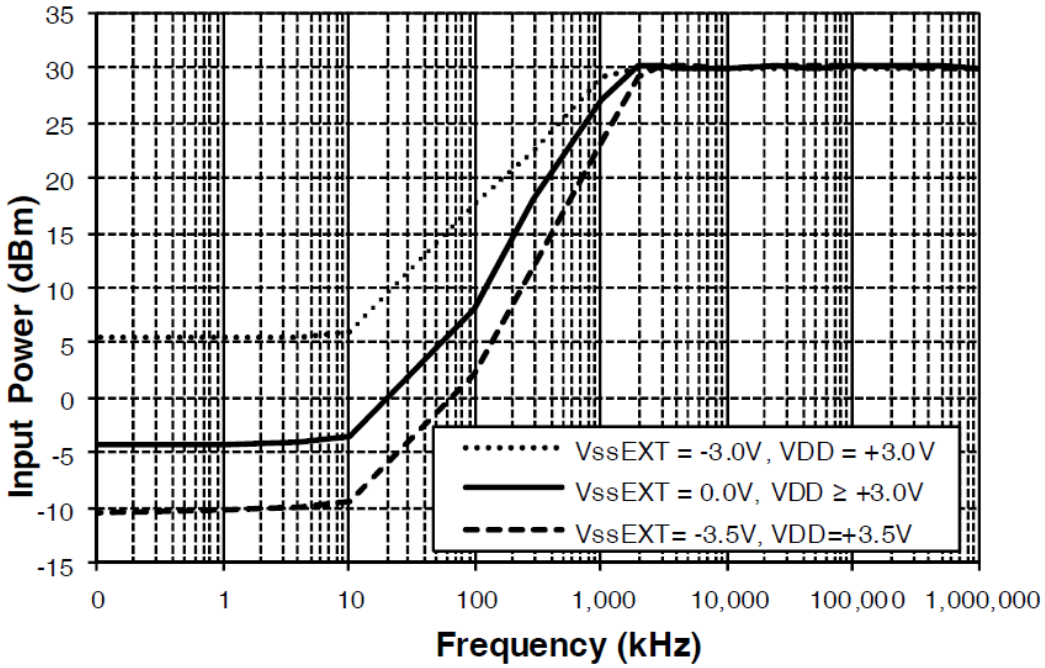


Figure 2. Maximum operating power vs. frequency, T_A = +25 °C

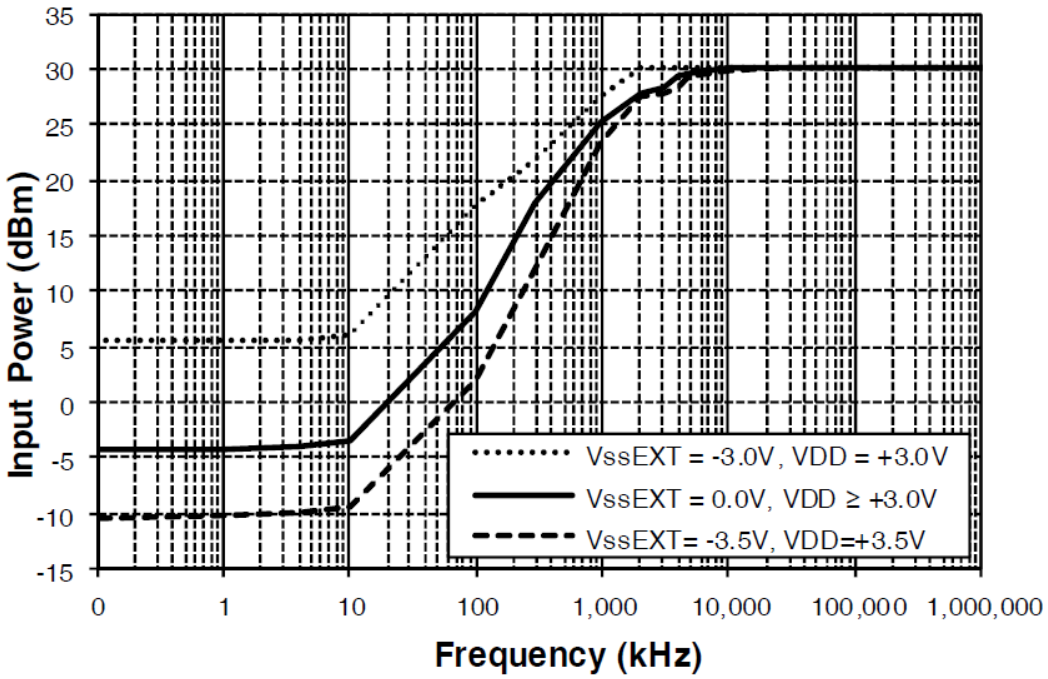


Figure 3. Maximum operating power vs. frequency, T_A = +50 °C

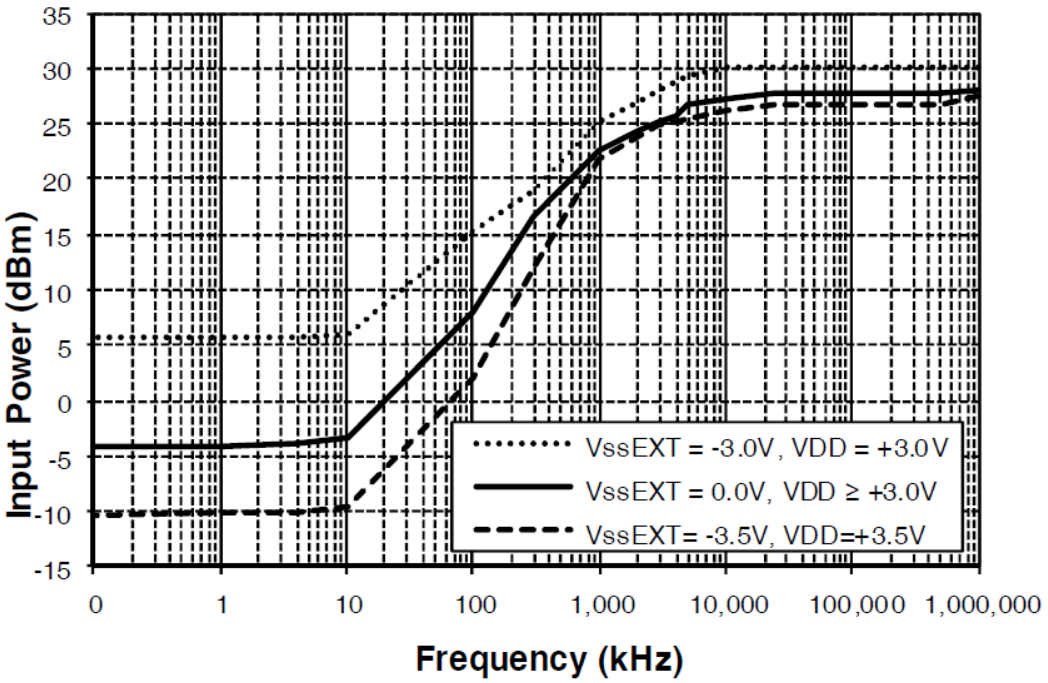


Figure 4. Maximum operating power vs. frequency, T_A = +85 °C

Typical performance data

Figure 5–Figure 18 show the typical performance data at +25 °C, V_{DD} = 3.3V, and V_{SS_EXT} = 0V, unless otherwise specified.

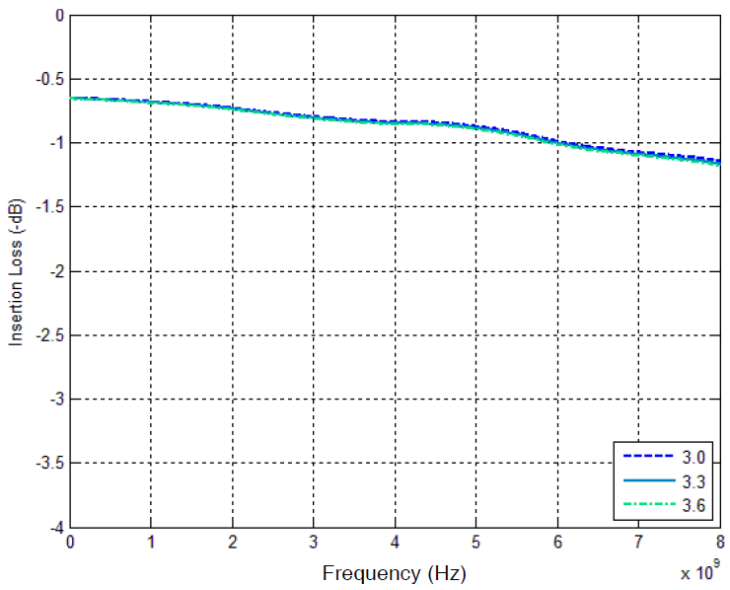


Figure 5. Insertion loss vs. V_{DD}

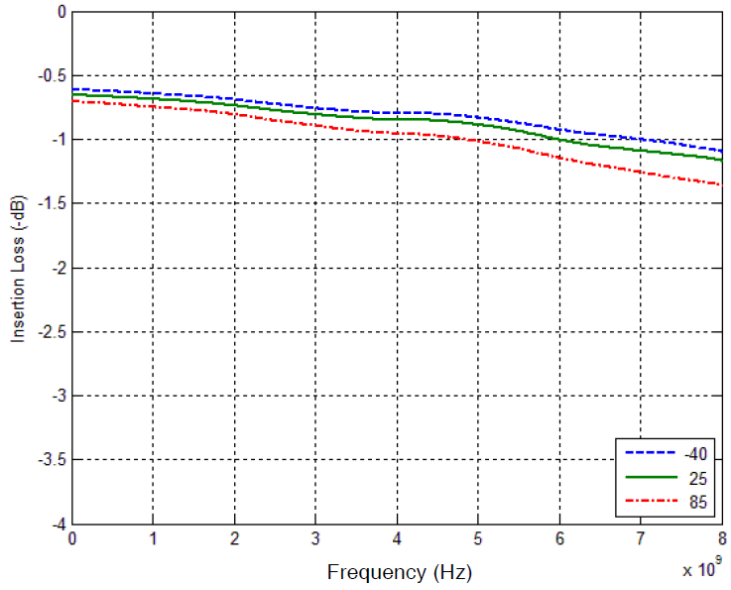


Figure 6. Insertion loss vs. temperature

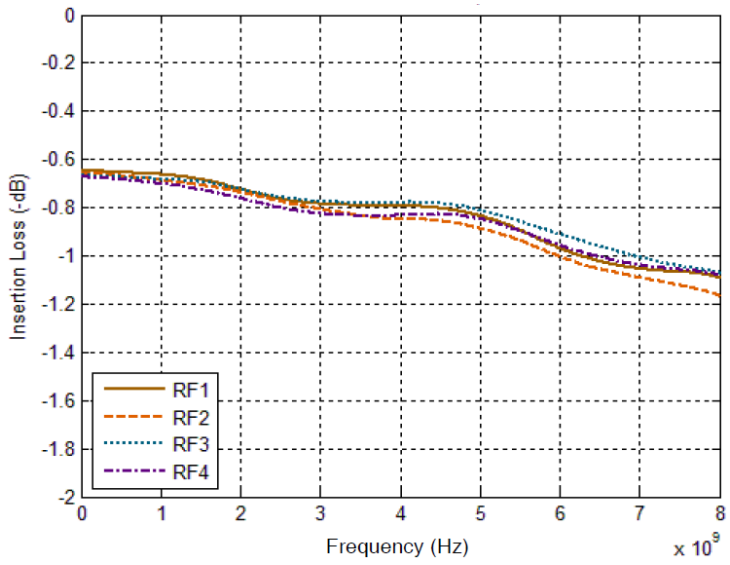


Figure 7. Insertion loss

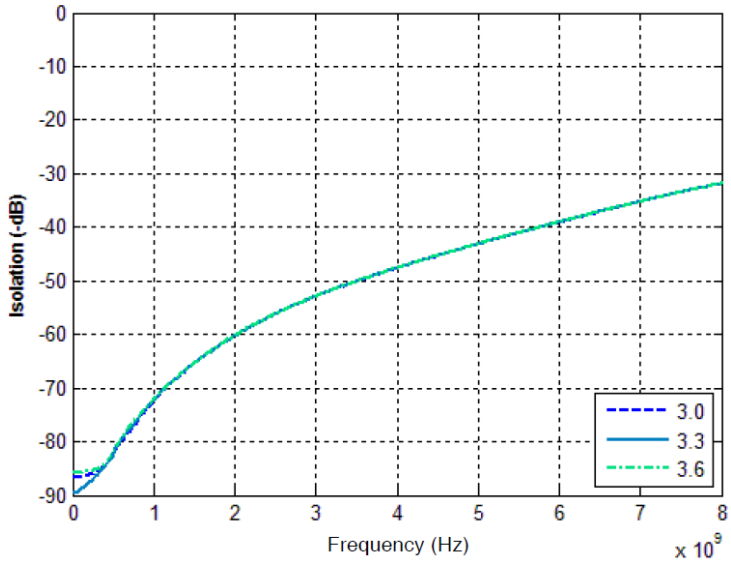


Figure 8. Isolation: RFx–RFx vs. V_{DD}

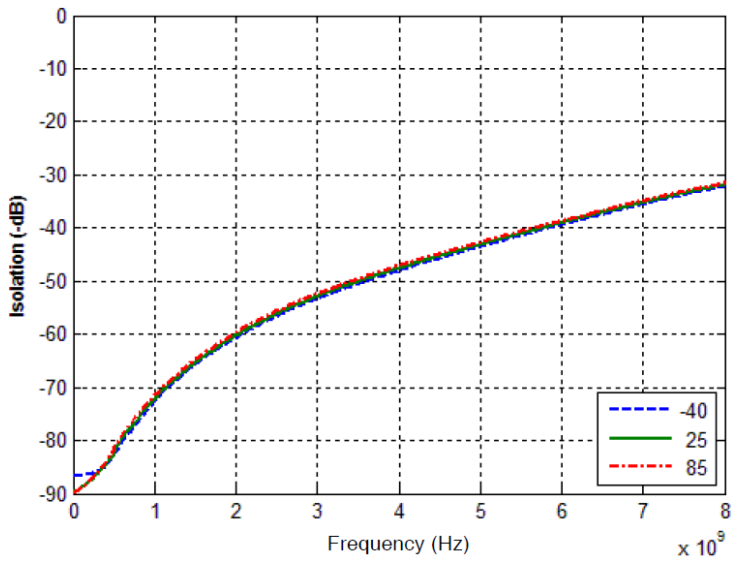


Figure 9. Isolation: RFx–RFx vs. temperature

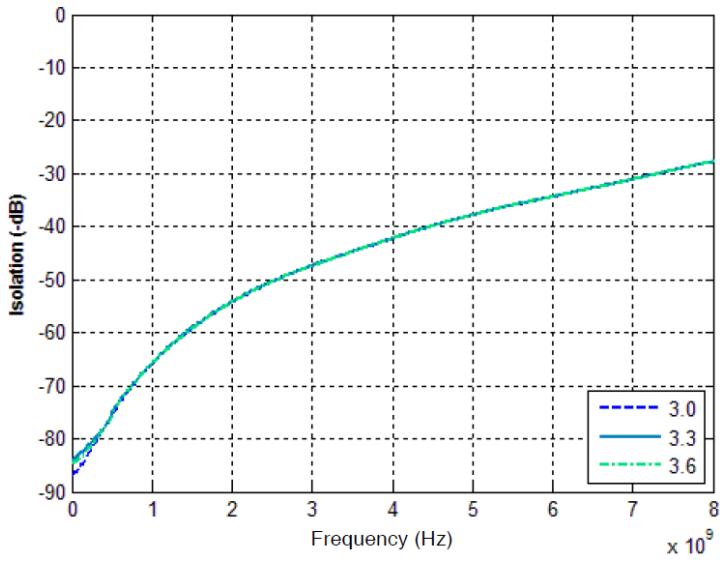


Figure 10. Isolation: RFx–RFC vs. V_{DD}

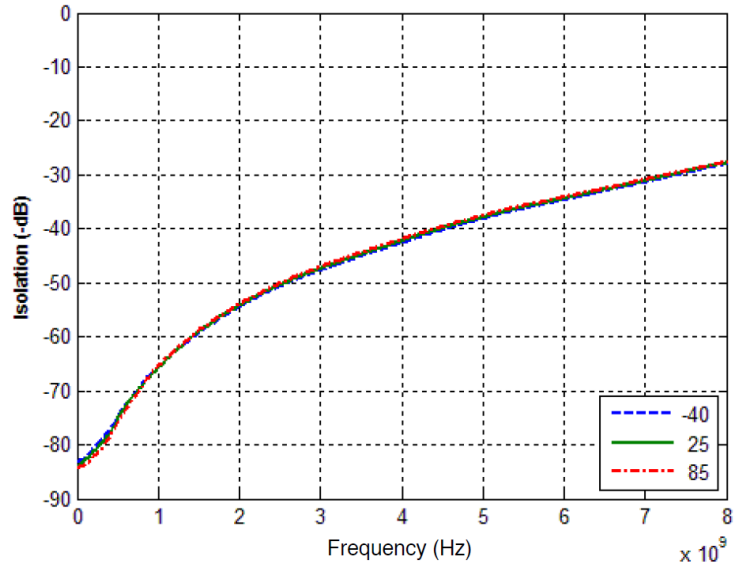


Figure 11. Isolation: RFx–RFC vs. temperature

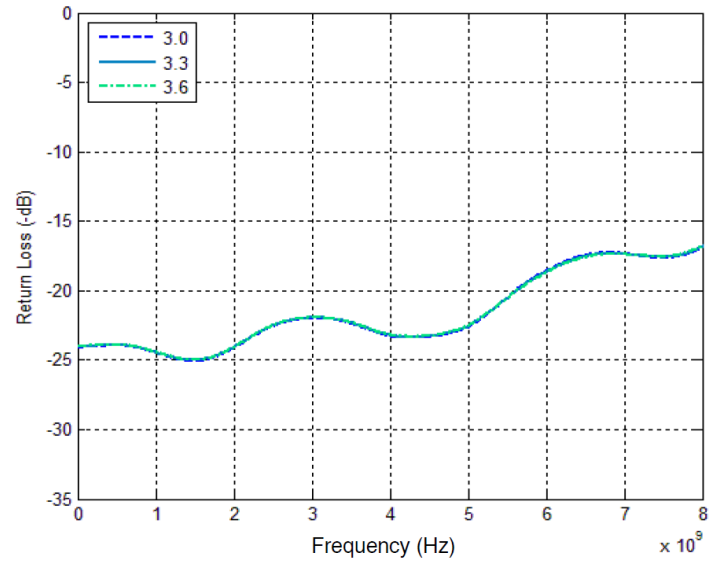


Figure 12. Active port return loss vs. V_{DD}

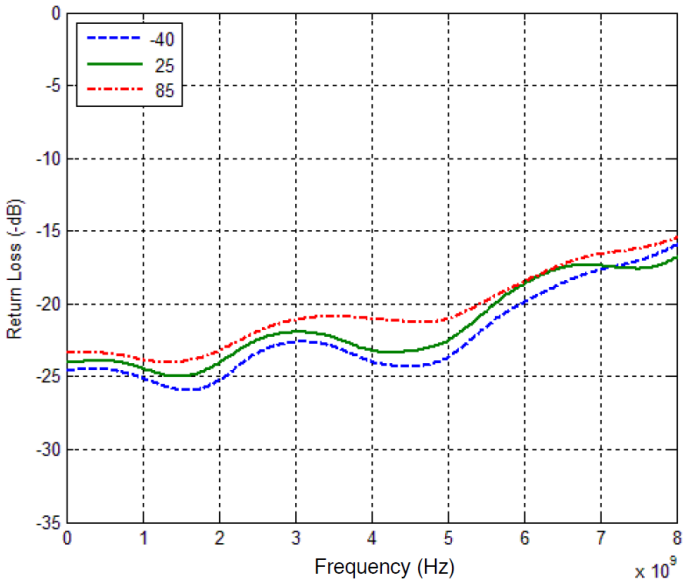


Figure 13. Active port return loss vs. temperature

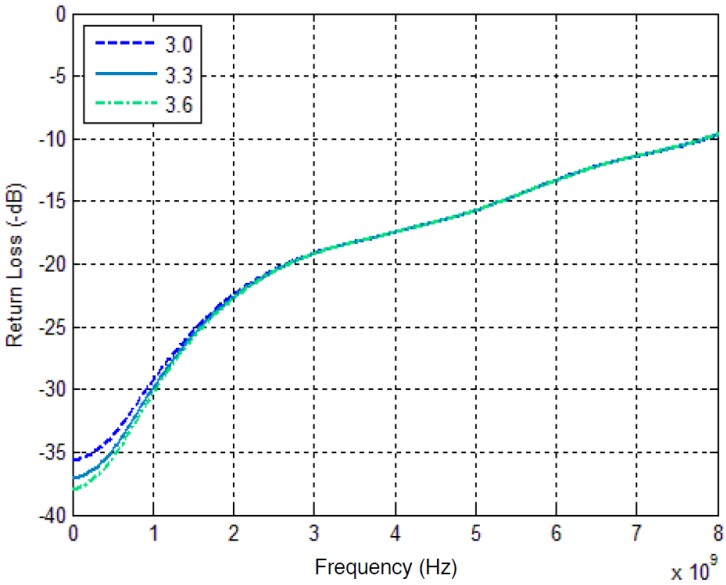


Figure 14. Terminated port return loss vs. V_{DD}

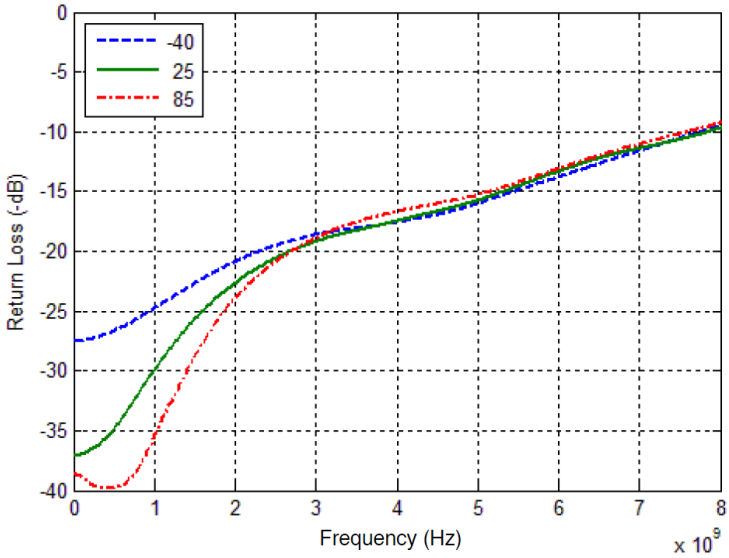


Figure 15. Terminated port return loss vs. temperature

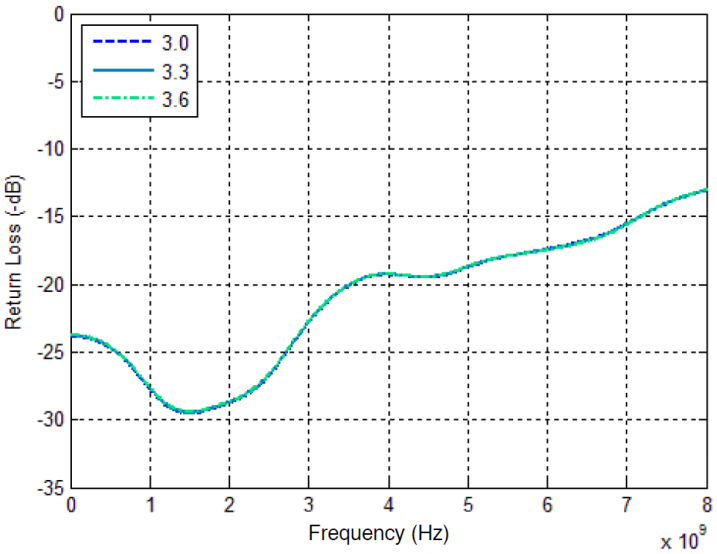


Figure 16. RFC port return loss vs. V_{DD}

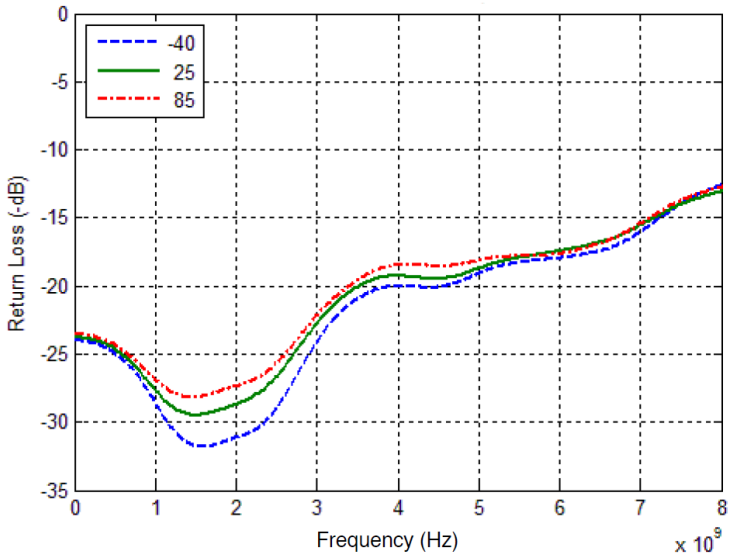


Figure 17. RFC port return loss vs. temperature

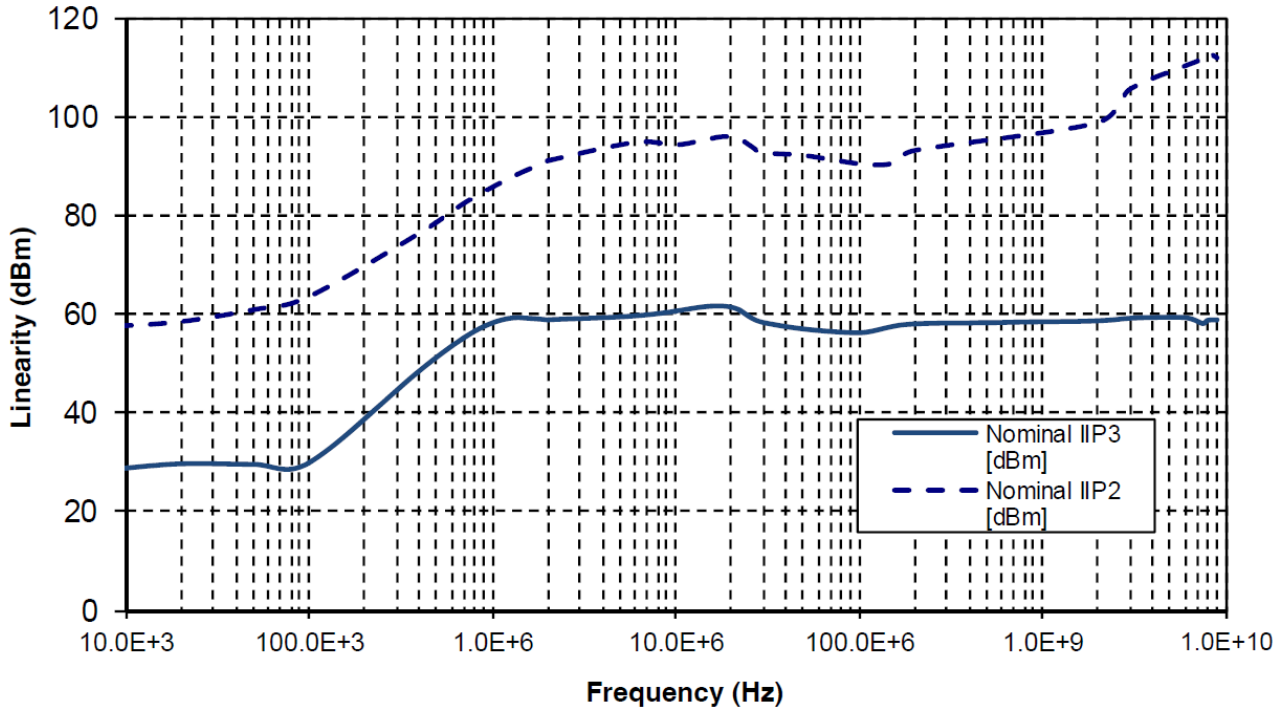


Figure 18. Linearity performance

Evaluation kit

pSemi designed the SP4T switch evaluation board (EVB) to ease your evaluation of the PE42540. The RF common port connects through a 50Ω transmission line via the top SMA connector, J1. The RF1, RF2, RF3, and RF4 ports connect through 50Ω transmission lines via SMA connectors J2, J4, J3, and J5, respectively. A through 50Ω transmission is available via SMA connectors J6 and J7. Use this transmission line to estimate the loss of the PCB over the environmental conditions being evaluated.

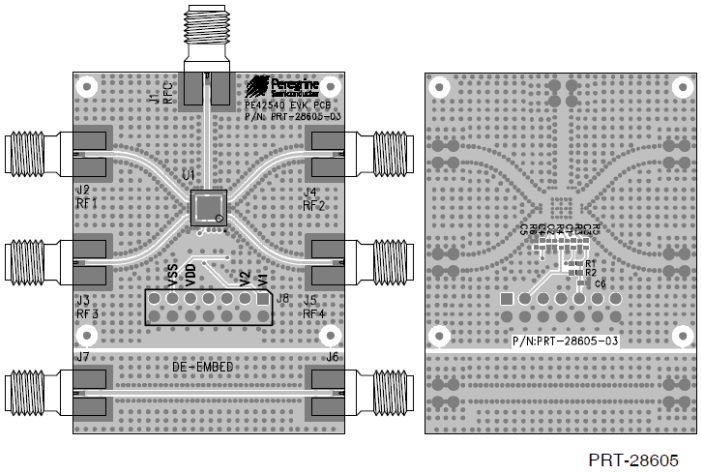


Figure 19. Evaluation board layout

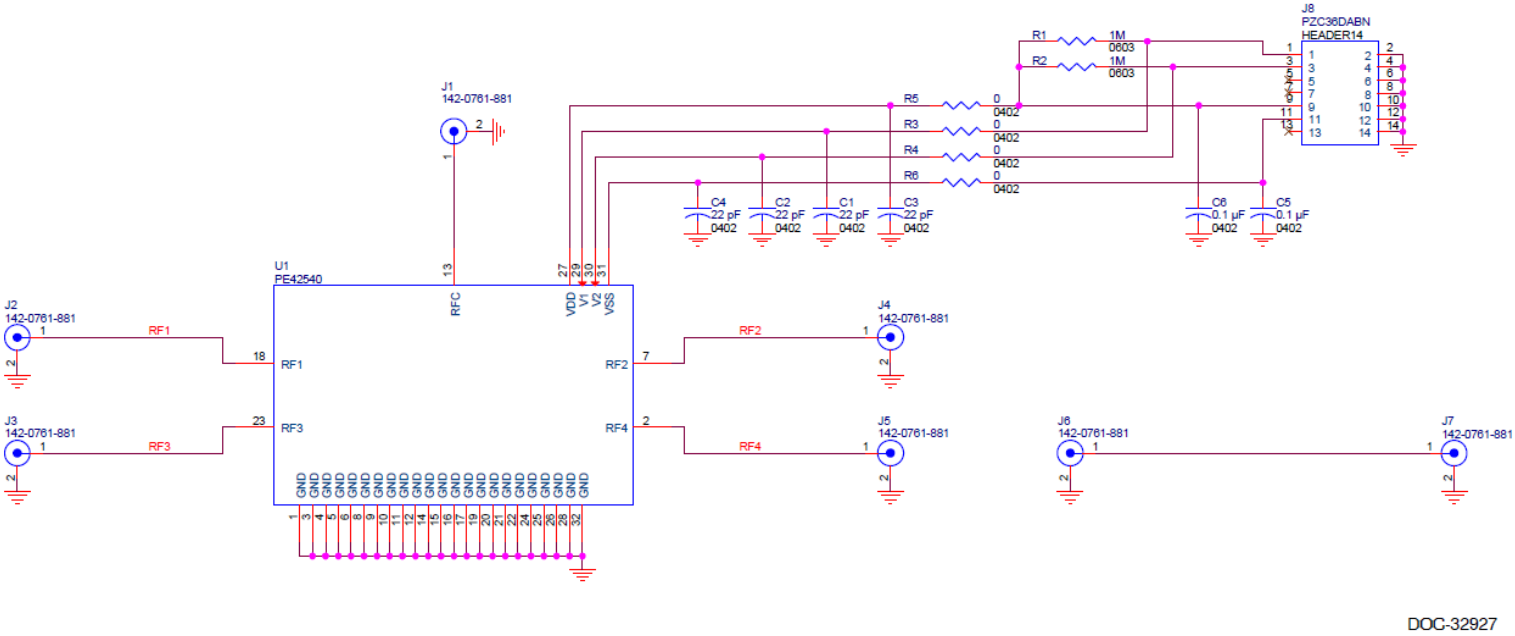


Figure 20. Evaluation board schematic

Pin configuration

Figure 21 shows the PE42540 pin configuration for the 32-lead 5 × 5 mm LGA package, and Table 7 lists the description for each pin.

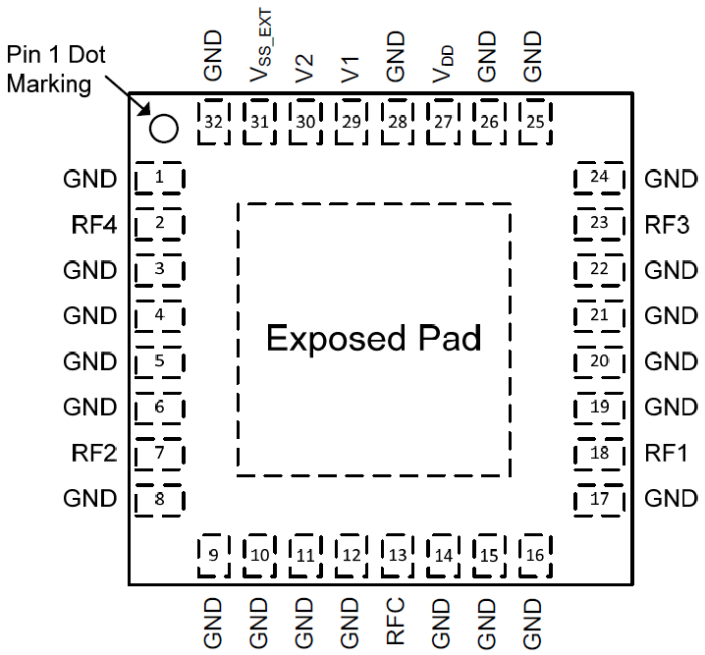


Figure 21. Pin configuration, top view

Table 7. Pin descriptions

Pin no.	Pin name	Description
1, 3–6, 8, 9–12, 14–17, 19–22, 24–26, 28, 32	GND	Ground
2	RF4(1)	RF port 4
7	RF2(1)	RF port 2
13	RFC(1)	RF common
18	RF1(1)	RF port 1
23	RF3(1)	RF port 3
27	V_{DD}	Supply voltage
29	V1	Switch control input, CMOS logic level
30	V2	Switch control input, CMOS logic level
31	V_{SS_EXT}(2)	External V_{SS} negative voltage control
Pad	GND	Exposed pad. Ground for proper operation.

Notes:
1. RF pins 2, 7, 13, 18, and 23 must be DC blocked with an external series capacitor or held at 0 VDC.
2. To bypass and disable the internal negative voltage generator, connect V_{SS_EXT} (pin 31) to = -V_{DD}. To enable the internal negative voltage generator, connect V_{SS_EXT} (pin 31) to GND.

Packaging information

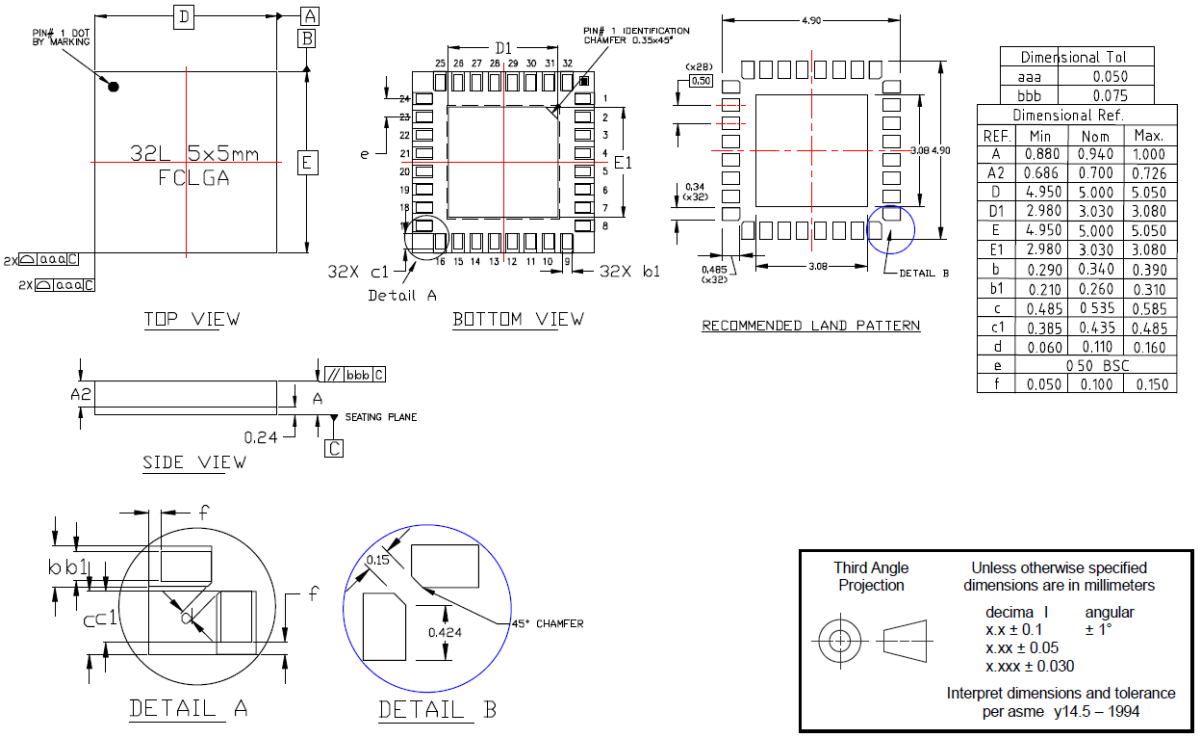
This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE42540 moisture sensitivity level rating for the 32-lead 5 × 5 mm LGA package is MSL3.

Package drawing

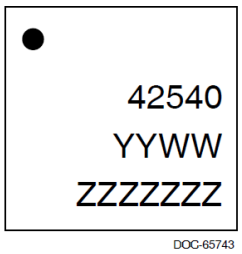


Dimensional Tol	
aaa	0.050
bbb	0.075

Dimensional Ref.			
REF.	Min	Nom	Max.
A	0.880	0.940	1.000
A2	0.686	0.700	0.726
D	4.950	5.000	5.050
D1	2.980	3.030	3.080
E	4.950	5.000	5.050
E1	2.980	3.030	3.080
b	0.290	0.340	0.390
b1	0.210	0.260	0.310
c	0.485	0.535	0.585
c1	0.385	0.435	0.485
d	0.060	0.110	0.160
e	0.50 BSC		
f	0.050	0.100	0.150

Figure 22. Package mechanical drawing for the 32-lead 5 × 5 mm LGA package

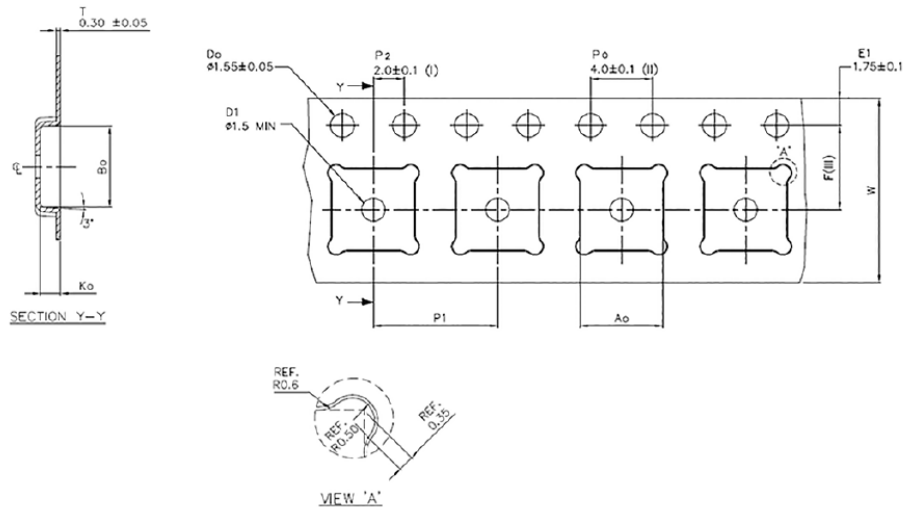
Top-marking specification



YYWW = Date Code

Figure 23. Package marking specification

Tape and reel specification

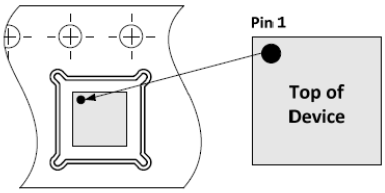


Direction of Feed

Notes: (I) Measured from centerline of sprocket hole to centerline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20.
(III) Measured from centerline of sprocket hole to centerline of pocket.

ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED.

Ao = 5.30 ± 0.1 mm
Bo = 5.30 ± 0.1 mm
Ko = 1.30 ± 0.1 mm
F = 5.50 ± 0.1 mm
P_1 = 8.00 ± 0.1 mm
W = 12.00 ± 0.3 mm



Device Orientation in Tape

Figure 24. Tape and reel specification for the 32-lead 5 × 5 mm LGA package

Ordering information

Order code	Description	Packaging	Shipping method
PE42540G-Z	PE42540 SP4T RF switch	Green 32-lead 5 × 5 mm LGA	3000 units/T&R
EK42540-01	PE42540 evaluation kit	Evaluation kit	1/box

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