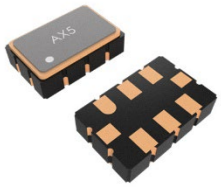
AX5

CLEARCLOCK™ OSCILLATOR FAMILY | LOW JITTER | 5.0X3.2MM XO

Description

Based on our PLL technology, the AX5 series is a programmable XO with LVPECL, LVDS, HCSL, and CML output logic options. Programmed at the factory prior to shipment, this series is perfect for quick turnaround solutions with a wide frequency range of up to 2100MHz. The AX5 series comes in a 5.0 x 3.2mm package with fixed VDD options from 1.8V, 2.5V and 3.3V.



Features

- Ultra-Low Jitter: 125 fs typ RMS (200fs MAX, F>250MHz);
- Available with any frequency from 50MHz to 2100MHz
- Lowest in-class power consumption (60mA typ LVDS)
- ±20ppm stability (-40 to +85ºC)
- 3.3V, 2.5V, 1.8V Vdd supply
- LVPECL, LVDS, HCSL, & CML differential output options
- Industry standard 5.0 x 3.2mm footprint

Typical Applications

- Networking & communications
- 10G/40G/100G optical Ethernet
- RF systems, base stations (BTS)
- Datacenter
- PCI Express
- Test & measurement

Electrical Specifications

Parameters		Min.	Typ.	Max.	Units	Notes
Frequency Range	LVPECL	50		2100	MHz	Option “P”
	LVDS	100		2100		Option “D”
	HCSL	50		700		Option “H”
	CML	100		2100		Option “M”
Supply Voltage (Vdd) [Note 1]		2.97	3.3	3.63	V	Option “A”
		2.25	2.5	2.75		Option “B”
		1.71	1.8	1.89		Option “C”
Supply Current (Idd)	LVPECL		100	111	mA	Max @ 2100MHz; 3.3V
	LVDS		60	65		Max @ 2100MHz; 3.3V
	HCSL		73	78		Max @ 700MHz; 3.3V
	CML		63	68		Max @ 2100MHz; 3.3V
Operating Temperature Range		-20		+70	°C	Option “D”
		-40		+85		Option “F”
Storage Temperature		-55		+150	°C	
Frequency Accuracy (Initial Set-Tolerance) [Note 2] at time of shipment (Pre-Reflow) @ +25°C		-5.00	< ±3.00	+5.00	ppm	Relative to carrier
Frequency Stability over Operating Temperature Range		-15		+15	ppm	Over -20°C to +70°C
		-20		+20		Over -40°C to +85°C
Aging over 20 Year Product Life [Note 3, 4]		-15		+15	ppm	
All-Inclusive Frequency Accuracy (Total Stability) over 20 Year Product Life [Note 3]		-40		+40	ppm	Over -20°C to +70°C
		-45		+45		Over -40°C to +85°C

Electrical Specifications *continued*

Parameters			Min.	Typ.	Max.	Units	Notes
Rise (Tr) / Fall (Tf) Time (20% to 80% Vpeak to peak)					400	ps	
Duty Cycle			45		55	%	@ 50% Vdd
Powerup Time [Note 3]				< 5.0	10	ms	
Output High Voltage (VOH) Output Low Voltage (VOL)	LVPECL	VOH	Vdd-1.165		Vdd-0.8	V	50Ω to Vdd–2.0V or Thevenin equivalent
		VOL	Vdd-2.0		Vdd-1.55		
	LVDS	VOH		1.4	1.6		100Ω between OUT-P and OUT-N
		VOL	0.9	1.1			
	HCSL	VOH	0.66		1.15		50Ω to GND
		VOL	0.0		0.15		
	CML	VOH	Vdd-0.085		Vdd		50Ω to Vdd
		VOL	Vdd-0.6		Vdd-0.32		
Output Enable & Disable Control			0.8*(Vdd)			V	Output Enable; or No Connect
					0.2*(Vdd)		Output Disable; High Impedance
Output Enable Time					2.5	ms	
Output Disable Time					10	µs	
Output Disable Current Consumption	LVPECL			95	105	mA	Max @ 2100MHz; 3.3V
	LVDS			54	59		Max @ 2100MHz; 3.3V
	HCSL			72	76		Max @ 700MHz; 3.3V
	CML			57	62		Max @ 2100MHz; 3.3V

Note 1: Supply Voltage (Vdd) = 1.8V option not available with LVPECL output
Note 2: Excludes carrier frequencies 122.88MHz, 491.52MHz, 368.4MHz, 614.4MHz, 737.28MHz, 860.16MHz, 983.04MHz, & 1105.92MHz. The Frequency Accuracy (Initial Set-Tolerance) at time of shipment (Pre-Reflow) for the above carrier frequencies = ±10ppm MAX.
Note 3: Relative to initial measured frequency @ +25°C
Note 4: Includes temperature stability, initial frequency accuracy, load pulling, power supply variation, and 20 year aging frequency.

RMS Phase Jitter (12kHz -20MHz BW) | Vdd= 3.3V/2.5V/1.8V [Note 5, 6, 7]

Carrier F0 (MHz)	Min.	Typ.	Max.	Units	Notes
251 to 2100		125	200	fsec	All Differential Outputs: LVPECL, LVDS, HCSL & CML
312.500000		125	145	fsec	LVPECL Output
322.265625		125	145	fsec	LVPECL Output
491.250000		115	135	fsec	LVPECL Output
622.080000		125	145	fsec	LVPECL Output
644.531250		115	135	fsec	LVPECL Output
1000.000000		115	135	fsec	LVPECL Output
1024.000000		125	145	fsec	LVPECL Output
1500.000000		110	130	fsec	LVPECL Output
2000.000000		130	150	fsec	LVPECL Output
2100.000000		130	150	fsec	LVPECL Output
126 to 250		150	300	fsec	All Differential Outputs: LVPECL, LVDS, HCSL & CML
150.000000		150	170	fsec	LVPECL Output
156.250000		130	160	fsec	LVPECL Output
200.000000		130	150	fsec	LVPECL Output
212.500000		125	145	fsec	LVPECL Output
250.000000		205	225	fsec	LVPECL Output
50 to 125		250	400	fsec	All Differential Outputs: LVPECL, LVDS, HCSL & CML
100.000000		150	170	fsec	LVPECL Output
122.880000		130	160	fsec	LVPECL Output
125.000000		130	150	fsec	LVPECL Output

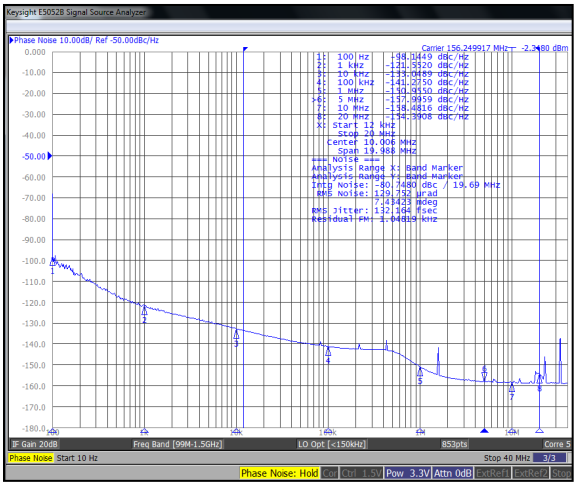
Note 5: Guaranteed by characterization; RMS Phase Jitter specifications are inclusive of any spurs
Note 6: Phase jitter measured with Keysight E5052B Signal Source Analyzer not using a balun or buffer
Note 7: Refer to section 1.1 for phase noise test setup and representative phase noise plots

Phase Noise Test Setup [Note 8]

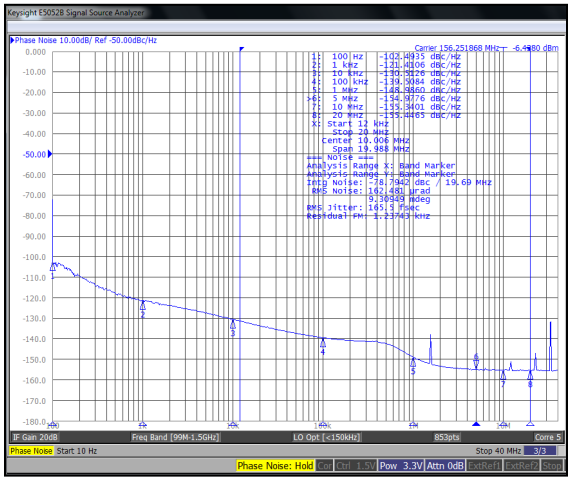
- Keysight E5052B Signal Source Analyzer
- Integration Bandwidth = 12kHz to 20MHz
- Spurious Activity (entire plot trace) = NOT Omitted (Normalized in dBc/Hz)
- Specifed Spur Omission Function = NOT Enabled
- IF Gain = 20dB
- Correlation = 5
- Average = 3

Typical Phase Noise and Jitter Characteristics (@ 25ºC ± 3ºC)

F=156.2500MHz
Vdd=3.3V
LVPECL
RMS Phase Jitter = 132 fsec



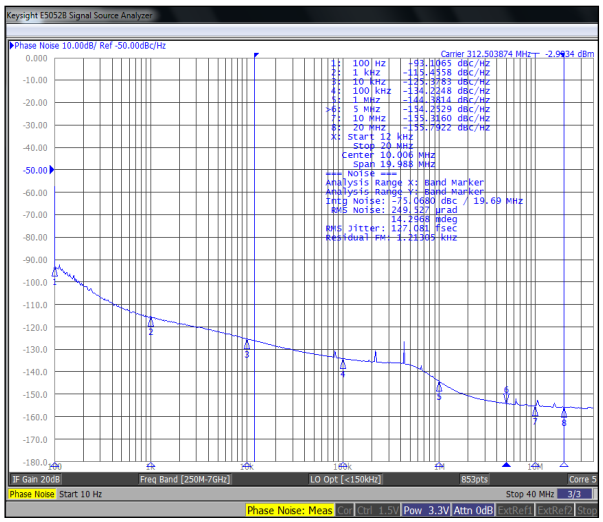
F=156.2500MHz
Vdd=3.3V
LVDS
RMS Phase Jitter = 165 fsec



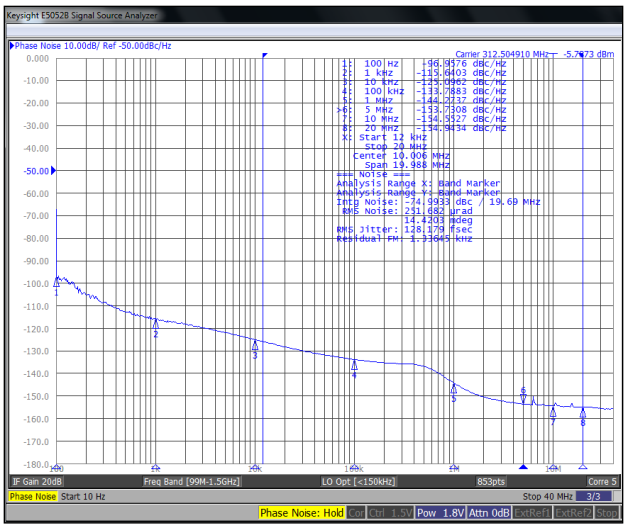
Note 8: Contact Abracon for phase noise plots at any desired combination of Vdd, differential output format, and carrier frequency within the available range

Typical Phase Noise and Jitter Characteristics (@ 25ºC ± 3ºC) *Continued*

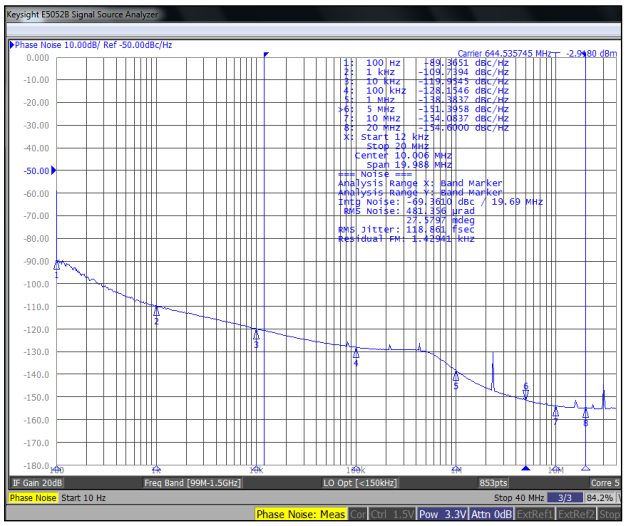
F=312.5000MHz | Vdd=3.3V | LVPECL
RMS Phase Jitter = 127 fsec



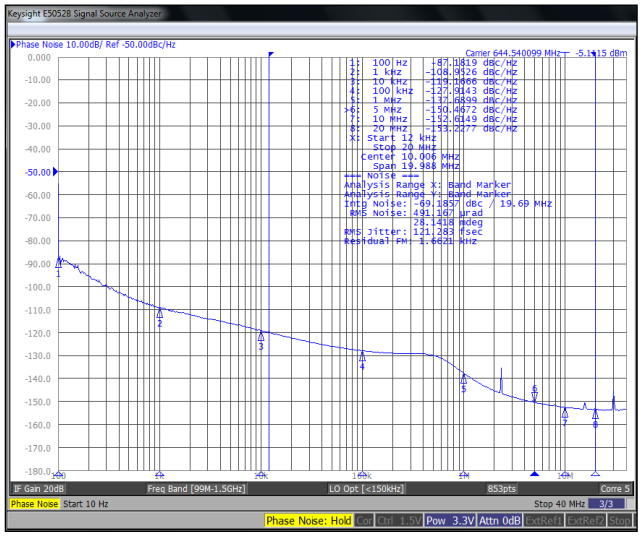
F=312.5000MHz| Vdd=1.8V | LVDS
RMS Phase Jitter = 128 fsec



F=644.53125MHz | Vdd=3.3V | LVPECL
RMS Phase Jitter = 118 fsec



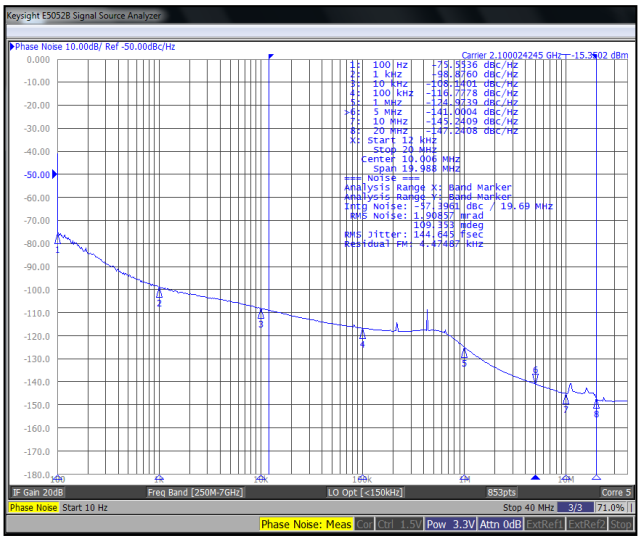
F=644.53125MHz | Vdd=3.3V | LVDS
RMS Phase Jitter = 121 fsec



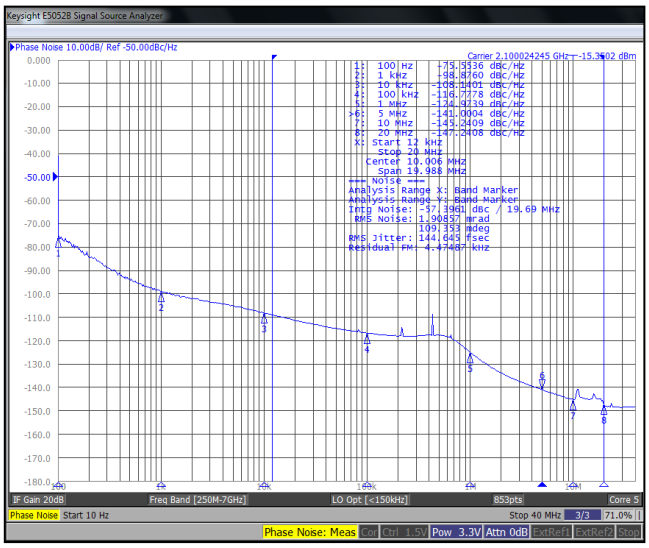
Note 8: Contact Abracon for phase noise plots at any desired combination of Vdd, differential output format, and carrier frequency within the available range

Typical Phase Noise and Jitter Characteristics (@ 25ºC ± 3ºC) *Continued*

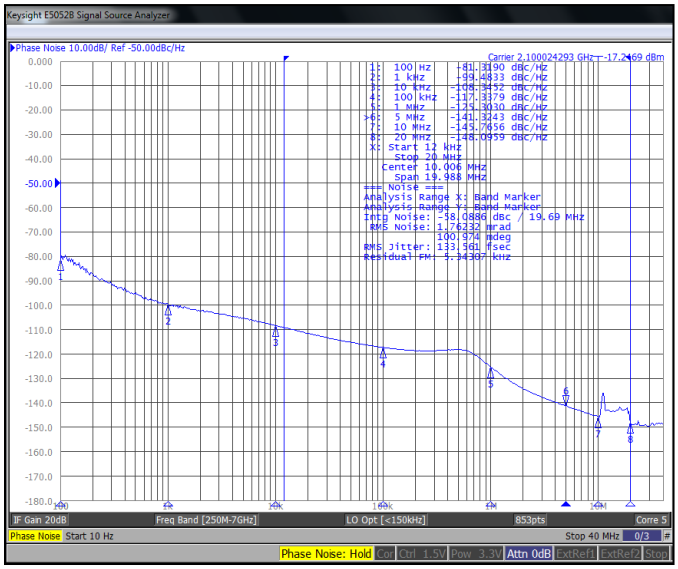
F=2100.0000MHz | Vdd=3.3V | LVPECL
RMS Phase Jitter = 144 fsec



F=2100.0000MHz | Vdd=3.3V | LVDS
RMS Phase Jitter = 135 fsec



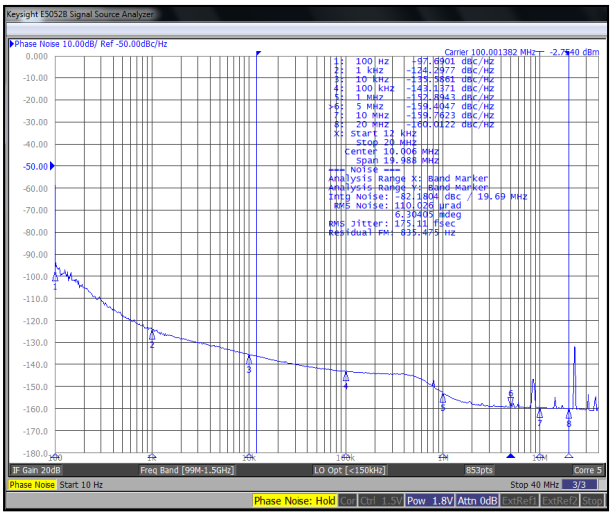
F=2100.0000MHz | Vdd=3.3V | CML
RMS Phase Jitter = 133 fsec



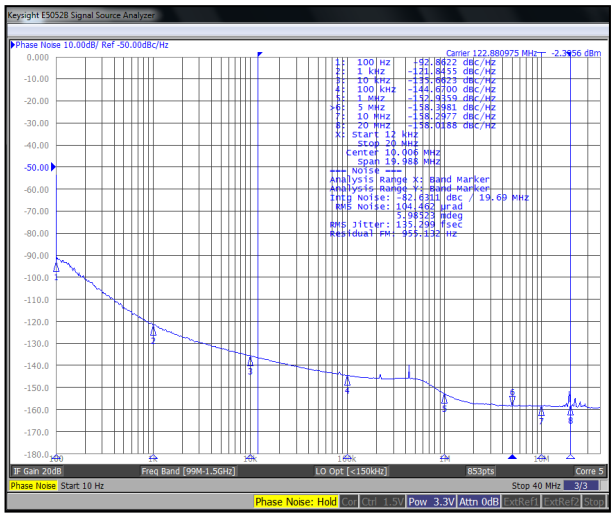
Note 8: Contact Abracon for phase noise plots at any desired combination of Vdd, differential output format, and carrier frequency within the available range

Typical Phase Noise and Jitter Characteristics (@ 25ºC ± 3ºC) *Continued*

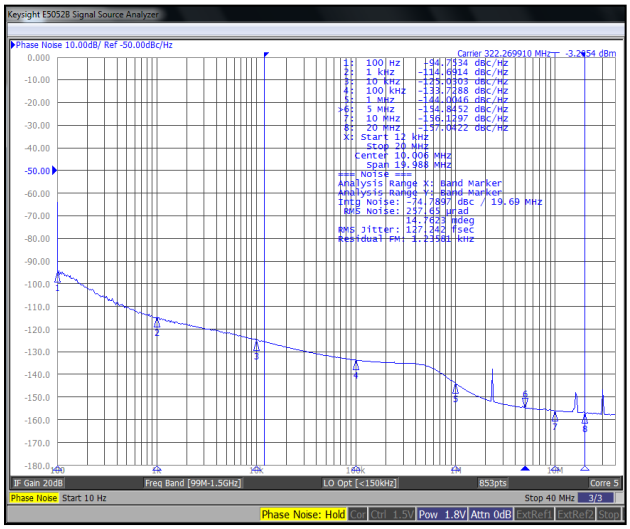
F=100.0000MHz | Vdd=1.8V | HCSL
RMS Phase Jitter = 175 fsec



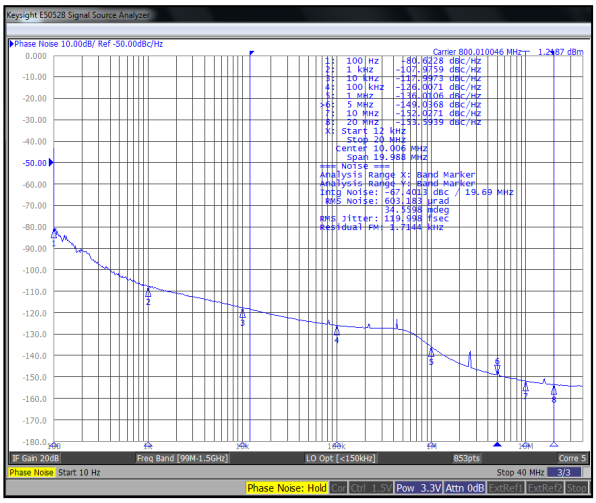
F=122.8800MHz | Vdd=3.3V | LVPECL
RMS Phase Jitter = 135 fsec



F=322.265625MHz | Vdd=1.8V | HCSL
RMS Phase Jitter = 127 fsec

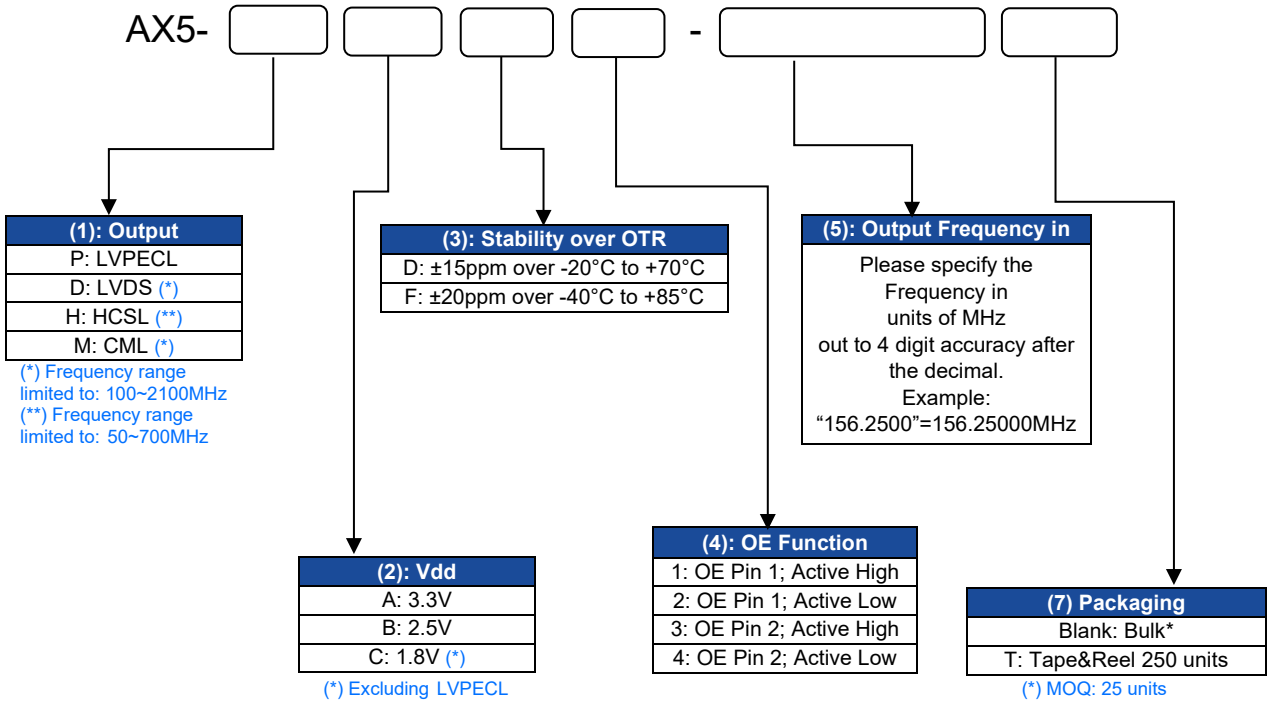


F=800.0000MHz | Vdd=3.3V | LVPECL
RMS Phase Jitter = 119 fsec



Note 8: Contact Abracon for phase noise plots at any desired combination of Vdd, differential output format, and carrier frequency within the available range

Part Identification (Left Blank If Standard) [Note 9]



Part Number Example:

AX5PAF1-644.53125

Note 9: Contact Abracon for non-standard part number configurations and/or requests with carrier frequency callouts up to 5 & 6 digit accuracy after the decimal.

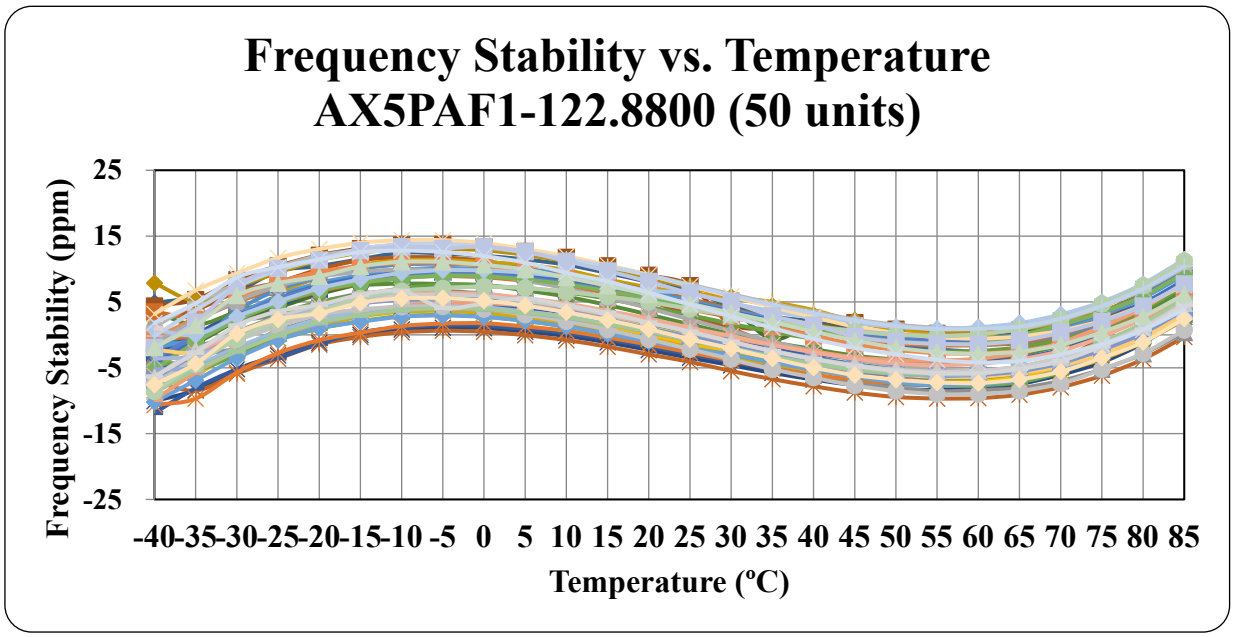
Cross Reference to SiLabs Si545 Family [Note 10]

Part Number[Note 10]

Si545	AX5	Frequency (MHz)	Output Logic	Vdd (V)
545AAA156M250BAG	AX5PxF1-156.2500	156.25000	LVPECL	2.5V, 3.3V
545AAA250M000BAG	AX5PxF1-250.0000	250.00000	LVPECL	2.5V, 3.3V
545BAA100M000BAG	AX5DxF1-100.0000	100.0000	LVDS	1.8V,2.5V,3.3V
545BAA622M080BAG	AX5DxF1-622.0800	622.08000	LVDS	1.8V,2.5V,3.3V
545AAA500M000BAG	AX5PxF1-500.0000	500.0000	LVPECL	2.5V, 3.3V
545AAA000127BAG	AX5PxF1-644.53125	644.53125	LVPECL	2.5V, 3.3V
545BAA500M000BAG	AX5DxF1-500.0000	500.0000	LVDS	1.8V,2.5V,3.3V
545AAA622M080BAG	AX5PxF1-622.08000	622.08000	LVPECL	2.5V, 3.3V
545BAA000127BAG	AX5DxF1-622.08000	622.08000	LVDS	1.8V,2.5V,3.3V
545AAA200M000BAG	AX5PxF1-200.0000	200.0000	LVPECL	2.5V, 3.3V
545BAA000275BAG	AX5DxF1-148.0000	148.0000	LVDS	1.8V,2.5V,3.3V
545AAA312M500BAG	AX5PxF1-312.5000	312.5000	LVPECL	2.5V, 3.3V
545AAA000274BAG	AX5PxF1-148.0000	148.0000	LVPECL	2.5V, 3.3V
545BAA312M500BAG	AX5DxF1-312.5000	312.5000	LVDS	1.8V,2.5V,3.3V
545AAA125M000BAG	AX5PxF1-125.0000	125.0000	LVPECL	2.5V, 3.3V
545AAA100M000BAG	AX5PxF1-100.0000	100.0000	LVPECL	2.5V, 3.3V
545BAA200M000BAG	AX5DxF1-200.0000	200.0000	LVDS	1.8V,2.5V,3.3V
545BAA125M000BAG	AX5DxF1-125.0000	125.0000	LVDS	1.8V,2.5V,3.3V
545BAA156M250BAG	AX5DxF1-156.2500	156.2500	LVDS	1.8V,2.5V,3.3V
545BAA250M000BAG	AX5DxF1-250.0000	250.0000	LVDS	1.8V,2.5V,3.3V

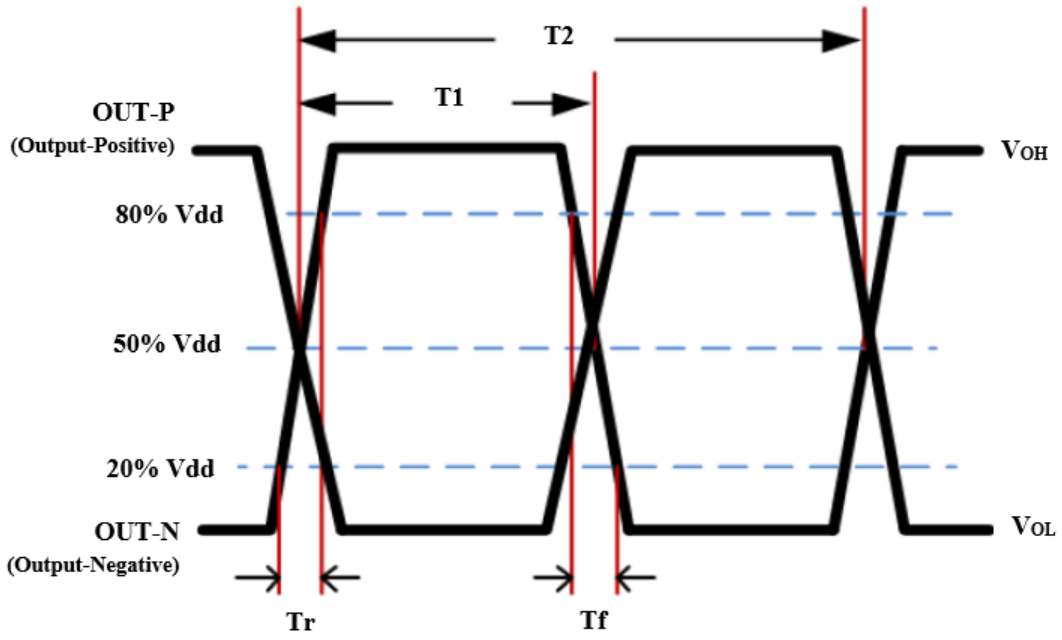
Note 10: The "x" in the AX5 part number is a placeholder for the supply voltage (Vdd) options below:
"x" = A = Vdd=3.3V
"x" = B = Vdd=2.5V
"x" = C = Vdd=1.8V (when applicable)

Typical Frequency vs. Temperature Characteristics



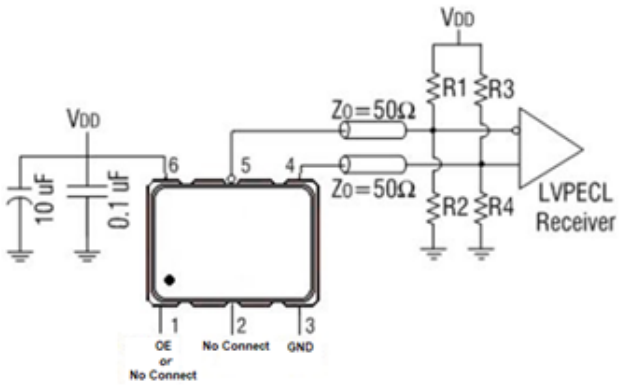
Differential Output Waveform

$$\text{Duty Cyle} = \left(\frac{T1}{T2}\right) * 100\% \text{ (measured at 50\% Vdd)}$$



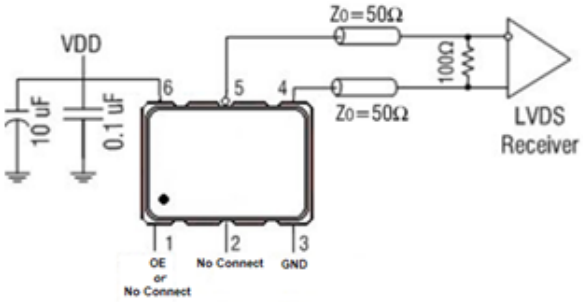
Recommended Test Circuit [Note 11]

LVPECL

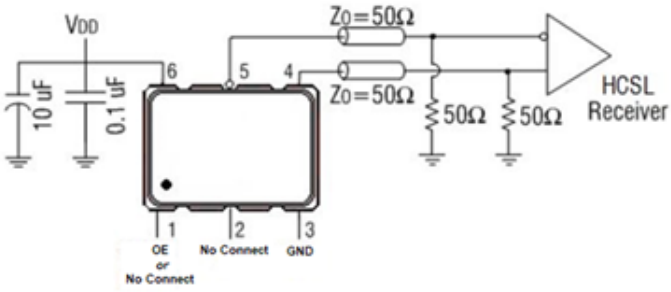


Vdd=3.3V: R1=R3=127Ω; R2=R4=82.5 Ω
Vdd=2.5V: R1=R3=250Ω: R2=R4=62.5 Ω

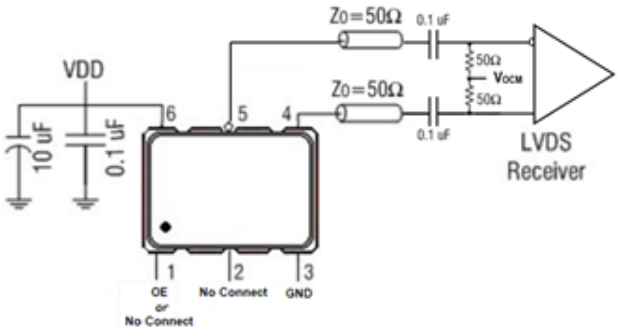
LVDS @ Vdd = 3.3V & 2.5V



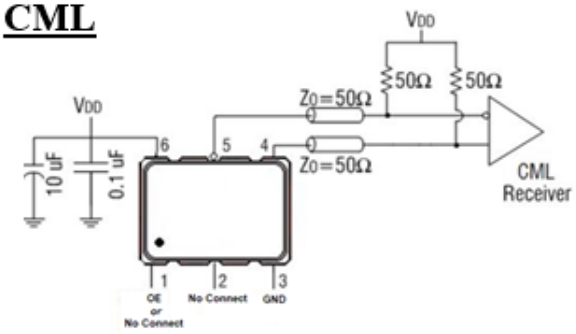
HCSL



LVDS @ Vdd = 1.8V



CML

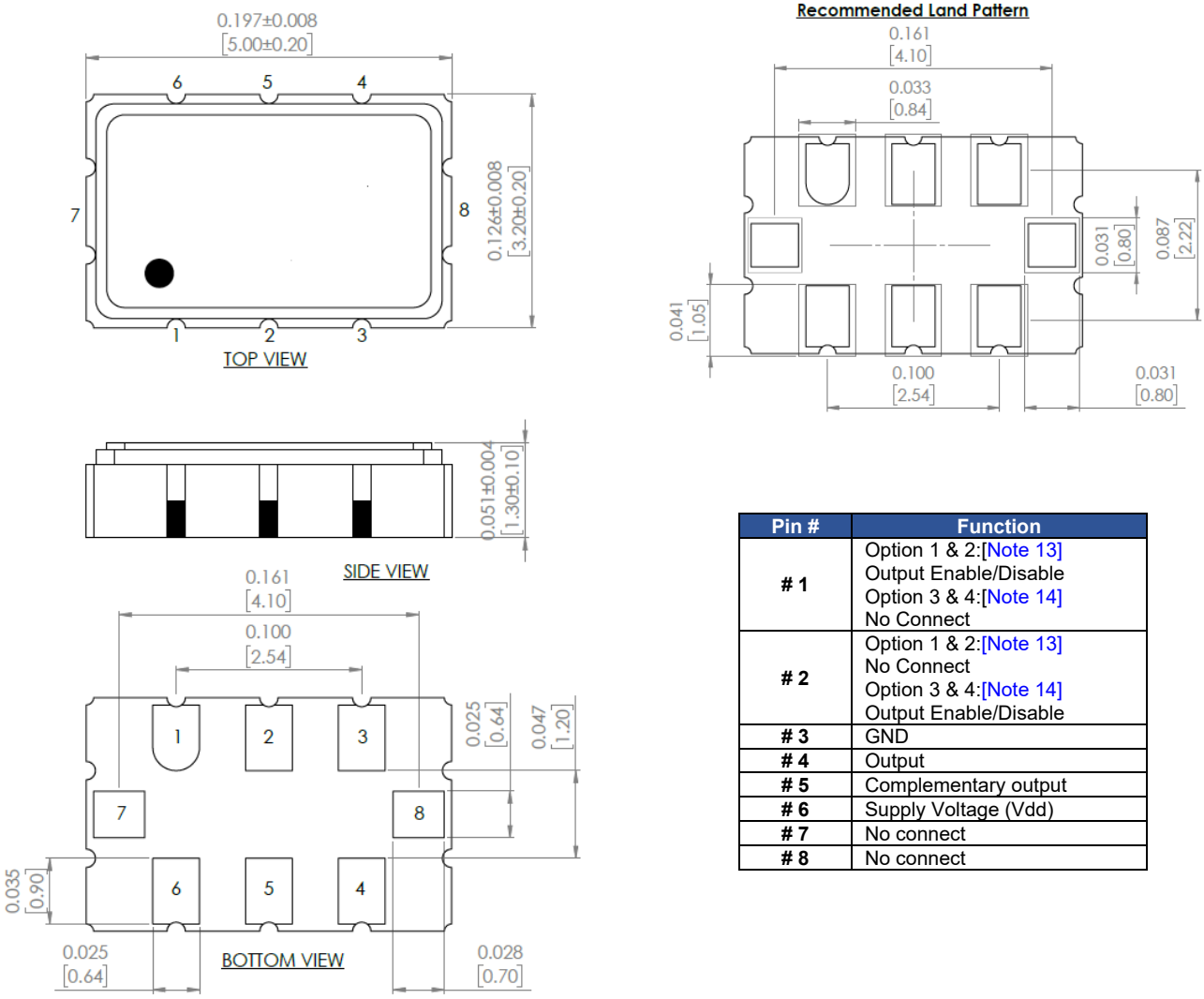


The output common mode voltage, V_{OCM}, is required to be supplied externally, where V_{OCM} = 1.3V.

AC coupling needs to be implemented between the clock device (oscillator) and the receiver circuit.

Note 11: Recommended test circuit images display OE Functions Option 1 & Option 2 where the OE Function is located on Pin 1. When the OE Function is located on Pin 2, then Pin 1=No Connect & Pin 2=OE or No Connect

Mechanical Dimensions



Pin #	Function
# 1	Option 1 & 2:[Note 13] Output Enable/Disable Option 3 & 4:[Note 14] No Connect
# 2	Option 1 & 2:[Note 13] No Connect Option 3 & 4:[Note 14] Output Enable/Disable
# 3	GND
# 4	Output
# 5	Complementary output
# 6	Supply Voltage (Vdd)
# 7	No connect
# 8	No connect

Note 12: Compatible with industry standard 5x3.2mm footprint. Pins #7 and #8 do not require a solder connection; it is not recommended to electrically connect the pins as they are for factory use only.
Note 13: Option 1 = Pin 1 Output Enable Active HIGH; Output Disable Active LOW
Option 2 = Pin 1 Output Enable Active LOW; Output Disable Active HIGH
Note 14: Option 3 = Pin 2 Output Enable Active HIGH; Output Disable Active LOW
Option 4 = Pin 2 Output Enable Active LOW; Output Disable Active HIGH

Dimensions: inches (mm)

Reflow Profile [JEDEC J-STD-020]

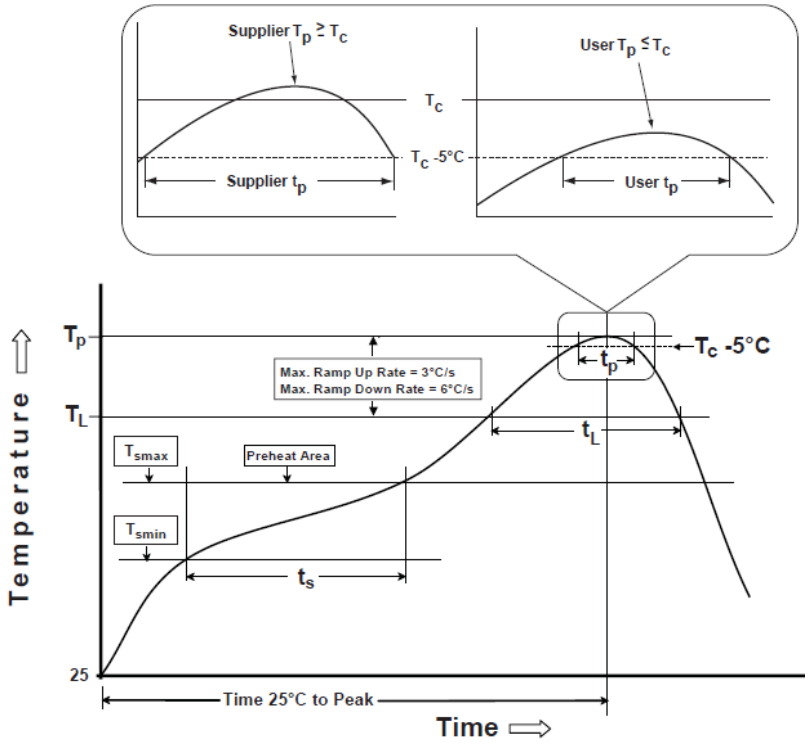


Table 1

SnPb Eutectic Process Classification Temperatures (T_c)		
Package Thickness	**Volume mm³ <350**	**Volume mm³ ≥350**
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2

Pb-Free Process Classification Temperatures (T_c)			
Package Thickness	**Volume mm³ <350**	**Volume mm³ 350-2000**	**Volume mm³ >2000**
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

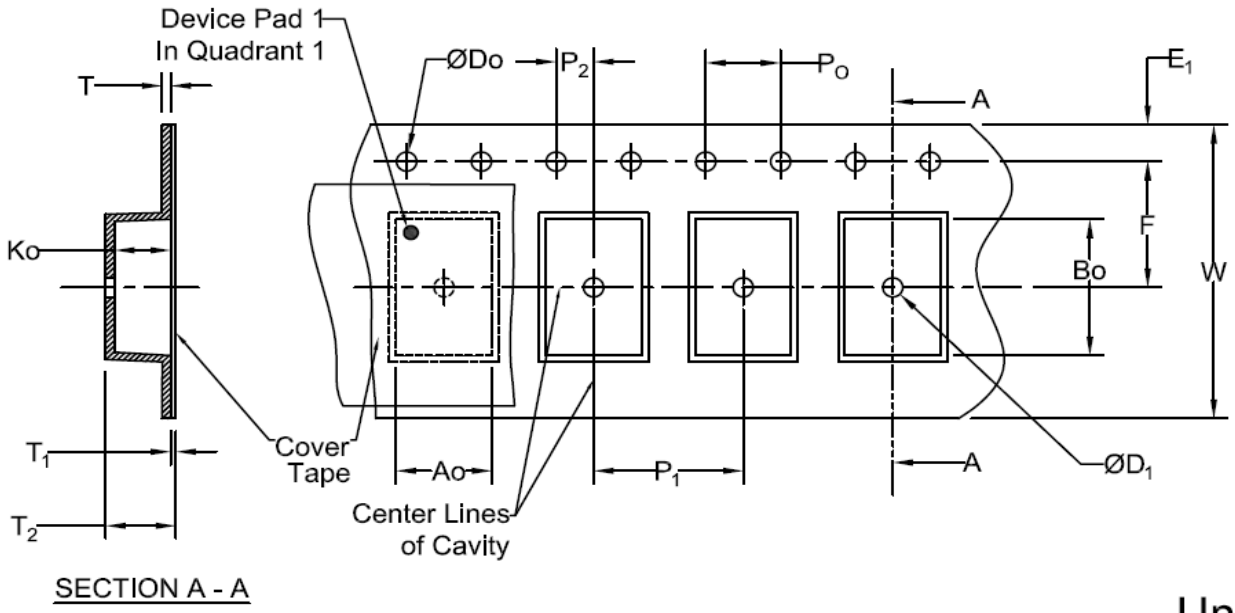
Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat / soak		
Temperature minimum (T_{smin})	100°C	150°C
Temperature maximum (T_{smax})	150°C	200°C
Time (T_{smin} to T_{smax}) (t_s)	60 - 120 sec.	60 - 120 sec.
Average ramp-up rate (T_{smax} to T_P)	3°C/sec. max	3°C/sec. max
Liquidous temperature (T_L)	183°C	217°C
Time at liquidous (t_L)	60 - 150 sec.	60 - 150 sec.
Peak package body temperature (T_P)*	**see Table 1**	**see Table 2**
Time (t_p)** within 5°C of the specified classification temperature (T_C)	20 sec.	30 sec.
Ramp-down rate (T_p to T_{smax})	6°C/sec. max	6°C/sec. max
Time 25°C to peak temperature	6 min. max	8 min. max
Reflow cycles	2 max	2 max

*Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.

**Tolerance for time at peak profile temperature (t_p) is defined as supplier minimum and a user maximum.

Packaging

Blank = Bulk*
T = Tape & Reel 250 units/reel



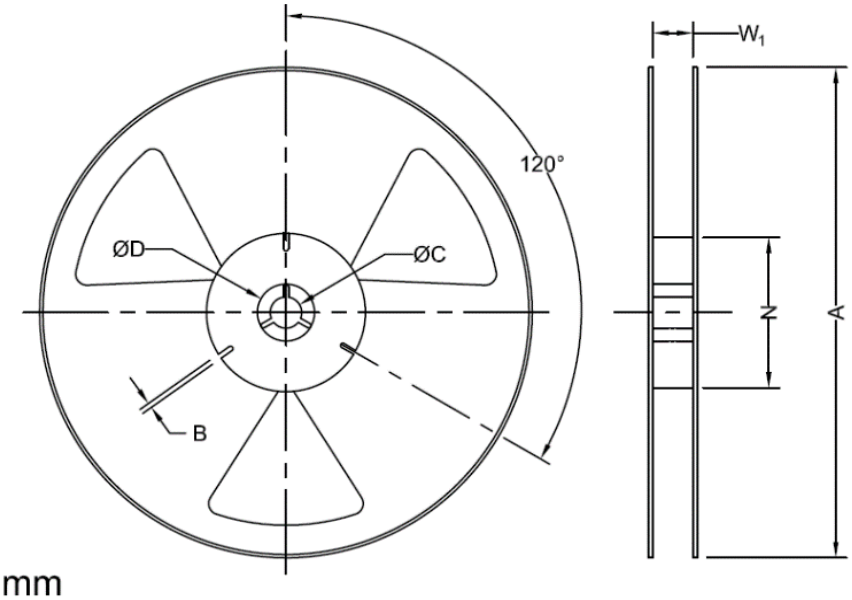
Unit: mm

Tape Specifications (mm)							
Width	Ao	Bo	Do	D_1 (Min)	E_1	F	Ko
12mm	*	*	1.5+0.1/-0.0	1.0	1.75±0.1	5.5±0.05	*

Tape Specifications (mm)							
Width	P_1	P_2	P_0	T (Max)	T_1 (Max)	T_2 (Max)	W (Max)
12mm	8.0±0.1	2.0±0.05	4.0±0.1	0.6	0.1	6.5	12.3

***Note: Compliant to EIA-481**

Dimensions: inches (mm)



Unit: mm

Tape Specifications (mm)							
Width	Qty/Reel	A (Nom)	B (Min)	C (Min)	D (Min)	N (Min)	*W_1
12mm	250	178	1.5	13.0+0.5/-0.2	20.2	50	12.4+2.0/-0.0

***Note: Measured at Hub**

Dimensions: inches (mm)