

NTB65N02R, NTP65N02R

Power MOSFET 65 A, 24 V N-Channel TO-220, D²PAK

Features

- Planar HD3e Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Pb-Free Packages are Available*

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ Unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	25	V_{dc}
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	V_{dc}
Thermal Resistance – Junction-to-Case Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Drain Current – Continuous @ $T_C = 25^\circ\text{C}$, Chip Continuous @ $T_C = 25^\circ\text{C}$, Limited by Package Single Pulse ($t_p = 10 \mu\text{s}$)	$R_{\theta JC}$ P_D I_D I_D I_{DM}	2.0 62.5 65 58 160	$^\circ\text{C/W}$ W A A A
Thermal Resistance – Junction-to-Ambient (Note 1) Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	$R_{\theta JA}$ P_D I_D	67 1.86 10	$^\circ\text{C/W}$ W A
Thermal Resistance – Junction-to-Ambient (Note 2) Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	$R_{\theta JA}$ P_D I_D	120 1.04 7.6	$^\circ\text{C/W}$ W A
Operating and Storage Temperature Range	T_J and T_{stg}	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 50 V_{dc}$, $V_{GS} = 10 V_{dc}$, $I_L = 11 A_{pk}$, $L = 1 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	60	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds	T_L	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- When surface mounted to an FR4 board using 1 in. pad size, (Cu Area 1.127 in²).
- When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in²).

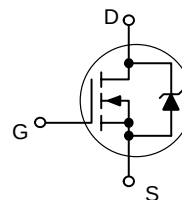
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



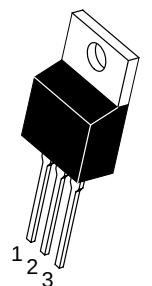
ON Semiconductor®

<http://onsemi.com>

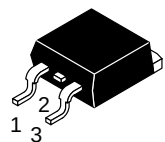
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
24 V	8.4 m Ω @ 10 V	65 A



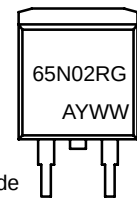
MARKING DIAGRAMS



TO-220AB
CASE 221A
STYLE 5



D²PAK
CASE 418AA
STYLE 2



65N02R = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

PIN ASSIGNMENT

PIN	FUNCTION
1	Gate
2	Drain
3	Source
4	Drain

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTB65N02R, NTP65N02R

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ Unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) ($V_{GS} = 0\text{ V}_{dc}$, $I_D = 250\text{ }\mu\text{A}_{dc}$) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	24 –	27.5 25.5	– –	V_{dc} $\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current ($V_{DS} = 20\text{ V}_{dc}$, $V_{GS} = 0\text{ V}_{dc}$) ($V_{DS} = 20\text{ V}_{dc}$, $V_{GS} = 0\text{ V}_{dc}$, $T_J = 150^\circ\text{C}$)	I_{DSS}	– –	– –	1.5 10	μA_{dc}
Gate-Body Leakage Current ($V_{GS} = \pm 20\text{ V}_{dc}$, $V_{DS} = 0\text{ V}_{dc}$)	I_{GSS}	–	–	± 100	nA_{dc}

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) ($V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}_{dc}$) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	1.0 –	1.5 4.1	2.0 –	V_{dc} $\text{mV}/^\circ\text{C}$
Static Drain-to-Source On-Resistance (Note 3) ($V_{GS} = 4.5\text{ V}_{dc}$, $I_D = 15\text{ A}_{dc}$) ($V_{GS} = 10\text{ V}_{dc}$, $I_D = 20\text{ A}_{dc}$) ($V_{GS} = 10\text{ V}_{dc}$, $I_D = 30\text{ A}_{dc}$)	$R_{DS(on)}$	– – –	11.2 8.4 8.2	12.5 10.5 –	$\text{m}\Omega$
Forward Transconductance (Note 3) ($V_{DS} = 10\text{ V}_{dc}$, $I_D = 15\text{ A}_{dc}$)	g_{FS}	–	27	–	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 20\text{ V}_{dc}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$)	C_{iss}	–	948	1330	pF
Output Capacitance		C_{oss}	–	456	640	
Transfer Capacitance		C_{rss}	–	160	225	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$(V_{GS} = 10\text{ V}_{dc}$, $V_{DD} = 10\text{ V}_{dc}$, $I_D = 30\text{ A}_{dc}$, $R_G = 3\text{ }\Omega$)	$t_{d(on)}$	–	7.0	–	ns
Rise Time		t_r	–	53	–	
Turn-Off Delay Time		$t_{d(off)}$	–	14	–	
Fall Time		t_f	–	10	–	
Gate Charge	$(V_{GS} = 4.5\text{ V}_{dc}$, $I_D = 30\text{ A}_{dc}$, $V_{DS} = 10\text{ V}_{dc}$) (Note 3)	Q_T	–	9.5	–	nC
		Q_1	–	3.0	–	
		Q_2	–	4.4	–	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	$(I_S = 20\text{ A}_{dc}$, $V_{GS} = 0\text{ V}_{dc}$) (Note 3) $(I_S = 30\text{ A}_{dc}$, $V_{GS} = 0\text{ V}_{dc}$) $(I_S = 15\text{ A}_{dc}$, $V_{GS} = 0\text{ V}_{dc}$, $T_J = 125^\circ\text{C}$)	V_{SD}	– – –	0.88 1.10 0.80	1.2 – –	V_{dc}
Reverse Recovery Time	$(I_S = 30\text{ A}_{dc}$, $V_{GS} = 0\text{ V}_{dc}$, $dI_S/dt = 100\text{ A}/\mu\text{s}$) (Note 3)	t_{rr}	–	29.1	–	ns
		t_a	–	13.6	–	
		t_b	–	15.5	–	
Reverse Recovery Stored Charge		Q_{RR}	–	0.02	–	μC

3. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

NTB65N02R, NTP65N02R

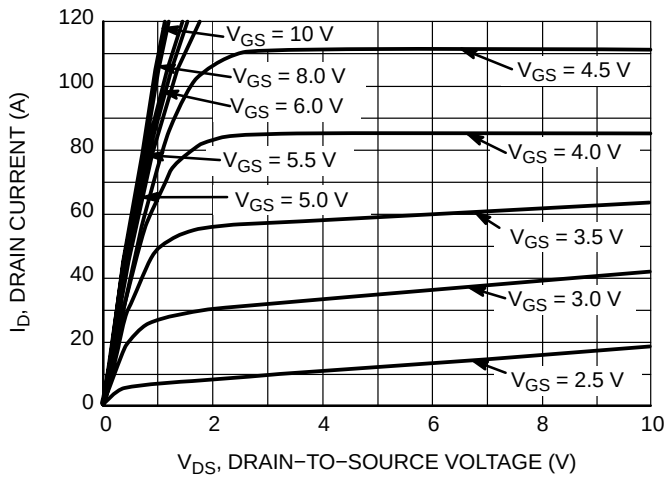


Figure 1. On-Region Characteristics

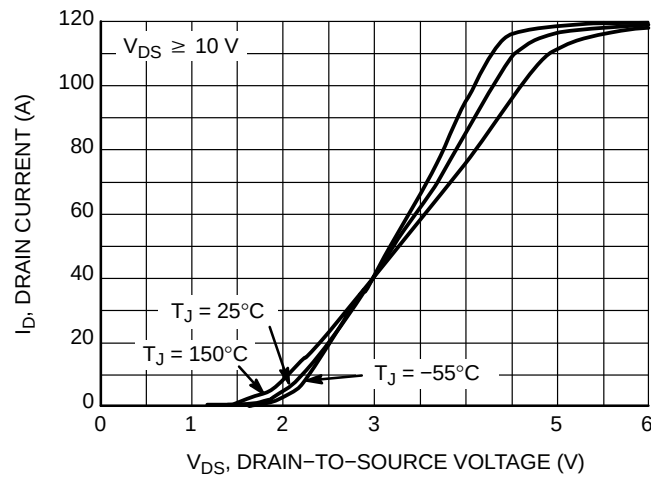


Figure 2. Transfer Characteristics

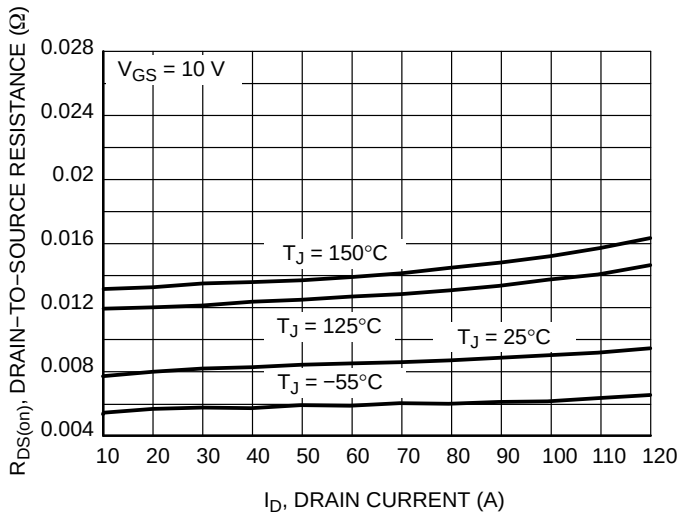


Figure 3. On-Resistance versus Drain Current and Temperature

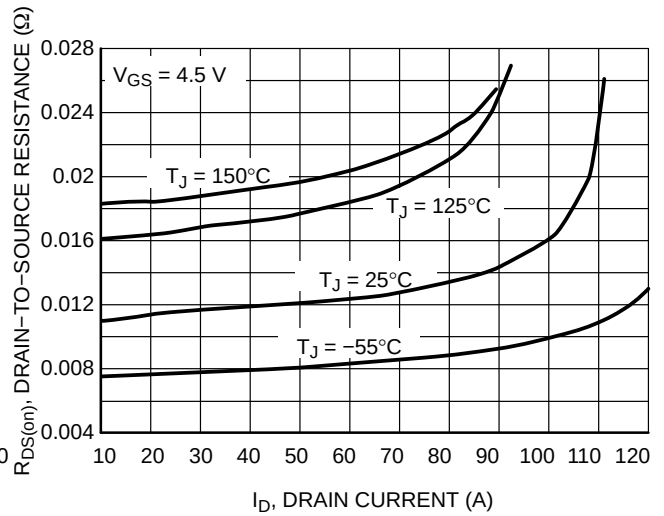


Figure 4. On-Resistance versus Drain Current and Temperature

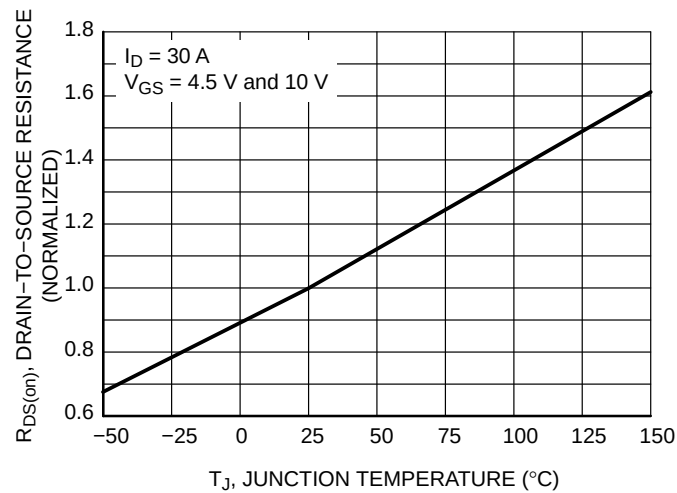


Figure 5. On-Resistance Variation with Temperature

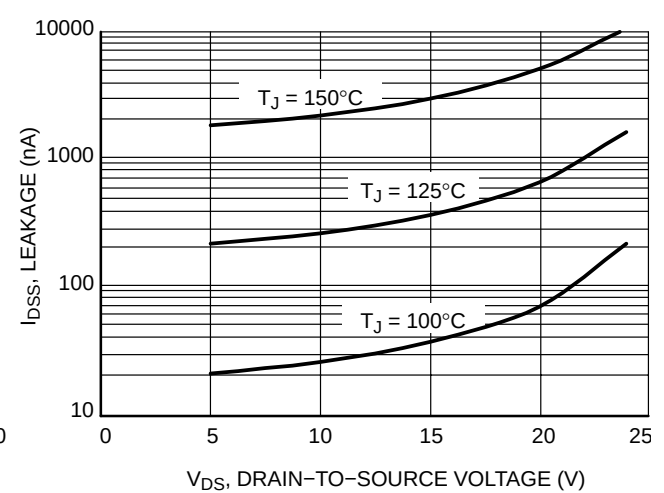
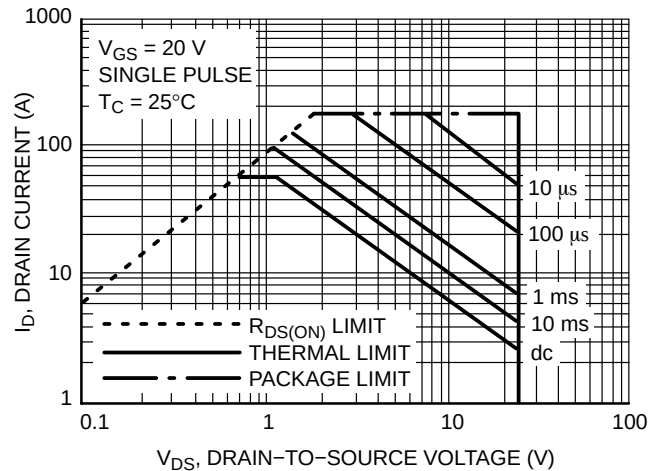
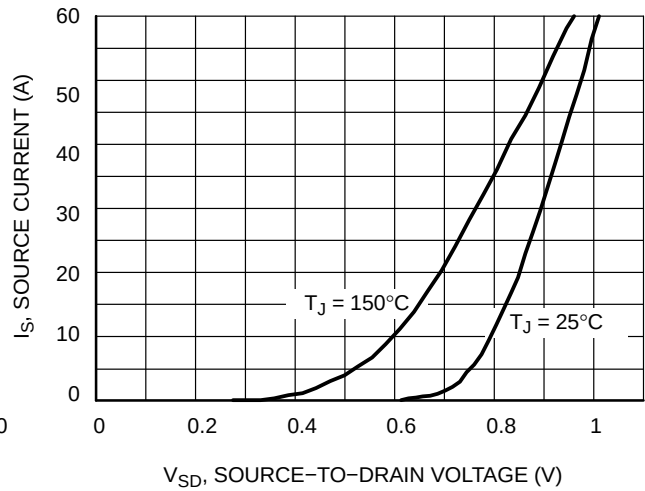
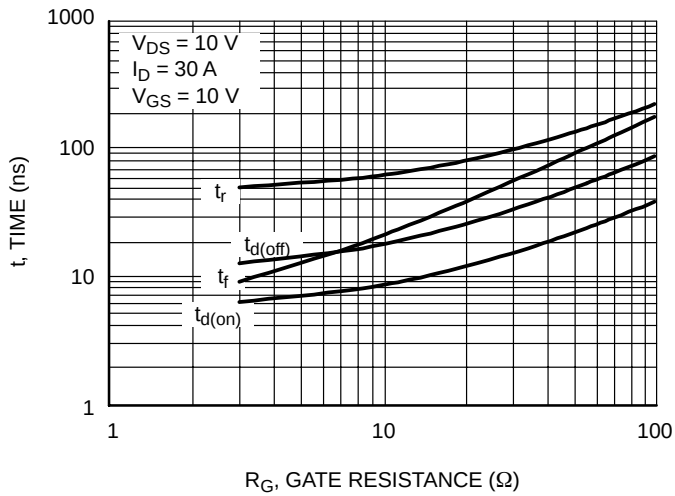
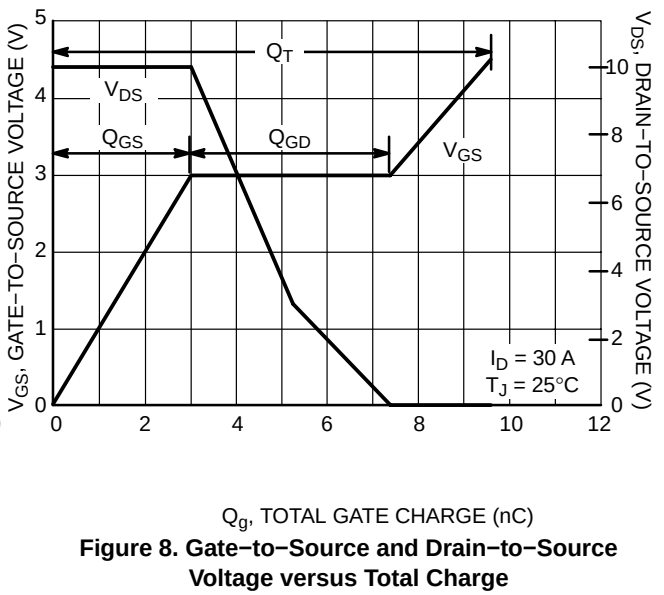
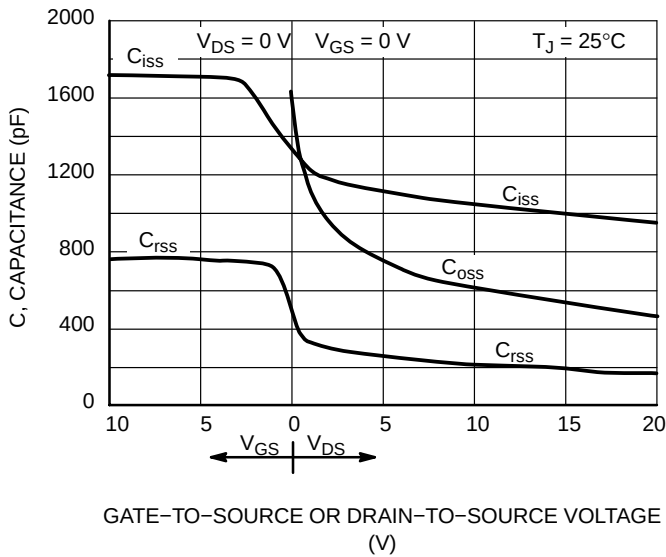


Figure 6. Drain-to-Source Leakage Current versus Voltage

NTB65N02R, NTP65N02R



NTB65N02R, NTP65N02R

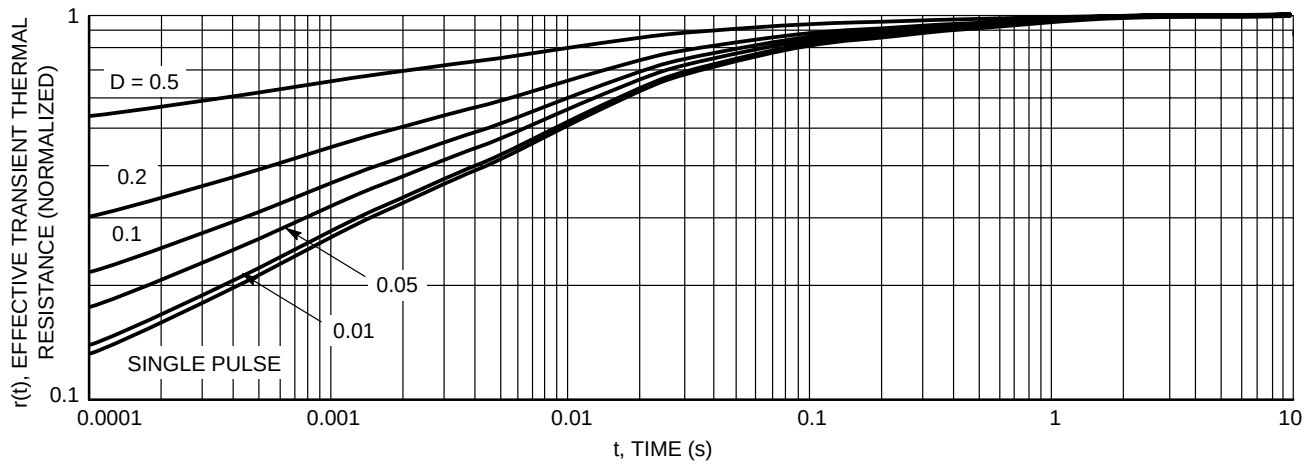
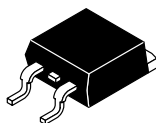


Figure 12. Thermal Response

ORDERING INFORMATION

Device	Package	Shipping [†]
NTB65N02R	D ² PAK	50 Units / Rail
NTB65N02RG	D ² PAK (Pb-Free)	50 Units / Rail
NTB65N02RT4	D ² PAK	800 / Tape & Reel
NTB65N02RT4G	D ² PAK (Pb-Free)	800 / Tape & Reel
NTP65N02R	TO-220AB	50 Units / Rail
NTP65N02RG	TO-220AB (Pb-Free)	50 Units / Rail

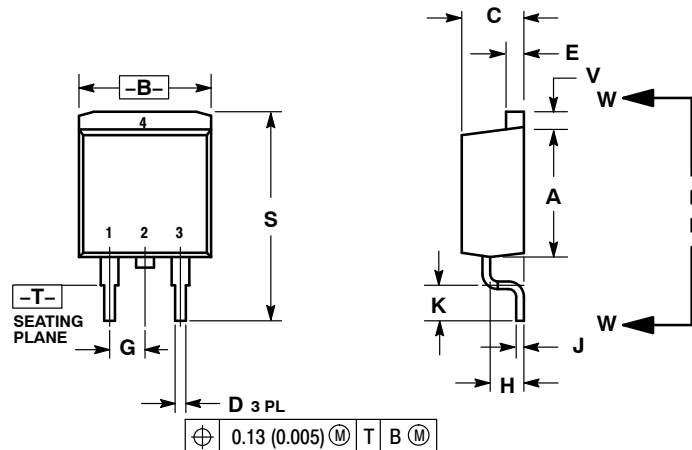
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



D²PAK 3
CASE 418B-04
ISSUE L

DATE 17 FEB 2015

SCALE 1:1

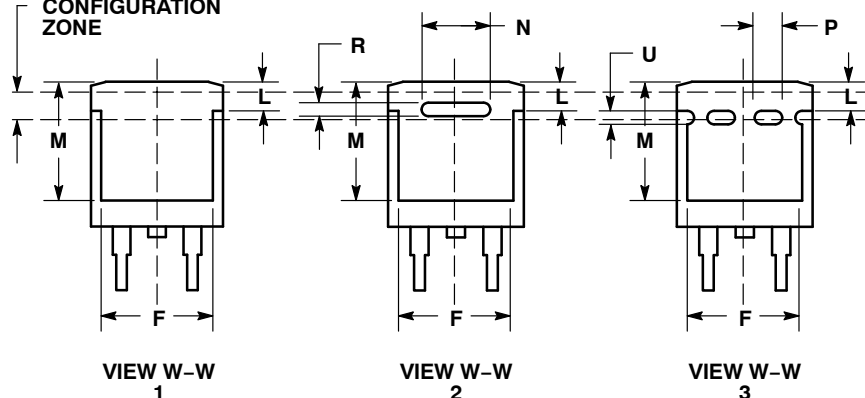


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197	REF	5.00	REF
P	0.079	REF	2.00	REF
R	0.039	REF	0.99	REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

VARIABLE
CONFIGURATION
ZONE



STYLE 1:

- PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:

- PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:

- PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5:

- PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:

- PIN 1. NO CONNECT
2. CATHODE
3. ANODE
4. CATHODE

MARKING INFORMATION AND FOOTPRINT ON PAGE 2

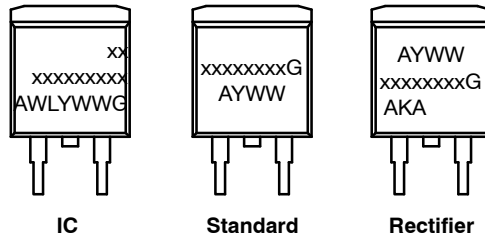
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ISSUE L

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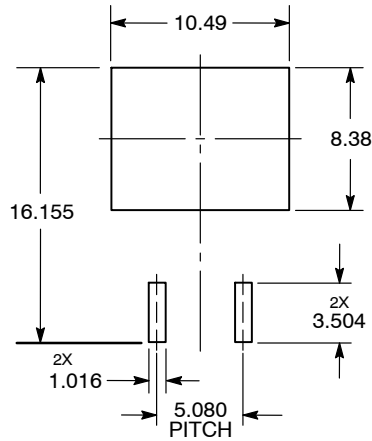
**GENERIC
MARKING DIAGRAM***



xx = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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