# PE4239

## Product Specification

*SPDT UltraCMOS® RF Switch*

## Features

- Single-pin or complementary CMOS logic control inputs
- +3.0V power supply needed for single-pin control mode
- Low insertion loss:
  - 0.7 dB at 1.0 GHz
  - 0.9 dB at 2.0 GHz
- Isolation:
  - 32 dB at 1.0 GHz
  - 23 dB at 2.0 GHz
- Typical input 1 dB compression point: +25 dBm
- Packaging: 6-lead SC-70

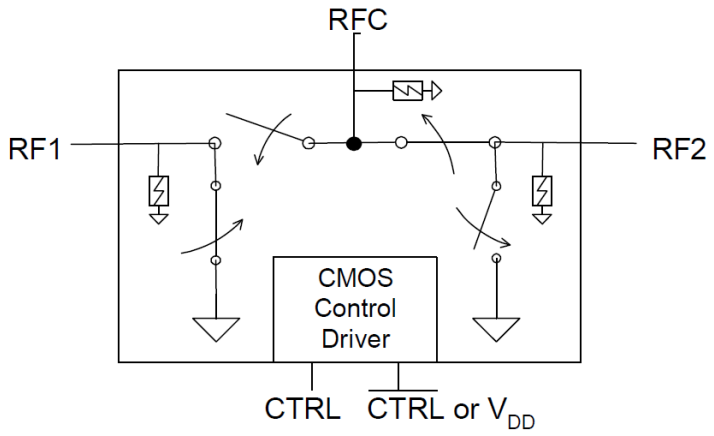


*Figure 1. PE4239 functional diagram*

## Product description

The PE4239 UltraCMOS® RF switch is designed to cover a broad range of applications from DC through 3.0 GHz. This reflective switch integrates on-board CMOS control logic with a low voltage CMOS-compatible control interface and can be controlled using either single-pin or complementary control inputs. Using a nominal +3V power supply voltage, a typical input 1 dB compression point of +25 dBm can be achieved.

The PE4239 UltraCMOS RF switch is manufactured on pSemi's UltraCMOS process, a patented variation of silicon-on-insulator (SOI) technology.



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# Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

## ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

## Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. Absolute maximum ratings

| Parameter or condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | -0.3 | 4.0 | V |
| Voltage on any input | $V_I$ | -0.3 | $V_{DD}$ + 0.3 | V |
| Storage temperature range | $T_{ST}$ | -65 | 150 | °C |
| Operating temperature range | $T_{OP}$ | -55 | 85 | °C |
| Input power, 50Ω | $P_{IN}$ | – | 30 | dBm |
| ESD voltage, Human Body Model | $V_{ESD}$ | – | 1000 | V |

# Electrical specifications

Table 2 lists the PE4239 key electrical specifications at +25 °C $T_{CASE}$ and $V_{DD}$ = 5V ($Z_S$ = $Z_L$ = 50Ω), unless otherwise specified.

Table 2. Electrical specifications

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operating frequency(1) | – | DC | – | 3000 | MHz |
| Insertion loss | 1000 MHz<br>2000 MHz | – | 0.7<br>0.9 | 0.85<br>1.05 | dB |
| Isolation | 1000 MHz<br>2000 MHz | 30<br>21 | 32<br>23 | – | dB |
| Return loss | 1000 MHz<br>2000 MHz | 18<br>16 | 20<br>18 | – | dB |
| ON switching time | 50% CTRL to 0.1 dB of final value, 1 GHz | – | 300 | – | ns |
| OFF switching time | 50% CTRL to 25 dB isolation, 1 GHz | – | 200 | – | ns |
| Video feedthrough(2) | – | – | 15 | – | $mV_{PP}$ |
| Input 1-dB compression point | 2000 MHz | 23 | 25 | – | dBm |
| Input IP3 | 2000 MHz, 14 dBm input power | 43 | 45 | – | dBm |
| **DC electrical specifications** | | | | | |
| Power supply voltage, $V_{DD}$ | – | 2.7 | 3.0 | 3.3 | V |
| Power supply current, $I_{DD}$ | $V_{DD}$ = 3V, $V_{CTRL}$ = 3V | – | 250 | 500 | nA |
| Control voltage high | – | 0.7 × $V_{DD}$ | – | – | V |
| Control voltage low | – | – | – | 0.3 × $V_{DD}$ | V |

Notes:
1. Device linearity begins to degrade below 10 MHz.
2. The DC transient at the output of any port of the switch when the control voltage is switched from low-to-high or high-to-low in a 50Ω test set-up, measured with 1 ns risetime pulses and 500-MHz bandwidth.

# Control logic

Table 3. Single-pin control logic truth table

| Control voltages | Signal path |
|---|---|
| Pin 6 ($\overline{CTRL}$ or $V_{DD}$) = $V_{DD}$<br>Pin 4 (CTRL) = High | RFC to RF1 |
| Pin 6 ($\overline{CTRL}$ or $V_{DD}$) = $V_{DD}$<br>Pin 4 (CTRL) = Low | RFC to RF2 |

Table 4. Complementary-pin control logic truth table

| Control voltages | Signal path |
|---|---|
| Pin 6 ($\overline{CTRL}$ or $V_{DD}$) = Low<br>Pin 4 (CTRL) = High | RFC to RF1 |
| Pin 6 ($\overline{CTRL}$ or $V_{DD}$) = High<br>Pin 4 (CTRL) = Low | RFC to RF2 |

## Control logic input

The PE4239 is a versatile RF switch that supports two operating control modes: single-pin control mode and complementary-pin control mode:

- *Single-pin control mode* enables the switch to operate with a single control pin (pin 4) supporting a +3V CMOS logic input and requires a dedicated +3V power supply connection on pin 6 ($V_{DD}$). This mode of operation reduces the number of control lines required and simplifies the switch control interface typically derived from a CMOS microprocessor I/O port.
- *Complementary-pin control mode* allows the switch to operate using complementary control pins CTRL and $\overline{CTRL}$ (pins 4 and 6, respectively), that can be directly driven by +3V CMOS logic or a suitable microprocessor I/O port. This enables the PE4239 to be used as a potential alternate source for SPDT RF switch products used in positive control voltage mode and operating within the PE4239 operating limits.

# Typical performance data

Figure 2–Figure 7 show the typical performance data at -40 °C to 85 °C, unless otherwise specified.

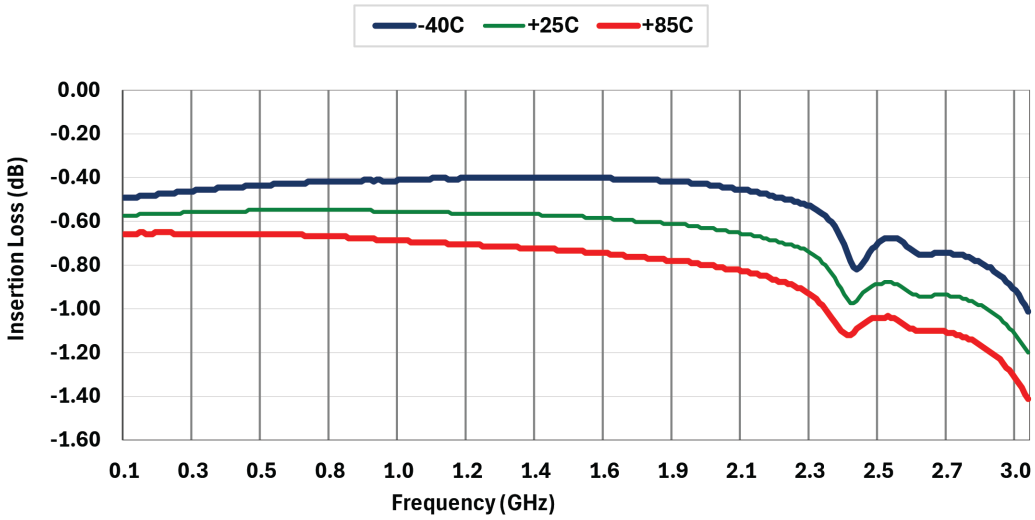



*Figure 2. Insertion loss, RFC to RF1*

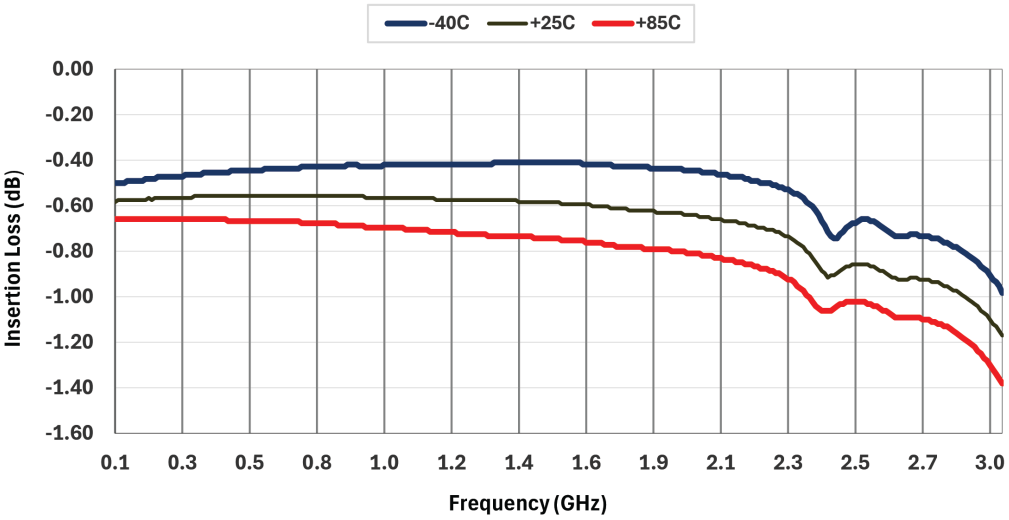



*Figure 3. Insertion loss, RFC to RF2*

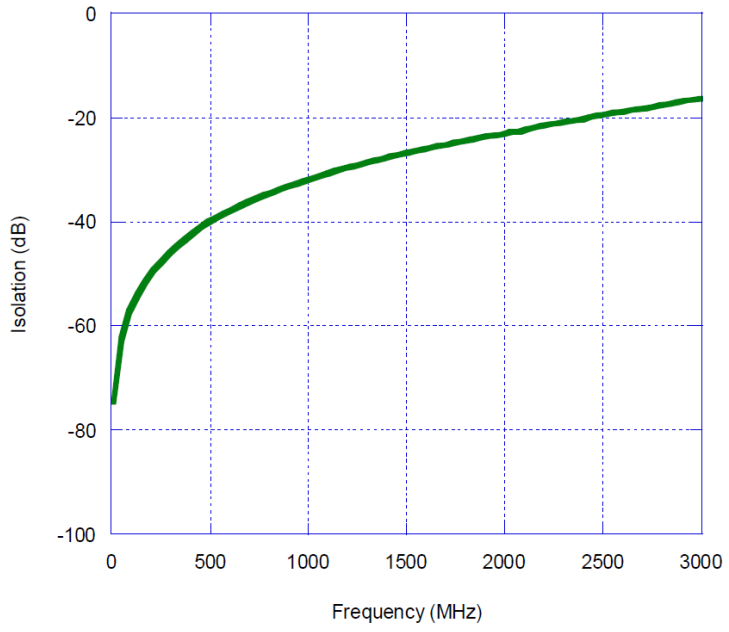



*Figure 4. Isolation, RFC to RF1*

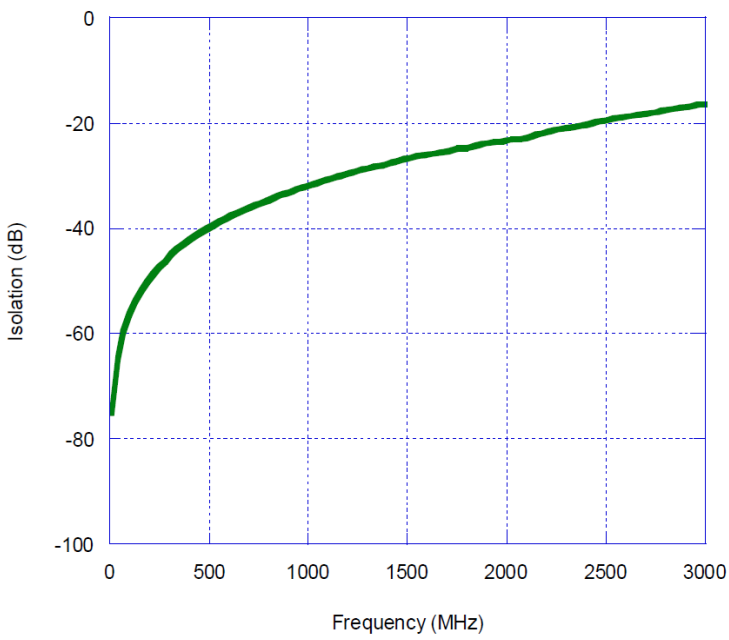



*Figure 5. Isolation, RFC to RF2*

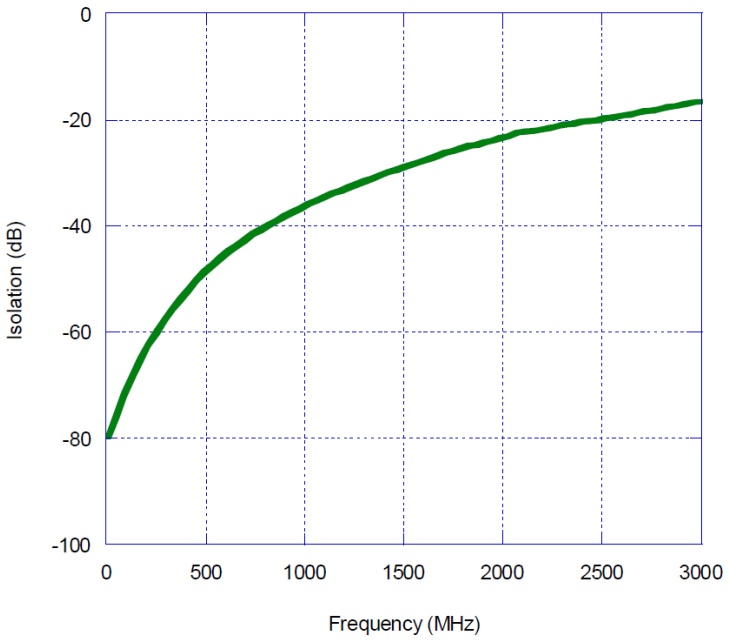



*Figure 6. Isolation, RF1 to RF2, RF2 to RF1*

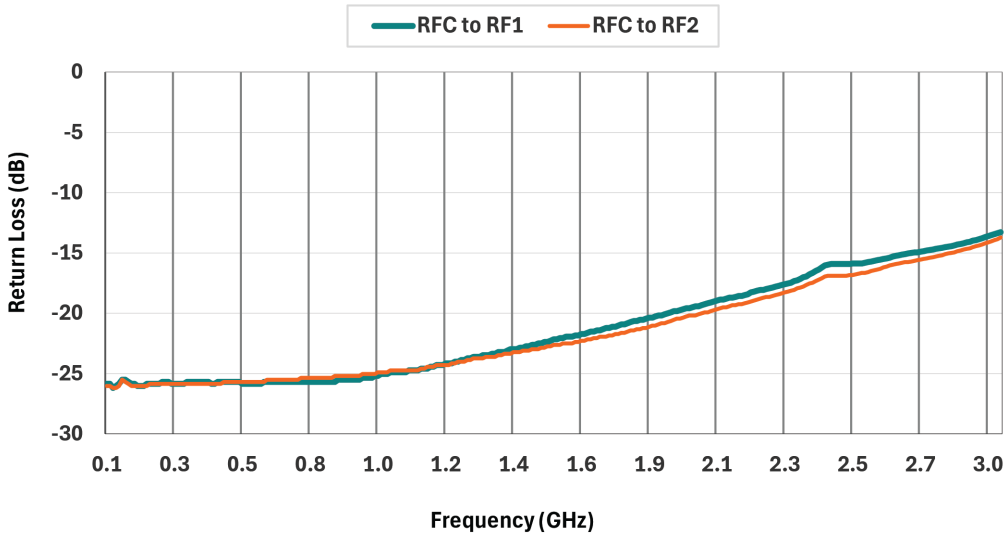



*Figure 7. Return loss, RFC to RF1, RF2*

# Evaluation kit

pSemi designed the SPDT switch evaluation board to ease your evaluation of the PE4239. The RF common port connects through a 50Ω transmission line to the top left SMA connector, J1.

Ports 1 and 2 connect through 50Ω transmission lines to the top two SMA connectors on the right side of the board, J3 and J2, respectively. A through transmission line connects SMA connectors J4 and J5. You can use this transmission line to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two-metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.0476", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0021", and εr of 4.4.

J6 provides a means for controlling DC and digital inputs to the device. Starting from the lower left pin, the second pin to the right (J6-3) connects to the device V1 or CTRL input. The fourth pin to the right (J6-7) connects to the device V2 or the $\overline{CTRL}/V_{DD}$ input.

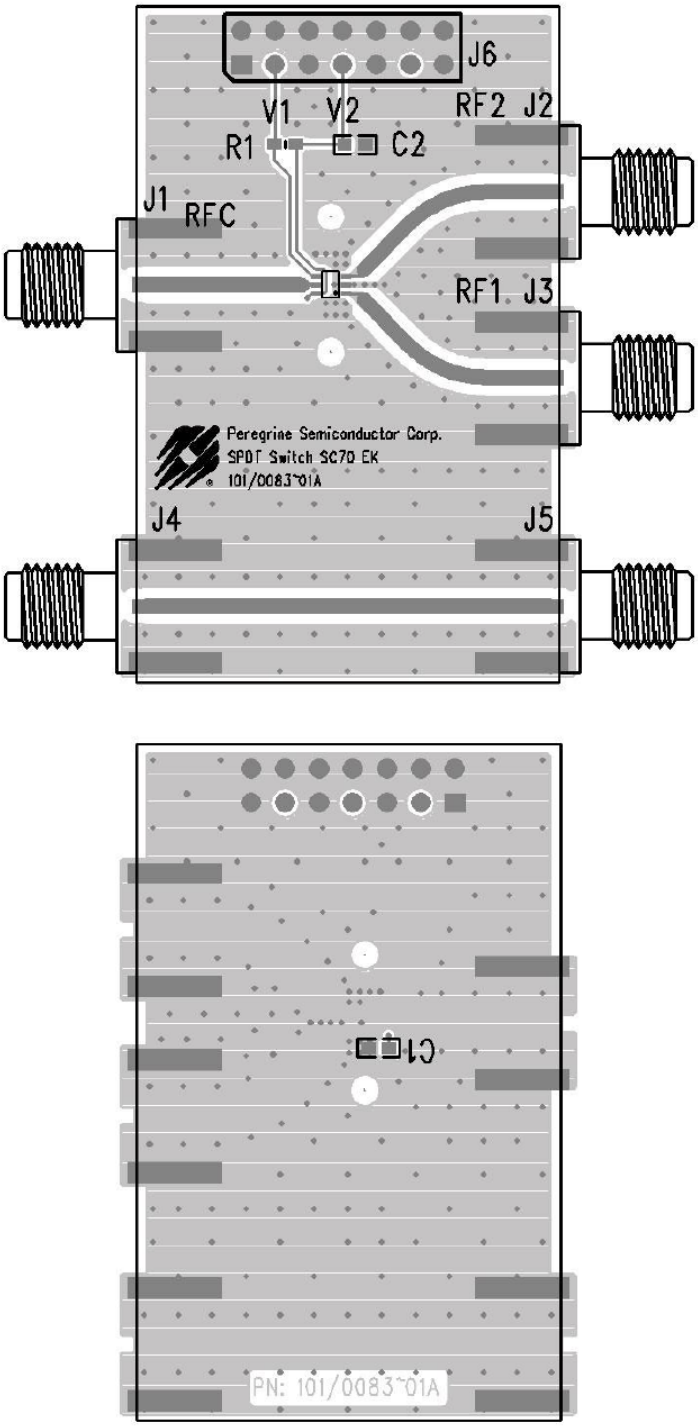



*Figure 8. Evaluation board layout (pSemi specification 101/0083)*

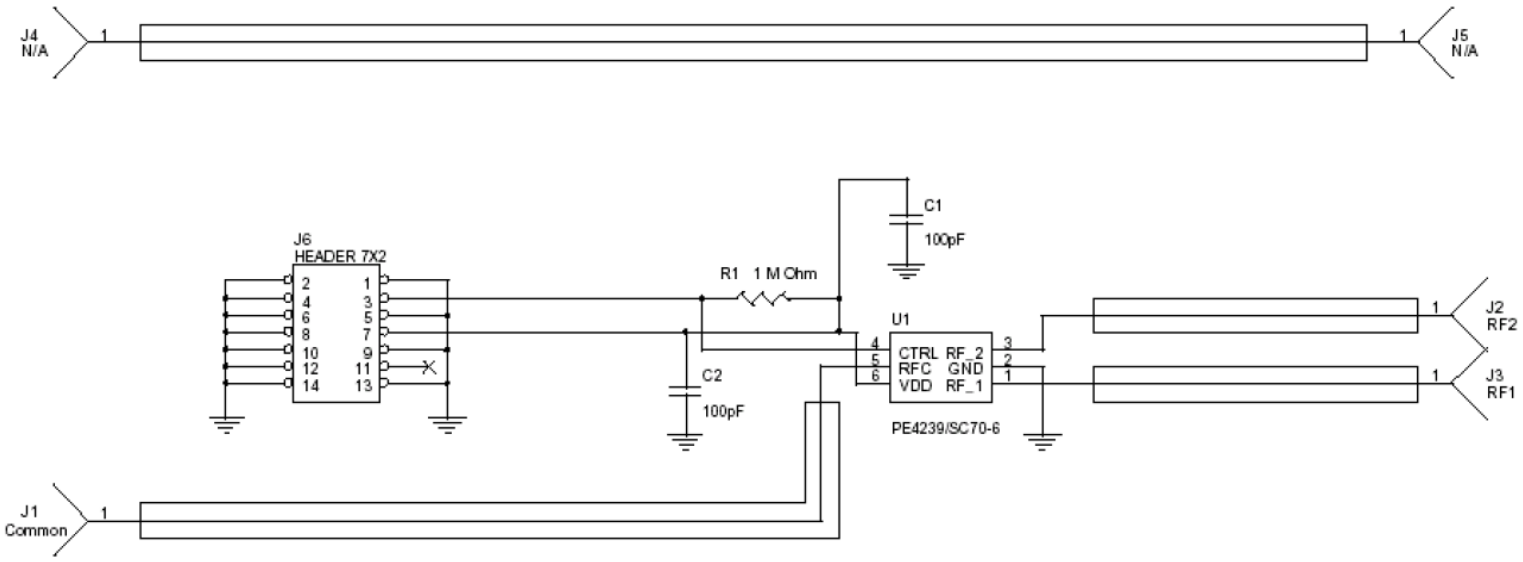



*Figure 9. Evaluation board schematic (pSemi specification 102/0104)*

# Pin configuration

Figure 10 shows the PE4239 pin configuration for the 6-lead SC-70 package, and Table 5 lists the description for each pin.

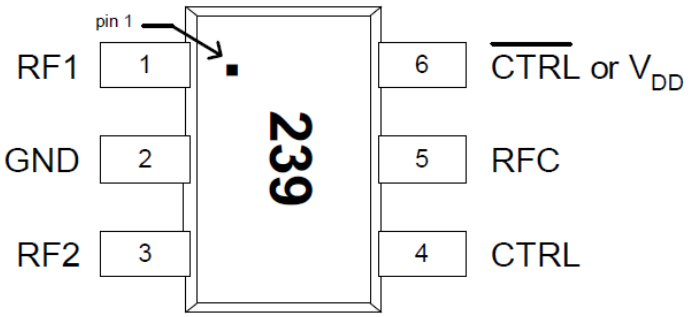



*Figure 10. Pin configuration, top view*

Table 5. Pin descriptions

| Pin no. | Pin name | Description |
|---|---|---|
| 1(*) | RF1 | RF port 1 |
| 2 | GND | Ground connection. Traces must be physically short and connected to ground plane for best performance. |
| 3(*) | RF2 | RF port 2 |
| 4 | CTRL | Switch control input, CMOS logic level. |
| 5(*) | RFC | RF common port |
| 6 | $\overline{CTRL}$ or $V_{DD}$ | This pin supports two interface options:<br>• *Single-pin control mode*: A nominal 3V supply connection is required.<br>• *Complementary-pin control mode*: A complementary CMOS control signal to CTRL is supplied to this pin. Bypassing on this pin is not required in this mode. |
| Note: * RF pins 1, 3, and 5 must be DC blocked with an external series capacitor or held at 0 VDC. | | |

# Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

## Moisture sensitivity level

The PE4239 moisture sensitivity level rating for the 6-lead SC-70 package is MSL3.

## Package drawing

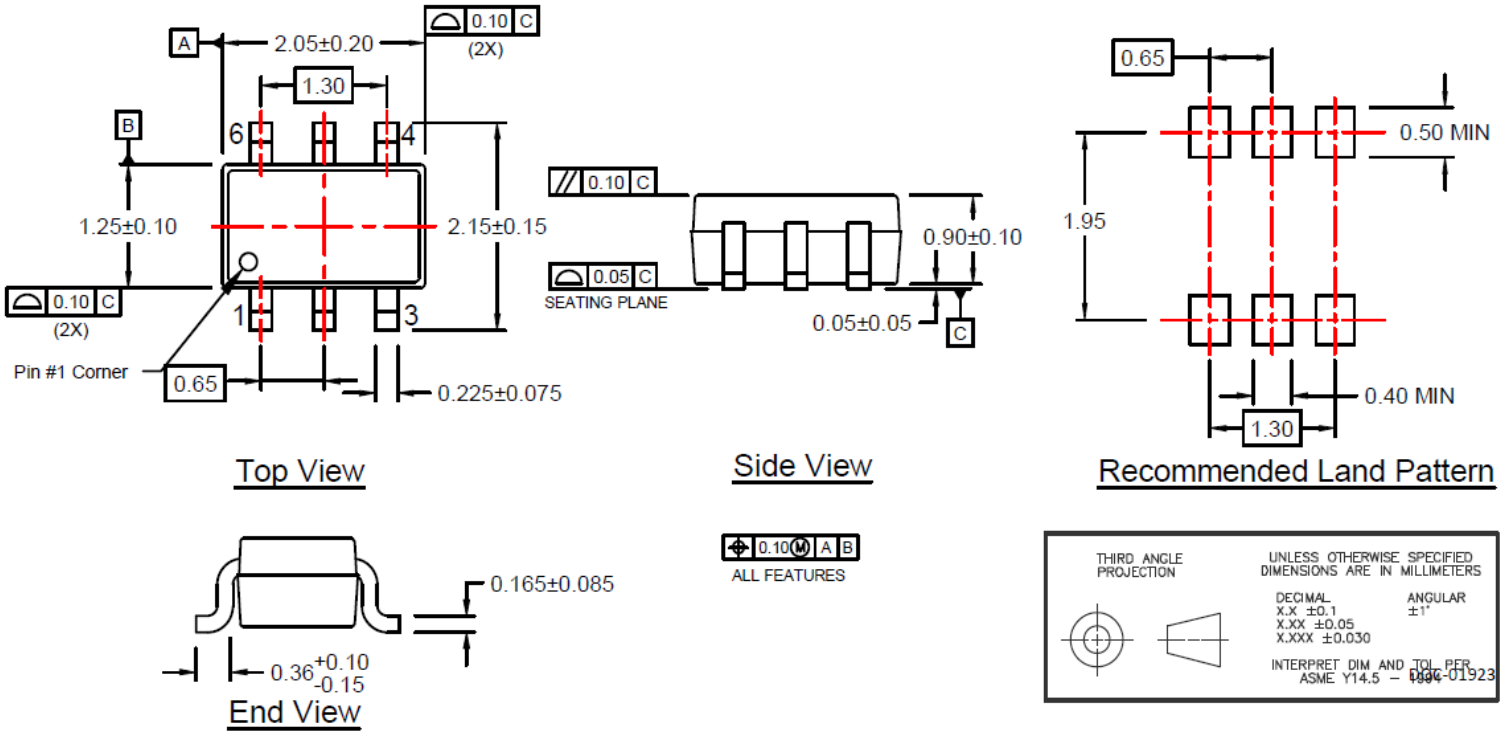



*Figure 11. Package mechanical drawing for the 6-lead SC-70 package*

## Package marking specification

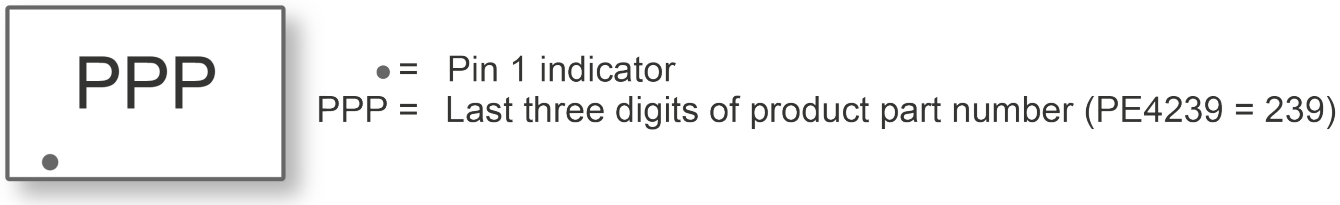



*Figure 12. Top-marking specification*

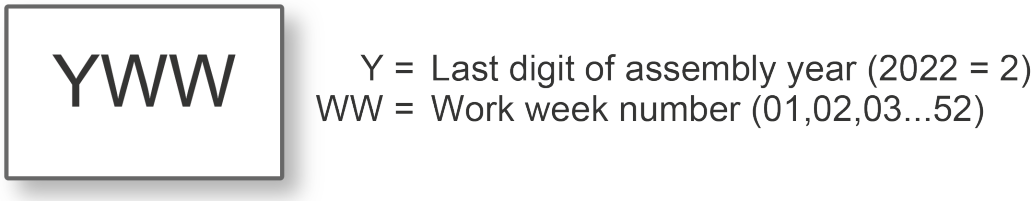
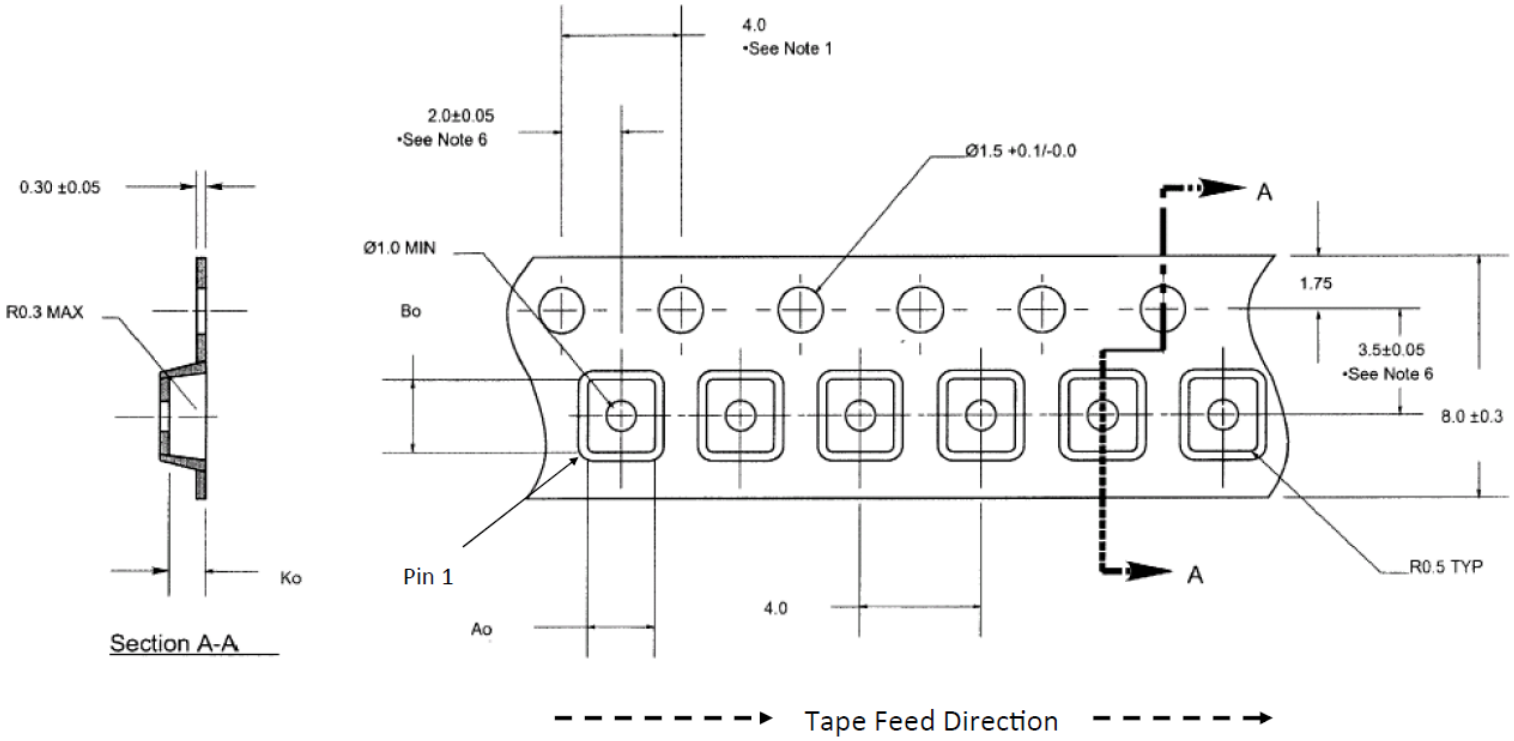



*Figure 13. Bottom-marking specification*

## Tape and reel specification




Notes:
1. 10 sprocket hole pitch cumulative tolerance ±.02.
2. Camber not to exceed 1mm in 100mm.
3. Material: Black Conductive Advantek Polystyrene.
4. Ao and Bo measured on a plane 0.3mm above the bottom of the pocket
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Ao = 2.25 mm
Bo = 2.4 mm
Ko = 1.2 mm

*Figure 14. Tape and reel specification for the 6-lead SC-70 package*

## Ordering information

| Order code | Description | Packaging | Shipping method |
|---|---|---|---|
| PE4239A-Z | PE4239 SPDT RF switch | Green 6-lead SC-70 | 3000 units/T&R |
| EK4239-01 | PE4239 evaluation kit | Evaluation kit | 1/box |

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