

PE42641

Product Specification

UltraCMOS® SP4T RF Switch, 100 MHz–3.0 GHz



Features

- Symmetric, high-power SP4T: All ports are WEDGE and CDMA compliant
- Low insertion loss:
 - 0.45 dB at 1000 MHz
 - 0.6 dB at 2000 MHz
- HaRP™ enhanced technology for unparalleled linearity
- Low harmonics:
 - $2f_0 = -86$ dBc at +35 dBm
 - $3f_0 = -81$ dBc at +35 dBm
- IMD3: -110 dBm at WCDMA Band I
- IIP3: +68 dBm
- Extremely high isolation:
 - 35 dB at 900 MHz
 - 29 dB at 1900 MHz
- Exceptionally high ESD tolerance:
 - Class 3 (4.0 kV HBM) on ANT pin
 - Class 2 (2.0 kV HBM) on all pins
- Integrated decoder for 2-pin control accepts 1.8V and 2.75V levels
- Low 4.5Ω series ON resistance
- No blocking capacitors required
- Packaging: 16-lead 3×3 mm QFN

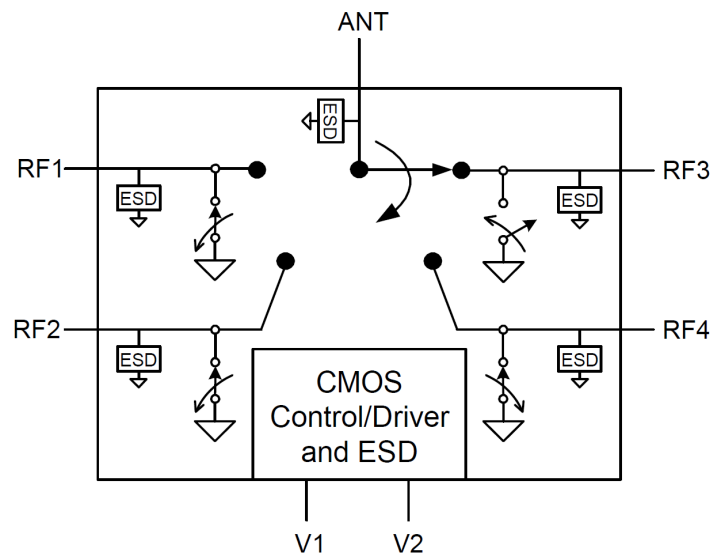


Figure 1. PE42641 functional diagram

Product description

The PE42641 is a HaRP-enhanced SP4T RF switch developed using pSemi UltraCMOS® process technology. This switch contains four identical WEDGE- and CDMA-compliant Tx paths and can be used in various GSM and WCDMA mobile applications and other wireless applications up to 3000 MHz. It is also suitable for antenna band switching and switchable matching networks for cellular and non-cellular mobile applications. It integrates on-board CMOS control logic with a low-voltage CMOS-compatible control interface and requires no DC blocking capacitors. This RoHS-compliant device is available in a standard $3 \times 3 \times 0.75$ mm QFN package.

pSemi HaRP technology enhancements deliver high linearity and exceptional harmonics performance. It is an innovative feature of the UltraCMOS process, providing performance superior to GaAs with the economy and integration of conventional CMOS.

Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. Absolute maximum ratings

Parameter or condition	Symbol	Min	Max	Unit
Power supply voltage	V _{DD}	-0.3	4.0	V
Voltage on any DC input	V _I	-0.3	V _{DD} + 0.3	V
Storage temperature range	T _{ST}	-65	+150	°C
RF input power (50Ω), 824–915 MHz ⁽¹⁾⁽²⁾	P _{IN} (50Ω)	–	+38	dBm
RF input power (50Ω), 1710–1910 MHz ⁽¹⁾⁽²⁾		–	+36	
RF input power (VSWR = ∞:1), 824–915 MHz ⁽¹⁾⁽²⁾	P _{IN} (∞:1)	–	+35	dBm
RF input power (VSWR = ∞:1), 1710–1910 MHz ⁽¹⁾⁽²⁾		–	+33	
ESD voltage, ANT pin ⁽³⁾	V _{ESD}	–	4000	V
ESD voltage, all pins ⁽³⁾		–	2000	
Notes: 1. Assumes an RF input period of 4620 μs and a duty cycle of 50%. 2. V _{DD} is within the operating range specified in Table 2 . 3. ESD voltage (HBM, MIL-STD-883 Method 3015.7).				

Recommended operating conditions

Table 2 lists the PE42641 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. Recommended operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Temperature range	T _{OP}	-40	–	+85	°C
Supply voltage	V _{DD}	2.65	2.75	2.85	V
Power supply current (V _{DD} = 2.75V)	I _{DD}	–	13	50	μA
RF input power (VSWR ≤ 3:1), 824–915 MHz ^(*)	P _{IN}	–	–	+35	dBm
RF input power (VSWR ≤ 3:1), 1710–1910 MHz ^(*)		–	–	+33	
Control voltage high	V _{IH}	1.4	–	–	V
Control voltage low	V _{IL}	–	–	0.4	V
Note: * Assumes a 4620-μs RF input period and a duty cycle of 50%.					

Electrical specifications

Table 3 lists the PE42641 key electrical specifications at +25 °C and $V_{DD} = 2.75V$ ($Z_S = Z_L = 50\Omega$), unless otherwise specified.

Table 3. Electrical specifications

Parameter	Condition	Min	Typ	Max	Unit
Operating frequency	–	10	–	3000	MHz
Insertion loss (symmetric ports) ^(*)	ANT–RF (850/900 MHz) ANT–RF (1800/1900 MHz) ANT–RF (1900/2200 MHz)	–	0.45 0.5 0.55	0.65 0.7 0.75	dB
Return loss (active ports)	850/900 MHz 1800/1900 MHz 1900/2100 MHz)	–	25 19 18	–	dB
Isolation	ANT–RF (850/900 MHz) ANT–RF (1800/1900 MHz) ANT–RF (1900/2200 MHz)	31 25 23.5	35 29 27.5	–	dB
Second harmonic	35 dBm output power, 850/900 MHz 33 dBm output power, 1800/1900 MHz	–	-86 -87	-80 -78	dBc
Third harmonic	35 dBm output power, 850/900 MHz 33 dBm output power, 1800/1900 MHz	–	-81 -80	-73.5 -72.5	dBc
IMD3 distortion	RF measured at 2.14 GHz at ANT port, input +20 dBm CW signal at 1.95 GHz, and -15 dBm CW signal at 1.76 GHz.	–	-110	–	dBm
Switching time	(10-90%) (90-10%) RF	–	2	5	µs

Note: * The typical ON resistance value at DC is 4.5Ω.

Electrical specifications, worst-case conditions

Table 4 lists the PE42641 worst-case electrical specifications at +85 °C and $V_{DD} = 2.65V$ ($Z_S = Z_L = 50\Omega$), unless otherwise specified.

Table 4. Electrical specifications, worst-case conditions

Parameter	Condition	Min	Typ	Max	Unit
Insertion loss	ANT–RF (850/900 MHz) ANT–RF (1800/1900 MHz) ANT–RF (1900/2200 MHz)	–	0.5 0.55 0.6	0.7 0.75 0.8	dB
Return loss (active ports)	850/900 MHz 1800/1900 MHz 1900/2100 MHz)	–	25 19 18	–	dB
Isolation	ANT–RF (850/900 MHz) ANT–RF (1800/1900 MHz) ANT–RF (1900/2200 MHz)	30.5 24.5 23	34.5 28.5 27	–	dB
Second harmonic	35 dBm output power, 850/900 MHz 33 dBm output power, 1800/1900 MHz	–	-84 -85	-78 -76	dBc
Third harmonic	35 dBm output power, 850/900 MHz 33 dBm output power, 1800/1900 MHz	–	-79 -78	-71.5 -70.5	dBc
IMD3 distortion	RF measured at 2.14 GHz at ANT port, input +20 dBm CW signal at 1.95 GHz, and -15 dBm CW signal at 1.76 GHz.	–	-108	–	dBm
Switching time	(10-90%) (90-10%) RF	–	2	5	μs

Control logic

Table 5. Truth table

Path	V2	V1
ANT–RF1	0	0
ANT–RF2	1	0
ANT–RF3	0	1
ANT–RF4	1	1

Typical performance data

Figures 2–7 show the typical performance data, as indicated.

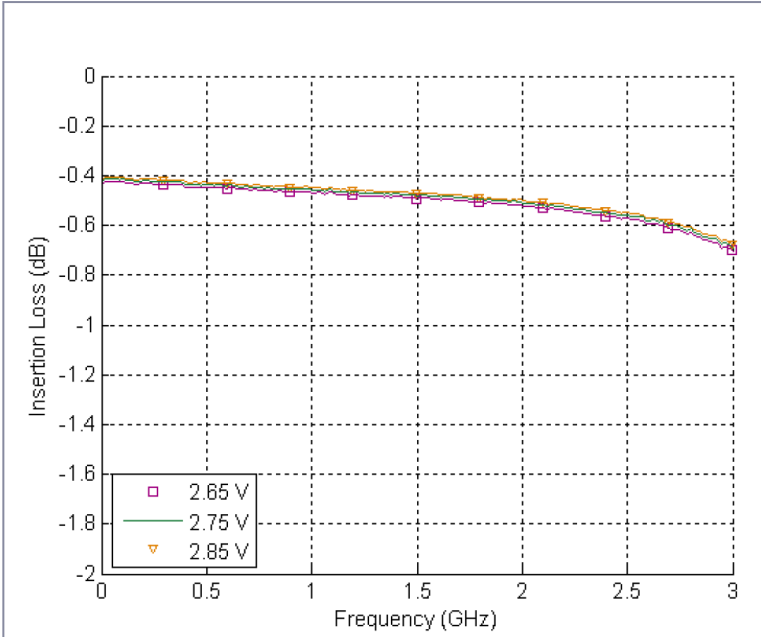


Figure 2. Insertion loss: ANT–RF at 25 °C

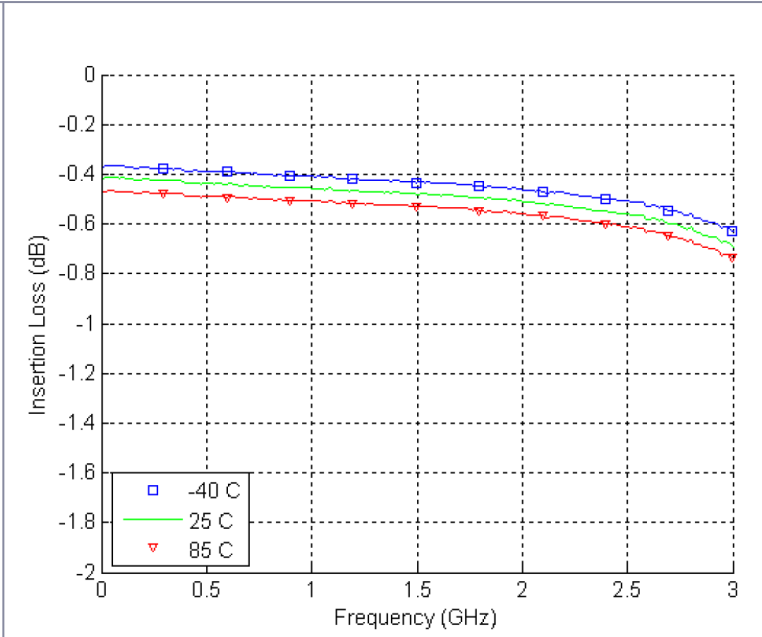


Figure 3. Insertion loss: ANT–RF at 2.75V

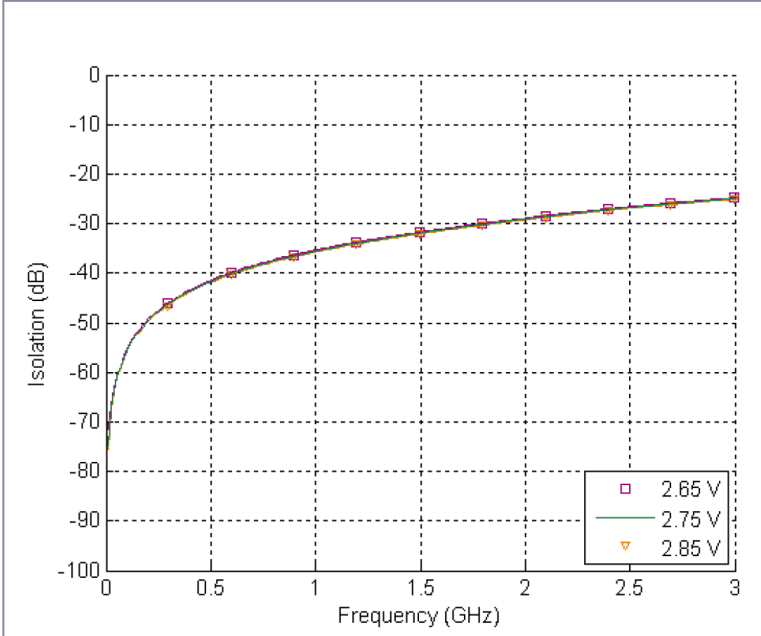


Figure 4. Isolation: ANT–RF at 25 °C

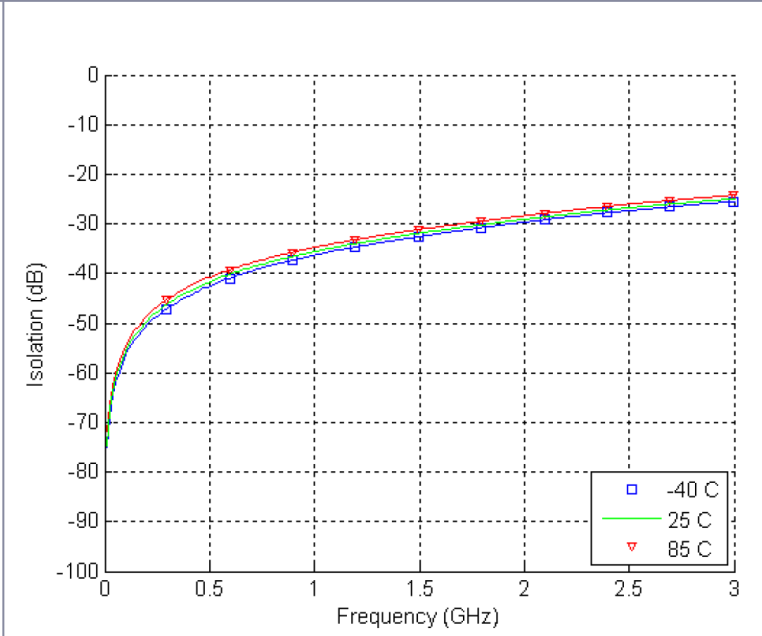


Figure 5. Isolation: ANT–RF at 2.75V

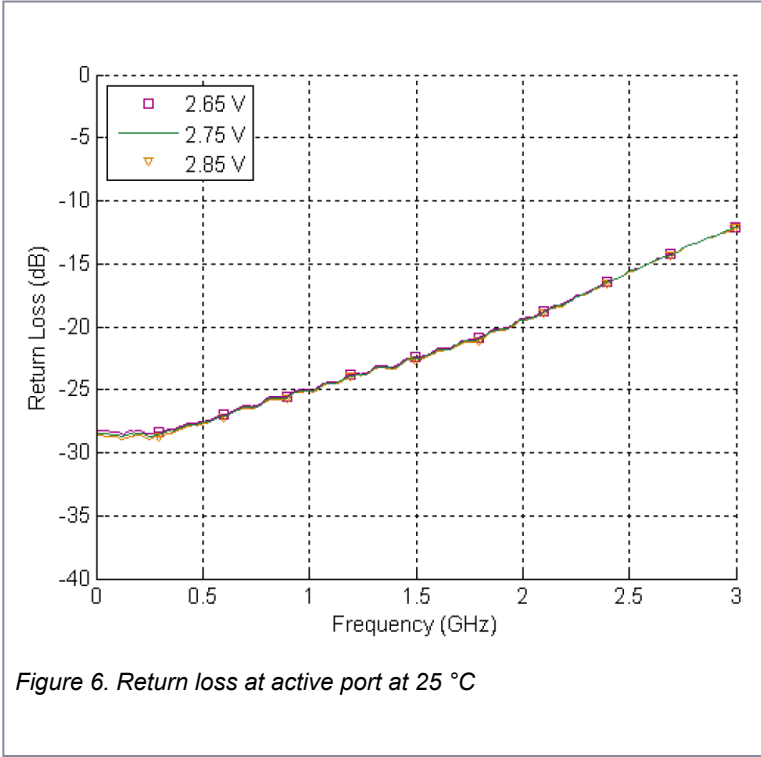


Figure 6. Return loss at active port at 25 °C

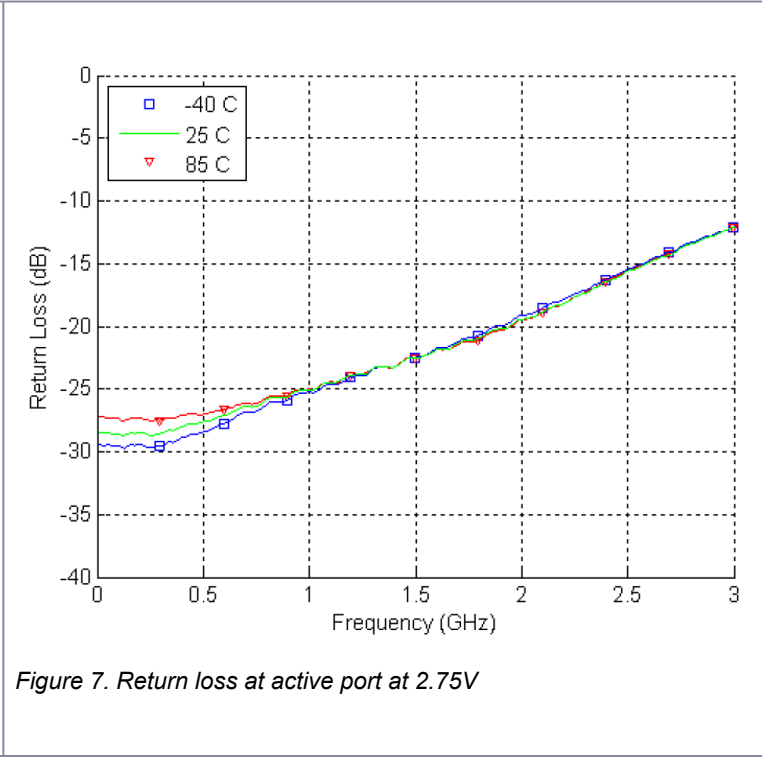


Figure 7. Return loss at active port at 2.75V

Evaluation board

pSemi designed the SP4T switch evaluation board to ease your evaluation of the pSemi PE42641. The RF common port connects through a 50 Ω transmission line via the top SMA connector, J1. Ports RF1, RF2, RF3, and RF4 connect through 50 Ω transmission lines via SMA connectors J3, J5, J2, and J4, respectively. A through 50 Ω transmission line is available via SMA connectors J6 and J7 to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a four metal layer FR4 material with a total thickness of 62 mils. The middle layers provide ground for the transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 32 mils, trace gaps of 25 mils, and metal thickness of 2.1 mils.

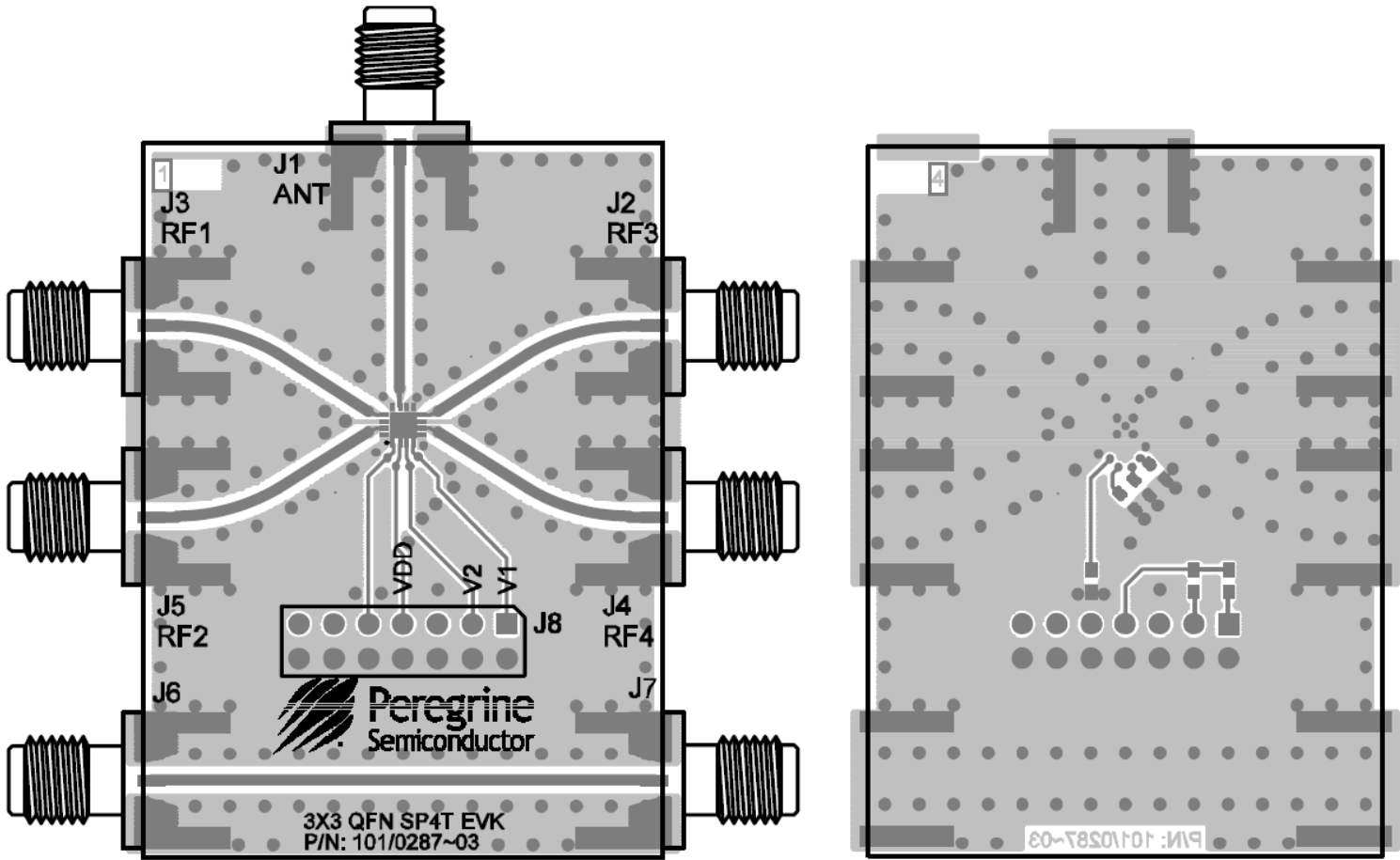


Figure 8. Evaluation board layout, pSemi specification 101/0287

Evaluation board schematic

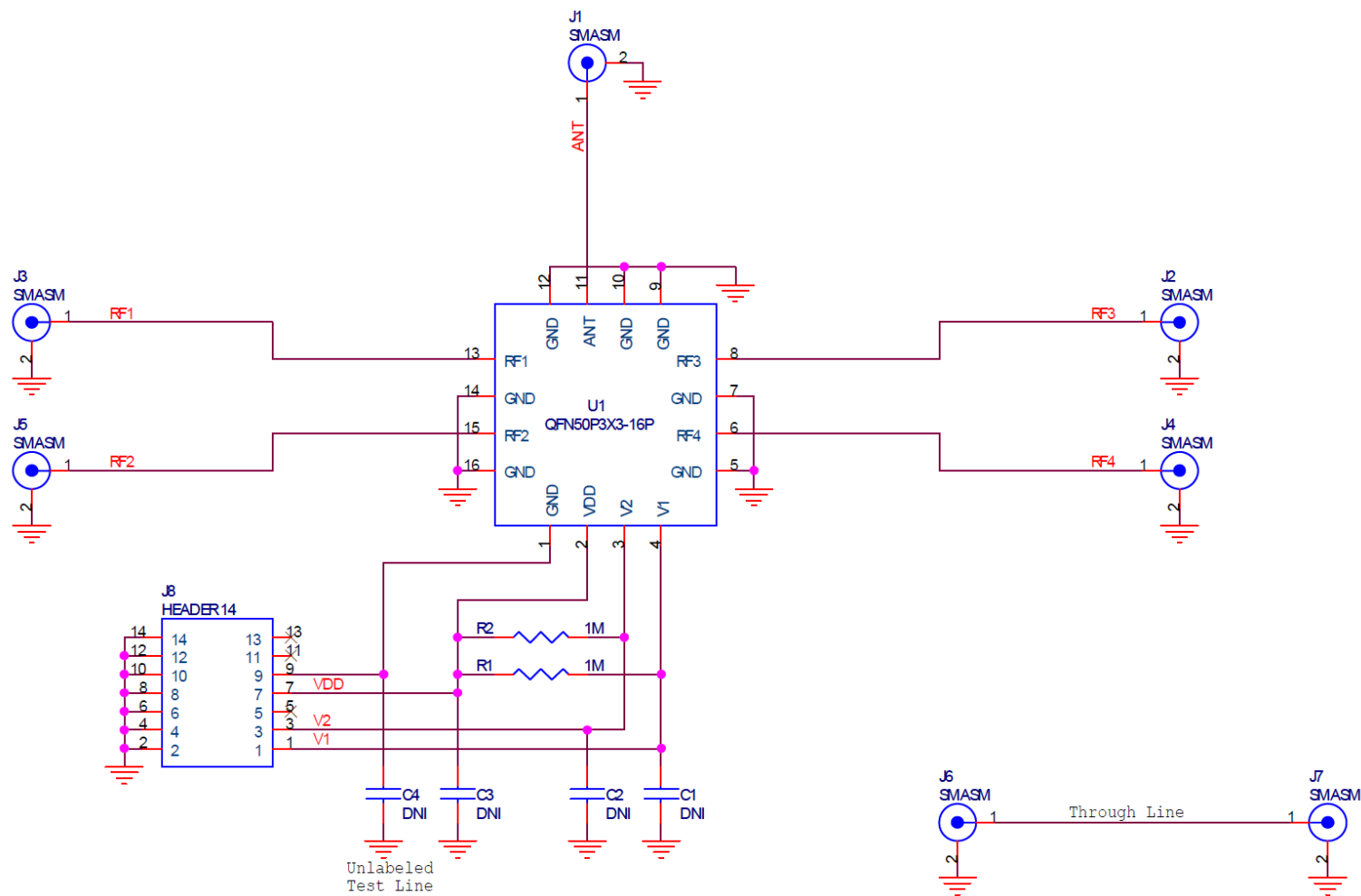


Figure 9. Evaluation board schematic, pSemi specification 102/0339

Pin configuration

Figure 10 shows the pin configuration for the 16-lead 3 × 3 mm QFN package, and Table 6 lists the description for each pin.

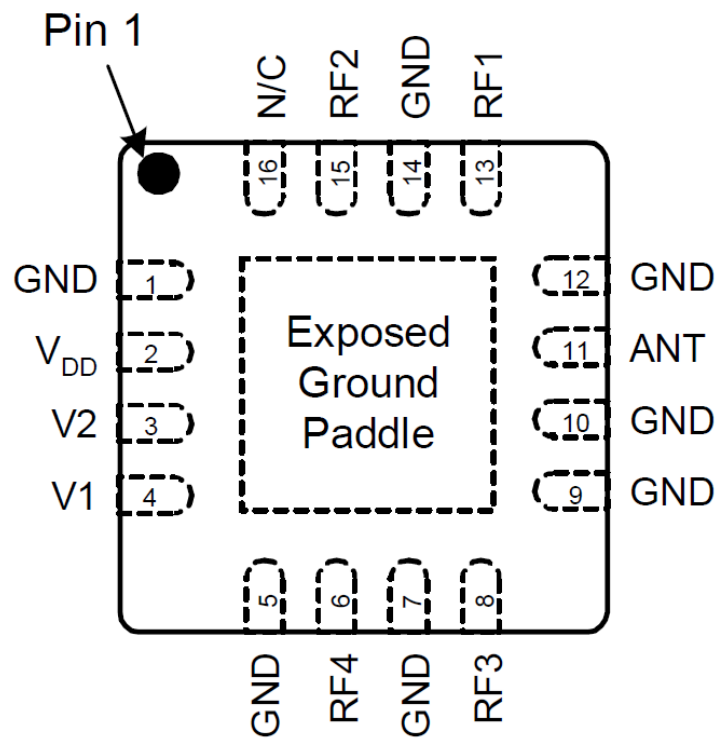


Figure 10. Pin configuration, top view

Table 6. Pin descriptions

Pin no.	Pin name	Description
1, 5, 7, 9, 10, 12, 14	GND	Ground
2	V _{DD}	Supply voltage
3	V2	Switch control input, CMOS logic level
4	V1	Switch control input, CMOS logic level
6(*)	RF4	RF port 4
8(*)	RF3	RF port 3
11(*)	ANT	RF common: Antenna
13(*)	RF1	RF port 1
15(*)	RF2	RF port 2
16	N/C	No connect
Pad	GND	Exposed pad. Ground for proper operation.

Note: * Blocking capacitors are only needed when non-zero DC voltage is present.

Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
 - Package drawing
- Package marking
 - Tape-and-reel information

Moisture sensitivity level

The PE42641 moisture sensitivity level rating for the 16-lead 3 × 3 mm QFN package is MSL1.

Package drawing

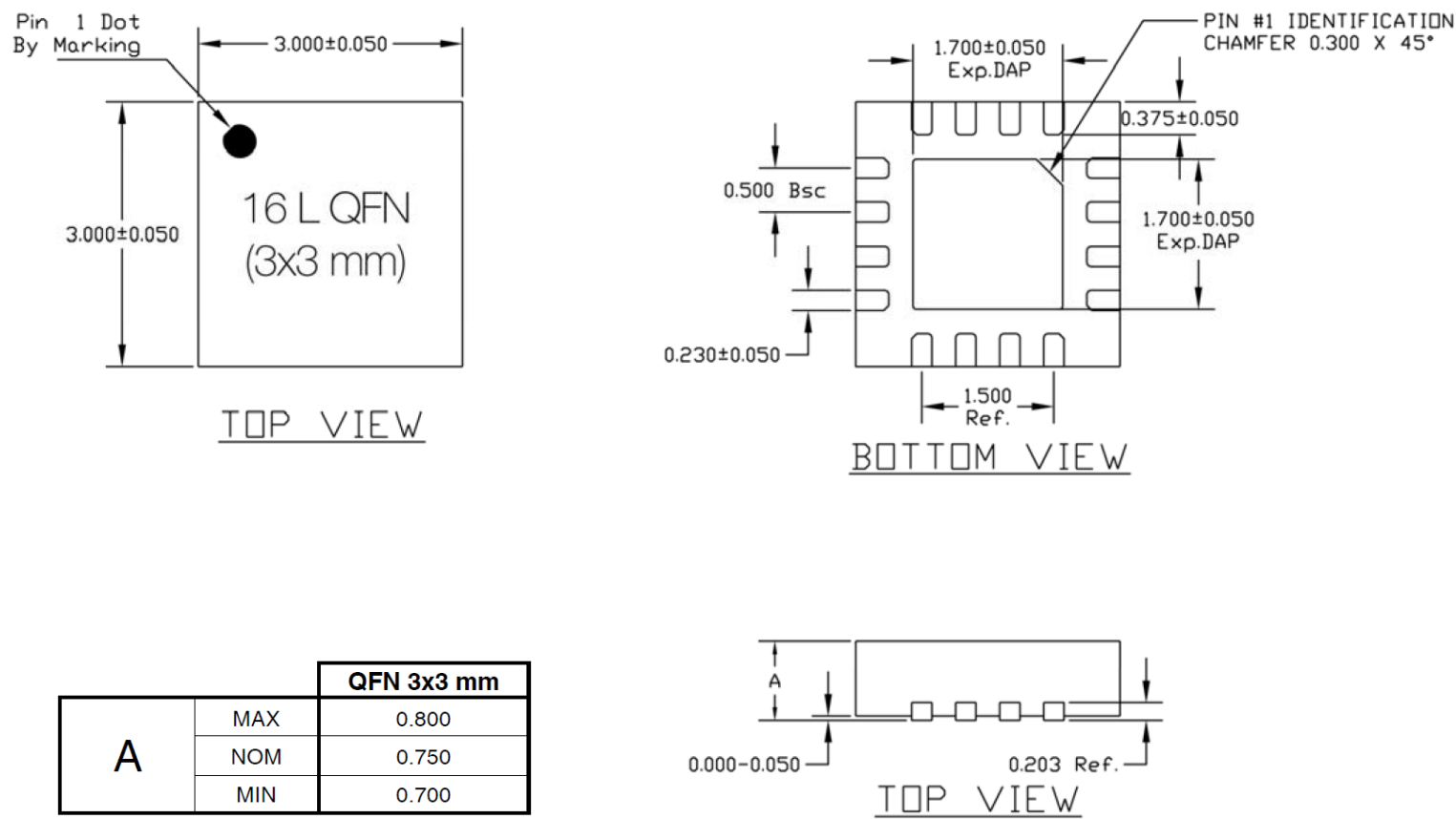
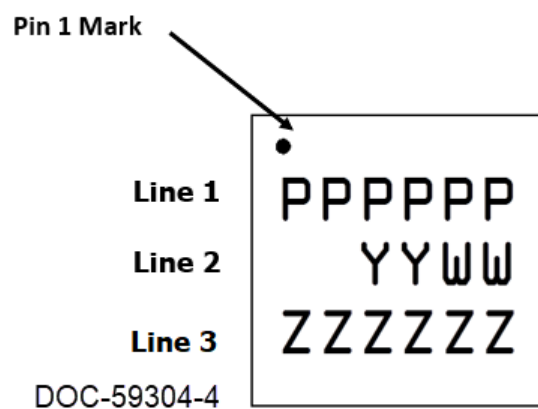


Figure 11. Package mechanical drawing for the 16-lead 3 × 3 mm QFN package

Top-marking specification



- P P P P P P = The part number (42641)
- Y Y = Assembly year last two digits
- W W = Assembly lot work week
- Z Z Z Z Z Z = Assembly lot code

Figure 12. Package marking specification

Tape and reel specification

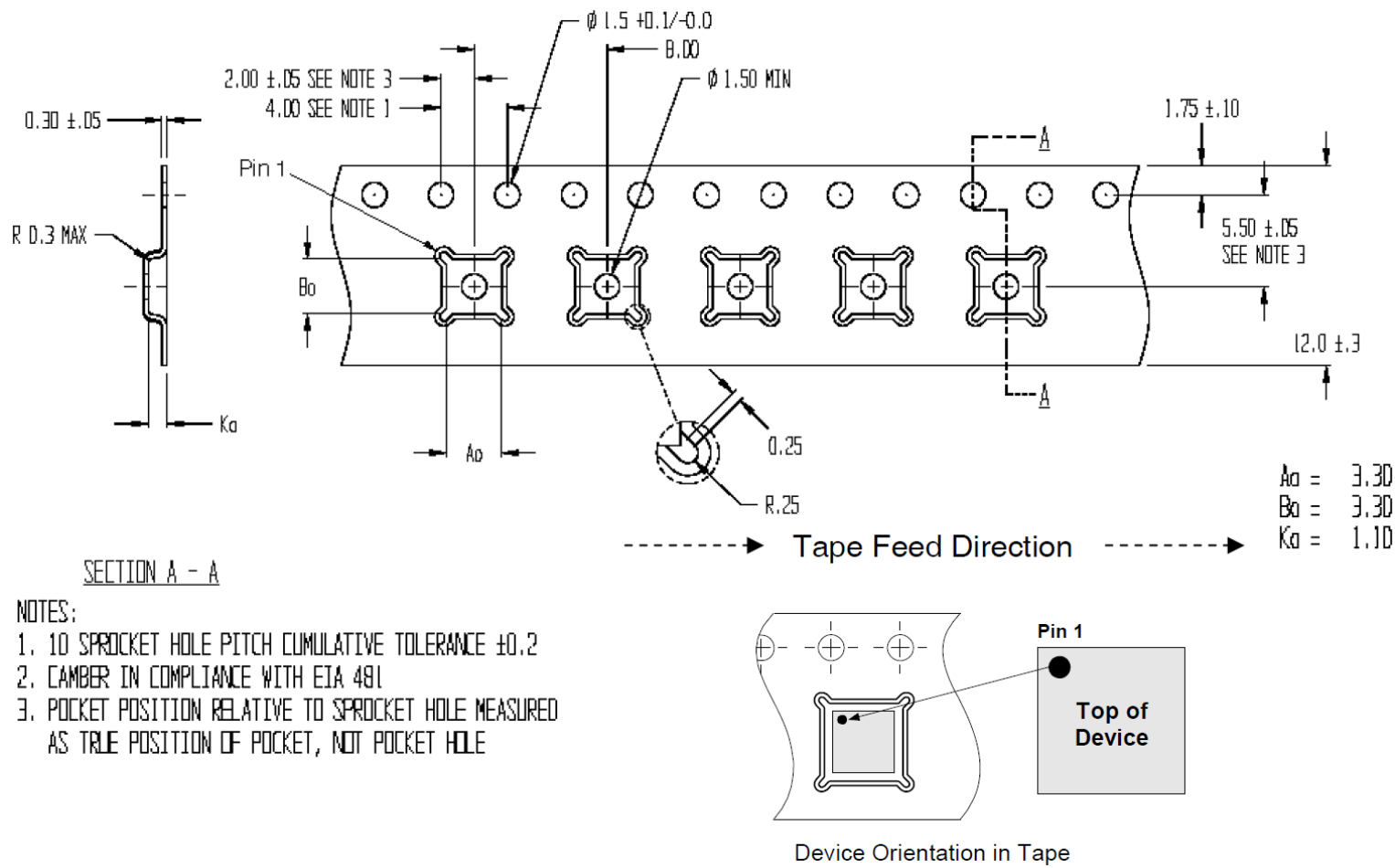
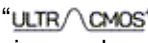


Figure 13. Tape and reel specification for the 16-lead 3 × 3 mm QFN package

Ordering information

Order code	Description	Packaging	Shipping method
PE42641MLBD-Z	PE42641 SP4T RF switch	Green 16-lead 3 × 3 mm QFN	3000 units/T&R
EK42641-04	PE42641 evaluation kit	Evaluation kit	1/box

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Sales contact

For more information, contact Sales at sales@psemi.com.