8-BIT MICROCONTROLLER

Table of Contents-

1. GENERAL DESCRIPTION 4
2. FEATURES 5
3. PARTS INFORMATION LIST 6
   3.1 Lead Free (RoHS) Parts information list 6
4. PIN CONFIGURATIONS 7
5. PIN DESCRIPTIONS 9
6. FUNCTIONAL DESCRIPTION 11
   6.1 On-Chip Flash EPROM 11
   6.2 I/O Ports 11
   6.3 Serial I/O 11
   6.4 Timers 11
   6.5 Interrupts 11
   6.6 Data Pointers 11
   6.7 Architecture 11
   6.8 Power Management 12
7. MEMORY ORGANIZATION 13
   7.1 Program Memory (on-chip Flash) 13
   7.2 Data Memory 14
   7.3 Scratch-pad RAM and Register Map 14
8. SPECIAL FUNCTION REGISTERS 17
   8.1 SFR Location Table 17
   8.2 SFR Detail Bit Descriptions 21
9. INSTRUCTION 51
   9.1 Instruction Timing 58
   9.2 MOVX Instruction 62
   9.3 External Data Memory Access Timing 63
   9.4 Wait State Control Signal 66
10. POWER MANAGEMENT 67
   10.1 Idle Mode 67
   10.2 Economy Mode 67
   10.3 Power Down Mode 68

11. RESET CONDITIONS 69
11.1 Sources of reset 69
11.2 Reset State 69
12. PROGRAMMABLE TIMERS/COUNTERS 71
12.1 Timer/Counters 0 & 1 71
12.2 Time-base Selection 71
12.3 Timer/Counter 2 74
13. NVM MEMORY 78
13.1 Operation 78
14. WATCHDOG TIMER 80
15. UART SERIAL PORT 82
15.1 Mode 0 82
15.2 Mode 1 83
15.3 Mode 2 84
15.4 Mode 3 87
15.5 Framing Error Detection 88
15.6 Multiprocessor Communications 88
16. I2C SERIAL PORT 90
16.1 I2C Bus 90
16.2 The I2C Control Registers: 91
16.3 Modes of Operation 93
16.4 Data Transfer Flow in Five Operating Modes 94
17. TIMED ACCESS PROTECTION 100
18. INTERRUPTS 102
18.1 Interrupt Sources 102
18.2 Priority Level Structure 103
18.3 Interrupt Response Time 105
18.4 Interrupt Inputs 105
19. KEYBOARD FUNCTION 106
20. INPUT CAPTURE 108
21. PULSE WIDTH MODULATED OUTPUTS (PWM) 110
22. I/O PORT 111
22.1 Quasi-Bidirectional Output Configuration 111
22.2 Open Drain Output Configuration 112
22.3 Push-Pull Output Configuration 113
22.4 Input Only Mode 113

23. OSCILLATOR 115
23.1 On-Chip RC Oscillator Option 115
23.2 External Clock Input Option 115
23.3 CPU Clock Rate select 116
24. POWER MONITORING 117
24.1 Power On Detect 117
24.2 Brownout Detect and Reset 117
25. ICP(IN-CIRCUIT PROGRAM) FLASH PROGRAM 119
26. CONFIG BITS 120
26.1 CONFIG0 120
26.2 CONFIG1 121
27. ELECTRICAL CHARACTERISTICS 123
27.1 Absolute Maximum Ratings 123
27.2 D.C. Characteristics 124
27.3 A.C. Characteristics 125
27.4 RC OSC AND AC CHARACTERISTICS 130
27.5 Typical Application Circuit 130
28. PACKAGE DIMENSIONS 131
28.1 40-pin DIP 131
28.2 44-pin PLCC 132
28.3 44-pin PQFP 133
28.4 48-pin LQFP 134
29. REVISION HISTORY 135

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1. GENERAL DESCRIPTION

The N79E352(R) is an 8-bit Turbo 51 microcontroller which has Flash EPROM programmable hardware writer. The instruction set of the N79E352(R) is fully compatible with the standard 8052. The N79E352(R) contains a 8Kbytes of main Flash EPROM; a 256 bytes of RAM; 128 bytes NVM Data Flash EPROM; three 16-bit timer/counters; 2-channel 8-bit PWM; 1-channel UART and 1 additional input capture. These peripherals are supported by 11 interrupt sources four-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the N79E352(R) allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security. N79E352(R) is designed for cost effective applications which can serve industrial devices, and other low power applications.

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2. FEATURES

- Fully static design 8-bit Turbo 51 CMOS microcontroller up to 24MHz when VDD=4.5V to 5.5V, 12MHz when VDD=2.7V to 5.5V, and 4MHz when VDD=2.4V to 5.5V.
- 8K bytes of AP Flash EPROM, with external writer programmable mode.
- 256 bytes of on-chip RAM.
- 128 bytes NVM Data Flash EPROM for customer data storage used and 10k writer cycles.
- Instruction-set compatible with MCS-51.
- On-chip configurable RC oscillator: 22.1184MHz/11.0592MHz (selectable by config bit) with ±2% accuracy, at 5V voltage and 25°C condition. (±2% accuracy is only for N79E352R.)
- Three 16-bit timer/counters.
- One input capture.
- 11 interrupt source with four levels of priority.
- One enhanced full duplex serial port with framing error detection and automatic address recognition.
- 4 outputs mode and TTL/Schmitt trigger selectable Port.
- Programmable Watchdog Timer with 20KHz internal RC clock can wake-up the power down mode, and have very low power under 10uA at 5V.
- Two-channel 8-bit PWM.
- One I2C communication port.
- Dual 16-bit Data Pointers.
- Software programmable access cycle to external RAM/peripherals.
- Eight keypads interrupt inputs with sharing the same interrupt source.
- LED drive capability (20mA) on all port pins, total 100mA.
- Low Voltage (3 levels) Detection interrupt and reset.
- Industrial temperature grade -40°C~85°C.
- Packages:
  - ■Lead Free (RoHS) DIP40: N79E352RADG
  - ■Lead Free (RoHS) PLCC44: N79E352RAPG
  - ■Lead Free (RoHS) PQFP44: N79E352RAFG
  - ■Lead Free (RoHS) LQFP48: N79E352RALG
  - ■Lead Free (RoHS) DIP40: N79E352ADG
  - ■Lead Free (RoHS) PLCC44: N79E352APG
  - ■Lead Free (RoHS) PQFP44: N79E352AFG
  - ■Lead Free (RoHS) LQFP48: N79E352ALG
  - -

3. PARTS INFORMATION LIST

3.1 Lead Free (RoHS) Parts information list

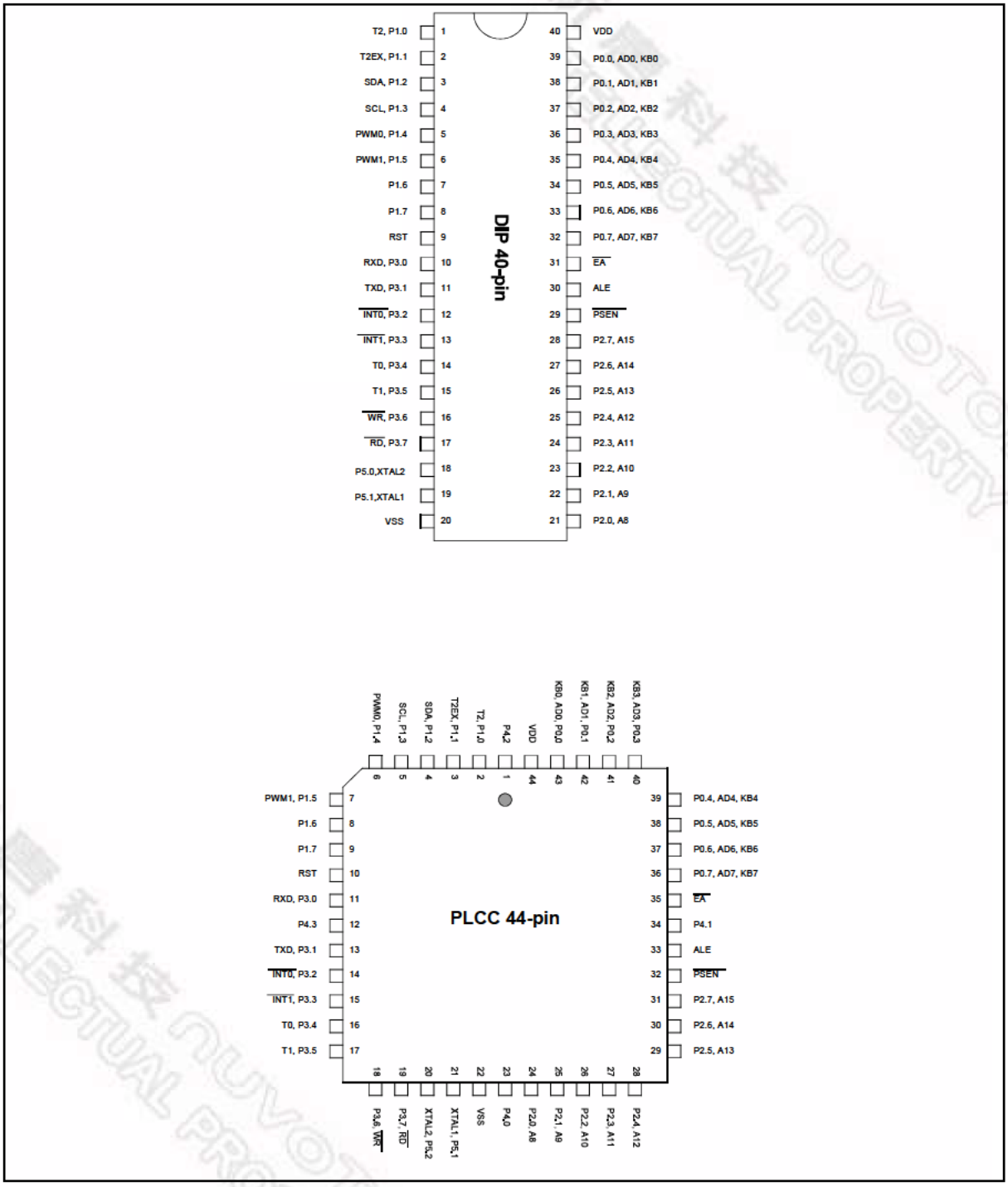
PART NO.	EPROM FLASH SIZE	RAM	NVM FLASH EPROM	INTERNAL RC OSCILLATOR ACCURACY[1]	PACKAGE
N79E352RADG	8KB	256B	128B	22.1184MHz ± 2%	DIP-40 Pin
N79E352RAPG	8KB	256B	128B	22.1184MHz ± 2%	PLCC-44 Pin
N79E352RAFG	8KB	256B	128B	22.1184MHz ± 2%	PQFP-44 Pin
N79E352RALG	8KB	256B	128B	22.1184MHz ± 2%	LQFP-48 Pin
N79E352ADG	8KB	256B	128B	22MHz ± 25%	DIP-40 Pin
N79E352APG	8KB	256B	128B	22MHz ± 25%	PLCC-44 Pin
N79E352AFG	8KB	256B	128B	22MHz ± 25%	PQFP-44 Pin
N79E352ALG	8KB	256B	128B	22MHz ± 25%	LQFP-48 Pin

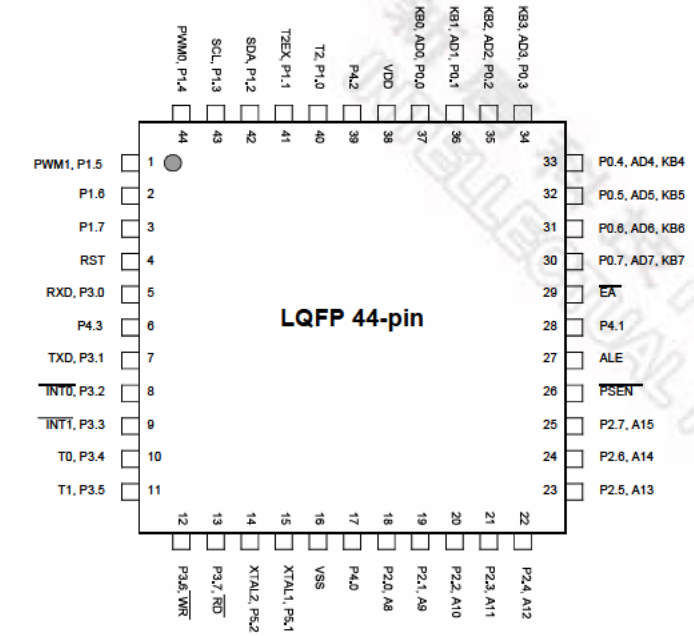
Table 3-1: Lead Free (RoHS) Parts information list

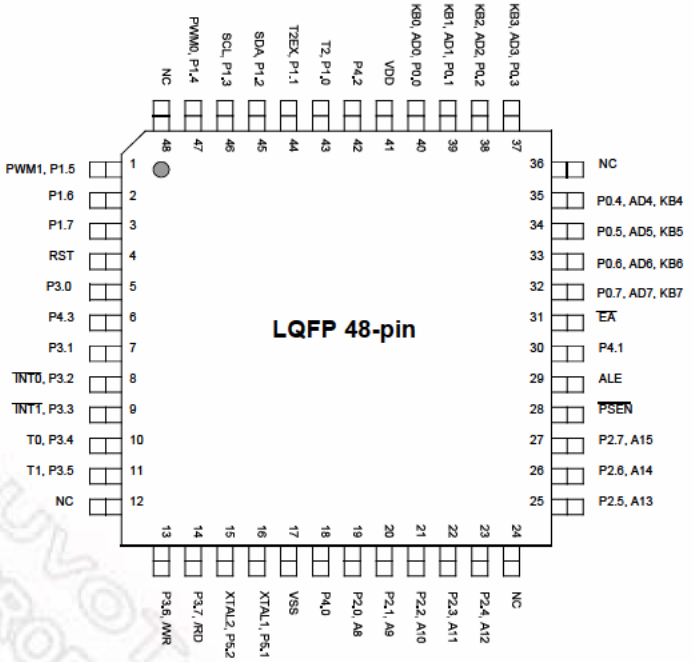
Note:

1. Factory calibration condition: V_{DD}=5.0V±10%, TA = 25°C

4. PIN CONFIGURATIONS




LQFP 44-pin
1 PWM1, P1.5
2 P1.6
3 P1.7
4 RST
5 RXD, P3.0
6 P4.3
7 TXD, P3.1
8 INT0, P3.2
9 INT1, P3.3
10 T0, P3.4
11 T1, P3.5
12 P3.6, WR
13 P3.7, RD
14 XTAL2, P5.2
15 XTAL1, P5.1
16 VSS
17 P4.0
18 P2.0, A8
19 P2.1, A9
20 P2.2, A10
21 P2.3, A11
22 P2.4, A12
23 P2.5, A13
24 P2.6, A14
25 P2.7, A15
26 PSEN
27 ALE
28 P4.1
29 EA
30 P0.7, AD7, KB7
31 P0.6, AD6, KB6
32 P0.5, AD5, KB5
33 P0.4, AD4, KB4
34 KB3, AD3, P0.3
35 KB2, AD2, P0.2
36 KB1, AD1, P0.1
37 KB0, AD0, P0.0
38 VDD
39 P4.2
40 T2, P1.0
41 T2EX, P1.1
42 SDA, P1.2
43 SCL, P1.3
44 PWM0, P1.4


LQFP 48-pin
1 PWM1, P1.5
2 P1.6
3 P1.7
4 RST
5 P3.0
6 P4.3
7 P3.1
8 INT0, P3.2
9 INT1, P3.3
10 T0, P3.4
11 T1, P3.5
12 NC
13 P3.6, WR
14 P3.7, RD
15 XTAL2, P5.2
16 XTAL1, P5.1
17 VSS
18 P4.0
19 P2.0, A8
20 P2.1, A9
21 P2.2, A10
22 P2.3, A11
23 P2.4, A12
24 NC
25 P2.5, A13
26 P2.6, A14
27 P2.7, A15
28 PSEN
29 ALE
30 P4.1
31 EA
32 P0.7, AD7, KB7
33 P0.6, AD6, KB6
34 P0.5, AD5, KB5
35 P0.4, AD4, KB4
36 NC
37 KB3, AD3, P0.3
38 KB2, AD2, P0.2
39 KB1, AD1, P0.1
40 KB0, AD0, P0.0
41 VDD
42 P4.2
43 T2, P1.0
44 T2EX, P1.1
45 SDA, P1.2
46 SCL, P1.3
47 PWM0, P1.4
48 NC

5. PIN DESCRIPTIONS

SYMBOL	Alternate Function 1	Alternate function 2	Type	DESCRIPTIONS
$\overline{EA}$			I	**EXTERNAL ACCESS ENABLE**: This pin forces the processor to execute out of external ROM. It should be kept high to access internal ROM. The ROM address and data will not be present on the bus if $\overline{EA}$ pin is high and the program counter is within internal ROM area. Otherwise they will be present on the bus.
$\overline{PSEN}$			O	**PROGRAM STORE ENABLE**: $\overline{PSEN}$ enables the external ROM data onto the Port 0 address/data bus during fetch and MOVC operations. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs from this pin.
ALE			O	**ADDRESS LATCH ENABLE**: ALE is used to enable the address latch that separates the address from the data on Port 0.
XTAL1	P5.1		I/O	**CRYSTAL1**: This is the crystal oscillator input. This pin may be driven by an external clock or configurable i/o pin, P5.1.
XTAL2	P5.0		I/O	**CRYSTAL2**: This is the crystal oscillator output. It is the inversion of XTAL1. Also a configurable i/o pin, P5.0.
VDD			P	**POWER SUPPLY**: Supply voltage for operation.
VSS			P	**GROUND**: Ground potential.
RST				**RESET:** A high on this pin for two machine cycles while the oscillator is running resets the device.
P0.0	KB0	AD0	I/O	**PORT0:** Support 4 mode output and 2 mode input. Multifunction pins for AD0-7and KB0-7.
P0.1	KB1	AD1	I/O	
P0.2	KB2	AD2	I/O	
P0.3	KB3	AD3	I/O	
P0.4	KB4	AD4	I/O	
P0.5	KB5	AD5	I/O	
P0.6	KB6	AD6	I/O	
P0.7	KB7	AD7	I/O	
P1.0		T2	I/O	**PORT1:** Support 4 mode output and 2 mode input. Multifunction pins for SDA & SCL (I2C), T2, T2EX and PWM0-1.
P1.1		T2EX	I/O	
P1.2		SDA	I/O	
P1.3		SCL	I/O	
P1.4		PWM0	I/O	
P1.5		PWM1	I/O	
P1.6	ICPDAT		I/O	
P1.7	ICPCLK		I/O	

P2.0		A8	I/O	**PORT2:** Support 4 mode output and 2 mode input. Multifunction pins for A8-A15,.
P2.1		A9	I/O	
P2.2		A10	I/O	
P2.3		A11	I/O	
P2.4		A12	I/O	
P2.5		A13	I/O	
P2.6		A14	I/O	
P2.7		A15	I/O	
P3.0		RXD	I/O	**PORT3:** Support 4 mode output and 2 mode input. Multifunction pins for RXD & TXD (uart), /INT0, /INT1, T0, T1, /WR and /RD.
P3.1		TXD	I/O	
P3.2		/INT0	I/O	
P3.3		/INT1	I/O	
P3.4		T0	I/O	
P3.5		T1	I/O	
P3.6		/WR	I/O	
P3.7		/RD	I/O	
P4.0			I/O	**PORT4:** Quasi output with internal pull up.
P4.1			I/O	
P4.2			I/O	
P4.3			I/O	

* Note: TYPE I: input, O: output, I/O: bi-directional.

In application if any pins need external pull-up, it is recommended to add a pull-up resistor (10kΩ) between pin and power (V_{DD}) instead of directly wiring pin to V_{DD} for enhancing EMC.

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6. FUNCTIONAL DESCRIPTION

N79E352(R) architecture consist of a 4T 8051 core controller surrounded by various registers, 8K bytes Flash EPROM, 256 bytes of RAM, 128 bytes NVM Data Flash EPROM; three timer/counters, one UART serial port, one I2C serial port, eight keyboard interrupt input, 2-channel PWM with 8-bit counter and Flash EPROM program by Writer.

6.1 On-Chip Flash EPROM

N79E352(R) includes one 8K bytes of main Flash EPROM for application program which need Writer to program the Flash EPROM.

6.2 I/O Ports

N79E352(R) has four 8-bit, one 4-bit port and one 2-bit port, with at least 36 I/O pins. All ports (except port 4) can be used as four outputs mode when it may set by PxM1.y and PxM2.y registers, it has strong pull-ups and pull-downs, and does not need any external pull-ups. Otherwise it can be used as general I/O port as open drain circuit. All ports can be used bi-directional and these are as I/O ports. These ports are not true I/O, but rather are pseudo-I/O ports. This is because these ports have strong pull-downs and weak pull-ups.

6.3 Serial I/O

N79E352(R) has one UART serial port that is functionally similar to the serial port of the original 8052 family. However the serial port on N79E352(R) can operate in different modes in order to obtain timing similarity as well. The Serial port has the enhanced features of Automatic Address recognition and Frame Error detection.

6.4 Timers

The device has total three 16-bit timers; two 16-bit timers that have functions similar to the timers of the 8052 family, and third timer is capable to function as timer and also provide capture support. When used as timers, user has a choice to set 12 or 4 clocks per count that emulates the timing of the original 8052. Each timer's count value is stored in two SFR locations that can be written or read by software. There are also some other SFRs associated with the timers that control their mode and operation.

6.5 Interrupts

The Interrupt structure in N79E352(R) is slightly different from that of the standard 8052. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased.

6.6 Data Pointers

The original 8052 had only one 16-bit Data Pointer (DPL, DPH). In the N79E352(R), there is an additional 16-bit Data Pointer (DPL1, DPH1). This new Data Pointer uses two SFR locations which were unused in the original 8052. In addition there is an added instruction, DEC DPTR (op-code A5H), which helps in improving programming flexibility for the user.

6.7 Architecture

N79E352(R) is based on the standard 8052 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard 8052 instruction set.

6.7.1 ALU

The ALU is the heart of the N79E352(R). It is responsible for the arithmetic and logical functions. It is also used in decision making, in case of jump instructions, and is also used in calculating jump addresses. The user cannot directly use the ALU, but the Instruction Decoder reads the op-code, decodes it, and sequences the data through the ALU and its associated registers to generate the required result. The ALU mainly uses the ACC which is a special function register (SFR) on the chip. Another SFR, namely B register is also used in Multiply and Divide instructions. The ALU generates several status signals which are stored in the Program Status Word register (PSW).

6.7.2 Accumulator

The Accumulator (ACC) is the primary register used in arithmetic, logical and data transfer operations in N79E352(R). Since the Accumulator is directly accessible by the CPU, most of the high speed instructions make use of the ACC as one argument.

6.7.3 B Register

This is an 8-bit register that is used as the second argument in the MUL and DIV instructions. For all other instructions it can be used simply as a general purpose register.

6.7.4 Program Status Word:

This is an 8-bit SFR that is used to store the status bits of the ALU. It holds the Carry flag, the Auxiliary Carry flag, General purpose flags, the Register Bank Select, the Overflow flag, and the Parity flag.

6.7.5 Scratch-pad RAM

N79E352(R) has a 256 bytes on-chip scratch-pad RAM. These can be used by the user for temporary storage during program execution. A certain section of this RAM is bit addressable, and can be directly addressed for this purpose.

6.7.6 Stack Pointer

N79E352(R) has an 8-bit Stack Pointer which points to the top of the Stack. This stack resides in the Scratch Pad RAM. Hence the size of the stack is limited by the size of this RAM.

6.8 Power Management

Like the standard 80C52, the N79E352(R) also has IDLE and POWER DOWN modes of operation. The N79E352(R) provides a new Economy mode which allow user to switch the internal clock rate divided by either 4, 64 or 1024. In the IDLE mode, the clock to the CPU core is stopped while the timers, serial ports and interrupts clock continue to operate. In the POWER DOWN mode, all the clock are stopped and the chip operation is completely stopped. This is the lowest power consumption state.

7. MEMORY ORGANIZATION

N79E352(R) separates the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

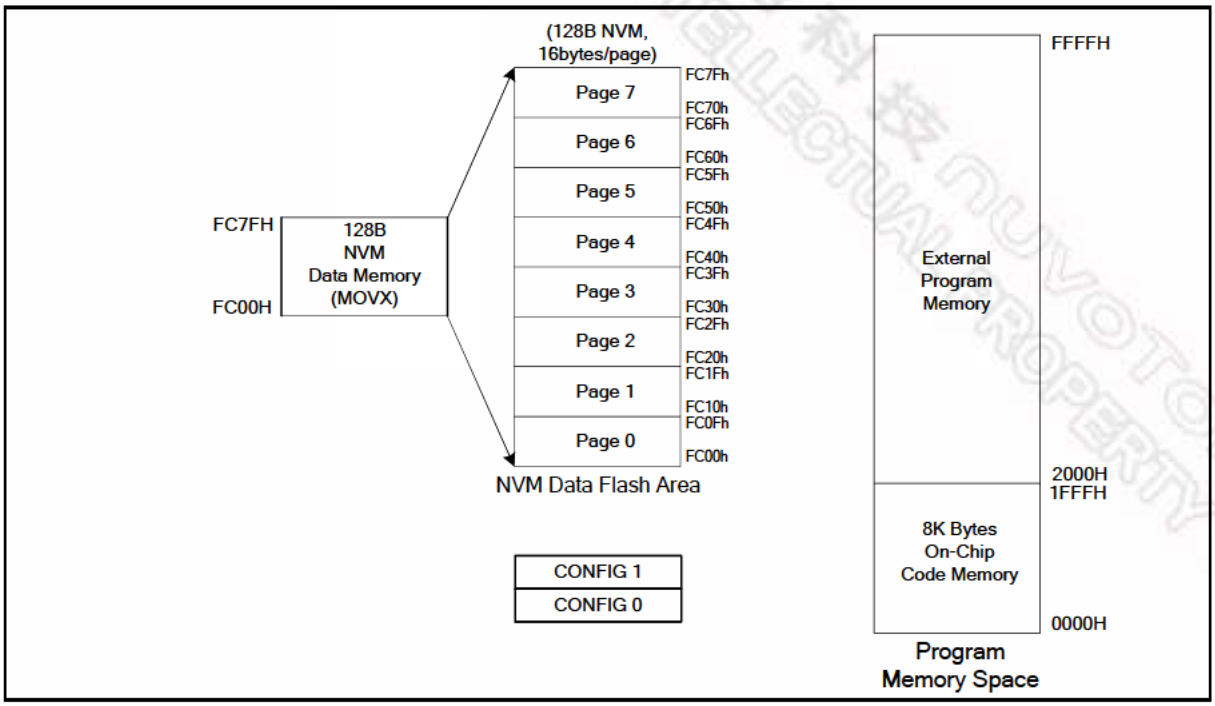


Figure 7-1: N79E352(R) Memory Map

7.1 Program Memory (on-chip Flash)

The Program Memory on N79E352(R) can be up to 8K bytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

7.2 Data Memory

The N79E352(R) has NVM data memory of 128 bytes for customer's data store used. The NVM data memory has 8 pages area and each page has 16 bytes. The N79E352(R) can access up to 64Kbytes of external Data Memory. This memory region is accessed by the MOVX instructions. For NVM s/w read access, user require to set EnNVM bit, otherwise, the access will goes to external data memory. N79E352(R) has the standard 256 bytes of on-chip Scratchpad RAM. This can be accessed either by direct addressing or by indirect addressing. There are also some Special Function Registers (SFRs), which can only be accessed by direct addressing. Since the Scratchpad RAM is only 256 bytes, it can be used only when data contents are small.

7.3 Scratch-pad RAM and Register Map

As mentioned before, N79E352(R) has separate Program and Data Memory areas. The on-chip 256 bytes scratch pad RAM is in addition to the external memory. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.

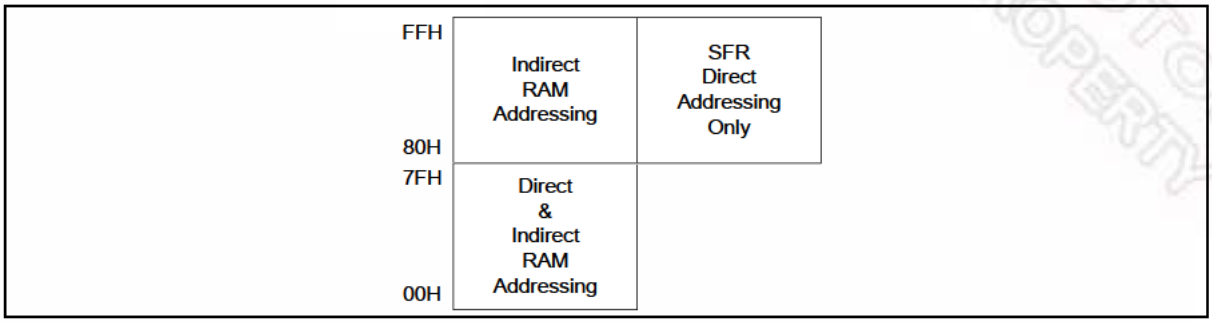


Figure 7-2: N79E352(R) RAM and SFR Memory Map

Since the scratch-pad RAM is only 256 bytes it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM. These are illustrated in next figure.

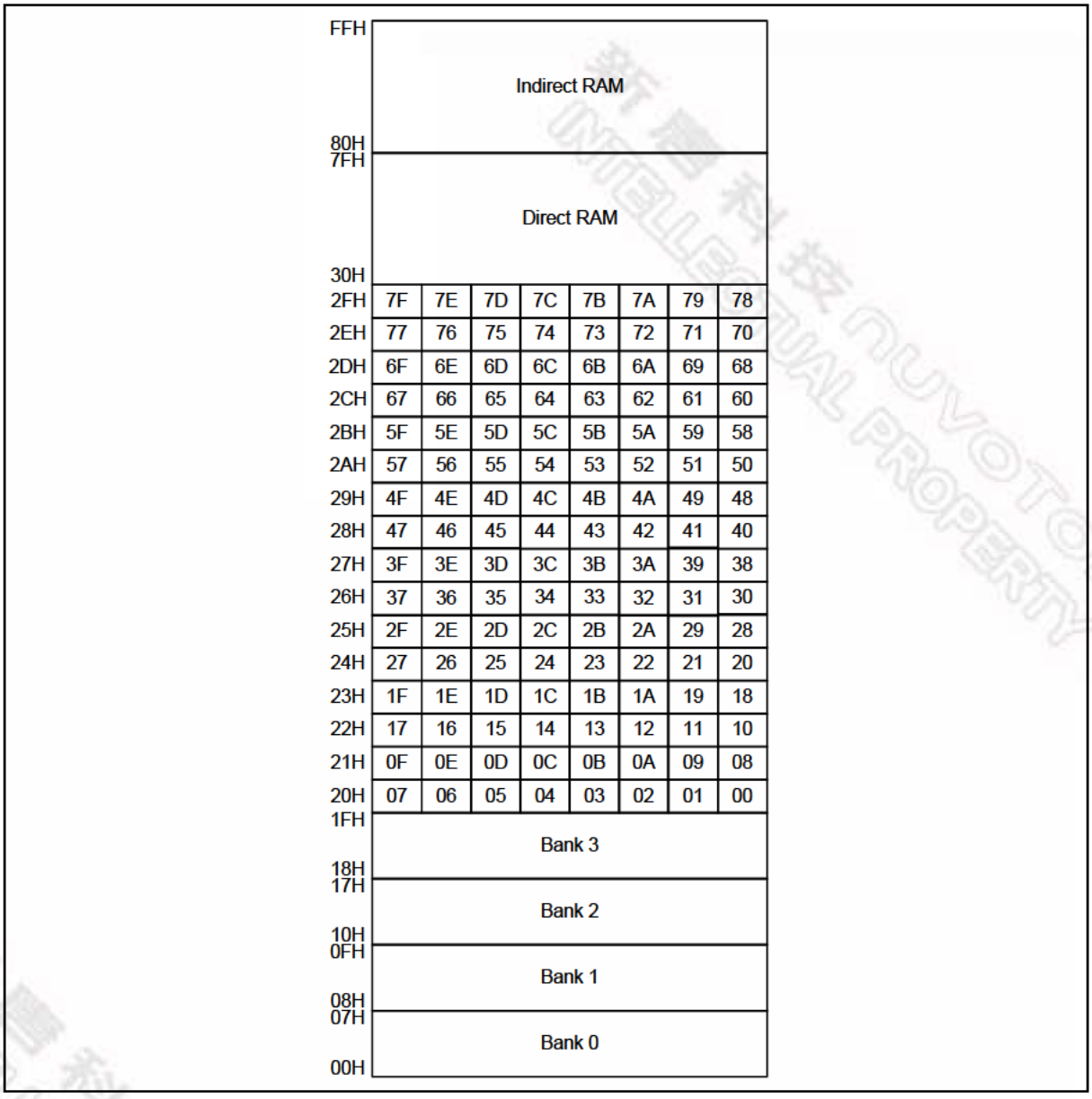


Figure 7-3: Scratch-pad RAM

7.3.1 Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed as Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at any one time N79E352 can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

7.3.2 Bit addressable Locations

The Scratch-pad RAM area from location 20h to 2Fh is byte as well as bit addressable. This means that a bit in this area can be individually addressed. In addition some of the SFRs are also bit addressable. The instruction decoder is able to distinguish a bit access from a byte access by the type of the instruction itself. In the SFR area, any existing SFR whose address ends in a 0 or 8 is bit addressable.

7.3.3 Stack

The scratch-pad RAM can be used for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a jump, call or interrupt is invoked the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07h at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, and then the SP is decreased.

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8. SPECIAL FUNCTION REGISTERS

The N79E352(R) uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes.

The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where one wishes to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. The N79E352(R) contains all the SFRs present in the standard 8052. However, some additional SFRs have been added. In some cases unused bits in the original 8052 have been given new functions. The list of SFRs is as follows. The table is condensed with eight locations per row. Empty locations indicate that there are no registers at these addresses. When a bit or register is not implemented, it will read high.

8.1 SFR Location Table

F8	IP1								FF
F0	B							IP1H	F7
E8	EIE	KBL			PORTS	P5M1	P5M2		EF
E0	ACC				CCL0	CCH0			E7
D8	WDCON		PWM0L	PWM1L	PWMCON1				DF
D0	PSW							PWMCON3	D7
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	NVMCON	NVMDAT	CF
C0	I2CON	I2ADDR	ROMMAP		PMR	STATUS	NVMADDR	TA	C7
B8	IP0	SADEN			I2DATA	I2STATUS	I2CLK	I2TIMER	BF
B0	P3	P0M1	P0M2	P1M1	P1M2	P2M1	P2M2	IP0H	B7
A8	IE	SADDR							AF
A0	P2	KBI	AUXR1	CAPCON0	CAPCON1	P4			A7
98	SCON	SBUF					P3M1	P3M2	9F
90	P1				P5				97
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON		8F
80	P0	SP	DPL	DPH	DPL1	DPH1	DPS	PCON	87

Note: The SFRs in the column with dark borders are bit-addressable.

Table 8- 1: Special Function Register Location Table

SYMBOL	DEFINITION	ADDRESS	MSB	BIT ADDRESS, SYMBOL						LSB	RESET
IP1	INTERRUPT PRIORITY 1	F8H	PCAP	PBO	-	PWDI	-	-	PKB	PI2	00x0 xx00B
IP1H	INTERRUPT HIGH PRIORITY 1	F7H	PCAPH	PBOH	-	PWDIH	-	-	PKBH	PI2H	00x0 xx00B
B	B REGISTER	F0H	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	0000 0000B
P5M2	PORT 5 OUTPUT MODE 2	EEH	-	-	-	-	-	-	P5M2.1	P5M2.0	CONFIG0.PMODE=1; Xxxx xx00B CONFIG0.PMODE=0; Xxxx xx11B
P5M1	PORT 5 OUTPUT MODE 1	EDH	-	-	-	-	-	ENCLK	P5M1.1	P5M1.0	CONFIG0.PMODE=1; Xxxx x000B CONFIG0.PMODE=0; Xxxx x011B
PORTS	PORT SHMITT REGISTER	ECH	-	-	P5S	-	P3S	P2S	P1S	P0S	xx0x 0000B
KBL	KEYBOARD LEVEL REGISTER	E9H	KBL.7	KBL.6	KBL.5	KBL.4	KBL.3	KBL.2	KBL.1	KBL.0	0000 0000B
EIE	INTERRUPT ENABLE 1	E8H	ECPTF	EBO	-	EWDI	-	-	EKB	EI2	00x0 xx00B
CCH0	INPUT CAPTURE 0 HIGH	E5H	CCH0.7	CCH0.6	CCH0.5	CCH0.4	CCH0.3	CCH0.2	CCH0.1	CCH0.0	0000 0000B
CCL0	INPUT CAPTURE 0 LOW	E4H	CCL0.7	CCL0.6	CCL0.5	CCL0.4	CCL0.3	CCL0.2	CCL0.1	CCL0.0	0000 0000B
ACC	ACCUMULATOR	E0H	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	0000 0000B
PWMCON1	PWM CONTROL REGISTER 1	DCH	PWMRUN	-	-	CLRPWM	-	-	-	-	0xx0 xxxxB
PWM1L	PWM 1 LOW BITS REGISTER	DBH	PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0	0000 0000B
PWM0L	PWM 0 LOW BITS REGISTER	DAH	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0	0000 0000B
WDCON	WATCH-DOG CONTROL	D8H	WDRUN	POR	-	-	WDIF	WTRF	EWRST	WDCLR	POR: X1xx 0000B External reset: Xxxx 0xx0B Watchdog reset: Xxxx 01x0B
PWMCON3	PWM CONTROL REGISTER 3	D7H	-	-	PWM1OE	PWM0OE	PCLK.1	PCLK.0	FP1	FP0	Xx00 0000B
PSW	PROGRAM STATUS WORD	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	0000 0000B
NVMDATA	NVM DATA	CFH	NVMDATA.7	NVMDATA.6	NVMDATA.5	NVMDATA.4	NVMDATA.3	NVMDATA.2	NVMDATA.1	NVMDATA.0	0000 0000B
NVMCON	NVM CONTROL	CEH	EER	EWR	EnNVM	-	-	-	-	-	000x xxxxB
TH2	TIMER 2 MSB	CDH	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0	0000 0000B
TL2	TIMER 2 LSB	CCH	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0	0000 0000B
RCAP2H	TIMER 2 RELOAD MSB	CBH	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0	0000 0000B
RCAP2L	TIMER 2 RELOAD LSB	CAH	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0	0000 0000B
T2MOD	TIMER 2 MODE	C9H	-	-	-	ICEN0	T2CR	1	T2OE	DCEN	Xxx0 0100B
T2CON	TIMER 2 CONTROL	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL	0000 0000B
TA	TIMED ACCESS PROTECTION	C7H	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0	0000 0000B
NVMADDR	NVM LOW BYTE ADDRESS	C6H	NVMADDR.7	NVMADDR.6	NVMADDR.5	NVMADDR.4	NVMADDR.3	NVMADDR.2	NVMADDR.1	NVMADDR.0	0000 0000B
STATUS	STATUS REGISTER	C5H	-	-	-	-	-	-	SPTA0	SPRA0	Xxxx xx00B
PMR	POWER MANAGEMENT REGISTER	C4H	CD1	CD0	SWB	-	-	ALE-OFF	-	-	010x xxxxB
ROMMAP	ROMMAP REGISTER	C2H	WS	1	-	-	-	1	1	0	01xxx110B
I2ADDR	I2C ADDRESS1	C1H	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	GC	xxxxxxx0B

SYMBOL	DEFINITION	ADDRESS	MSB	BIT ADDRESS, SYMBOL						LSB	RESET
I2CON	I2C CONTROL REGISTER	C0H	-	ENSI	STA	STO	SI	AA	-	-	x00000xxB
I2TIMER	I2C TIMER COUNTER REGISTER	BFH	-	-	-	-	-	ENTI	DIV4	TIF	Xxxx x000B
I2CLK	I2C CLOCK RATE	BEH	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0	0000 0000B
I2STATUS	I2C STATUS	BDH	I2STATUS.7	I2STATUS.6	I2STATUS.5	I2STATUS.4	I2STATUS.3	I2STATUS.2	I2STATUS.1	I2STATUS.0	1111 1000B
I2DAT	I2C DATA	BCH	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0	xxxxxxxxB
SADEN	SLAVE ADDRESS MASK	B9H	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0	00000000B
IP0	INTERRUPT PRIORITY	B8H	-	-	PT2	PS	PT1	PX1	PT0	PX0	Xx00 0000B
IP0H	INTERRUPT HIGH PRIORITY	B7H	-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	Xx00 0000B
P2M2	PORT 2 OUTPUT MODE 2	B6H	P2M2.7	P2M2.6	P2M2.5	P2M2.4	P2M2.3	P2M2.2	P2M2.1	P2M2.0	CONFIG0.PMODE=1; 0000 0000B CONFIG0.PMODE=0; 1111 1111B
P2M1	PORT 2 OUTPUT MODE 1	B5H	P2M1.7	P2M1.6	P2M1.5	P2M1.4	P2M1.3	P2M1.2	P2M1.1	P2M1.0	CONFIG0.PMODE=1; 0000 0000B CONFIG0.PMODE=0; 1111 1111B
P1M2	PORT 1 OUTPUT MODE 2	B4H	P1M2.7	P1M2.6	P1M2.5	P1M2.4	P1M2.3	P1M2.2	P1M2.1	P1M2.0	CONFIG0.PMODE=1; 0000 0000B CONFIG0.PMODE=0; 1111 1111B
P1M1	PORT 1 OUTPUT MODE 1	B3H	P1M1.7	P1M1.6	P1M1.5	P1M1.4	P1M1.3	P1M1.2	P1M1.1	P1M1.0	CONFIG0.PMODE=1; 0000 0000B CONFIG0.PMODE=0; 1111 1111B
P0M2	PORT 0 OUTPUT MODE 2	B2H	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0	1111 1111B
P0M1	PORT 0 OUTPUT MODE 1	B1H	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0	1111 1111B
P3	PORT3	B0H	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	1111 1111B
			/RD	/WR	T1	T0	/INT1	/INT0	TXD	RXD	
SADDR	SLAVE ADDRESS	A9H	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0	0000 0000B
IE	INTERRUPT ENABLE	A8H	EA	-	ET2	ES	ET1	EX1	ET0	EX0	0x00 0000B
P4	PORT4	A5H	-	-	-	-	P4.3	P4.2	P4.1	P4.0	Xxxx 1111B
CAPCON1	CAPTURE CONTROL 1	A4H	0	T0CC	-	-	ENF0	-	-	CPTF0	00xx 0xx0B
CAPCON0	CAPTURE CONTROL 0	A3H	-	-	-	-	CCT0.1	CCT0.0	-	-	Xxxx 00xxB
AUXR1	AUX FUNCTION REGISTER 1	A2H	KBF	BOD	BOI	LPBOV	SRST	BOV1	BOV0	BOS	0000 0000B
KBI	KEYBOARD INTERRUPT	A1H	KBI.7	KBI.6	KBI.5	KBI.4	KBI.3	KBI.2	KBI.1	KBI.0	0000 0000B
P2	PORT 2	A0H	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	1111 1111B
			A15	A14	A13	A12	A11	A10	A9	A8	
P3M2	PORT 3 OUTPUT MODE 2	9FH	P3M2.7	P3M2.6	P3M2.5	P3M2.4	P3M2.3	P3M2.2	P3M2.1	P3M2.0	CONFIG0.PMODE=1; 0000 0000B CONFIG0.PMODE=0; 1111 1111B

SYMBOL	DEFINITION	ADDRESS	MSB			BIT ADDRESS, SYMBOL				LSB	RESET
P3M1	PORT 3 OUTPUT MODE 1	9EH	P3M1.7	P3M1.6	P3M1.5	P3M1.4	P3M1.3	P3M1.2	P3M1.1	P3M1.0	CONFIG0.PMODE=1; 0000 0000B CONFIG0.PMODE=0; 1111 1111B
SBUF	SERIAL BUFFER	99H	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0	Xxxx xxxxB
SCON	SERIAL CONTROL	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	0000 0000B
P5	PORT5	94H	-	-	-	-	-	-	P5.1	P5.0	Xxxx xx11B
			-	-	-	-	-	-	XTAL1	XTAL2	
			-	-	-	-	-	-	-	CLKOUT	
P1	PORT 1	90H	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	1111 1111B
			-	-	PWM1	PWM0	SCL	SDA	T2EX	T2	
CKCON	CLOCK CONTROL	8EH	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0	0000 0001B
TH1	TIMER HIGH 1	8DH	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0	0000 0000B
TH0	TIMER HIGH 0	8CH	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0	0000 0000B
TL1	TIMER LOW 1	8BH	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0	0000 0000B
TL0	TIMER LOW 0	8AH	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0	0000 0000B
TMOD	TIMER MODE	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	0000 0000B
TCON	TIMER CONTROL	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	0000 0000B
PCON	POWER CONTROL	87H	SM0D	SMOD0	BOF	-	GF1	GF0	PD	IDL	001x 0000B
DPS	DATA POINTER SELECT	86H	-	-	-	-	-	-	-	DPS.0	Xxxx xxx0B
DPH1	DATA POINTER HIGH 1	85H	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0	0000 0000B
DPL1	DATA POINTER LOW 1	84H	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0	0000 0000B
DPH	DATA POINTER HIGH	83H	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0	0000 0000B
DPL	DATA POINTER LOW	82H	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0	0000 0000B
SP	STACK POINTER	81H	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0	0000 0111B
P0	PORT 0	80H	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	1111 1111B
			AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	
			KB7	KB6	KB5	KB4	KB3	KB2	KB1	KB0	

新唐科技 NUVOTON INTELLECTUAL PROPERTY

8.2 SFR Detail Bit Descriptions

PORT 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

Port 0 is an open-drain bi-directional I/O port. This port provides a multiplexed low order address/data bus during accesses to external memory. The ports also support alternate input function for Keyboard pins (KB0-7).

BIT	NAME	FUNCTION
7	P0.7	AD7 or KB7 or I/O pin by alternative.
6	P0.6	AD6 or KB6 or I/O pin by alternative.
5	P0.5	AD5 or KB5 or I/O pin by alternative.
4	P0.4	AD4 or KB4 or I/O pin by alternative.
3	P0.3	AD3 or KB3 or I/O pin by alternative.
2	P0.2	AD2 or KB2 or I/O pin by alternative.
1	P0.1	AD1 or KB1 or I/O pin by alternative.
0	P0.0	AD0 or KB0 or I/O pin by alternative.

Note: The initial value of the port is set by CONFIG0.PRHI bit. The default setting for CONFIG0.PRHI =1 which the alternative function output is turned on upon reset. If CONFIG0.PRHI is set to 0, the user has to write a 1 to port SFR to turn on the alternative function output.

STACK POINTER

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

BIT	NAME	FUNCTION
7-0	SP.[7:0]	The Stack Pointer stores the Scratch-pad RAM address where the stack begins. In other words it always points to the top of the stack.

DATA POINTER LOW

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

BIT	NAME	FUNCTION
7-0	DPL.[7:0]	This is the low byte of the standard 8052 16-bit data pointer.

DATA POINTER HIGH

Bit:	7	6	5	4	3	2	1	0

DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

BIT	NAME	FUNCTION
7-0	DPH.[7:0]	This is the high byte of the standard 8052 16-bit data pointer. This is the high byte of the DPTR 16-bit data pointer.

DATA POINTER LOW 1

Bit:

7	6	5	4	3	2	1	0
DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0

Mnemonic: DPL1 Address: 84h

BIT	NAME	FUNCTION
7-0	DPL1.[7:0]	This is the low byte of the new additional 16-bit data pointer that has been added to the N79E352(R). The user can switch between DPL, DPH and DPL1, DPH1 simply by setting register DPS = 1. The instructions that use DPTR will now access DPL1 and DPH1 in place of DPL and DPH. If they are not required they can be used as conventional register locations by the user.

DATA POINTER HIGH 1

Bit:

7	6	5	4	3	2	1	0
DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0

Mnemonic: DPH1 Address: 85h

BIT	NAME	FUNCTION
7-0	DPH1.[7:0]	This is the high byte of the new additional 16-bit data pointer that has been added to the N79E352(R). The user can switch between DPL, DPH and DPL1, DPH1 simply by setting register DPS = 1. The instructions that use DPTR will now access DPL1 and DPH1 in place of DPL and DPH. If they are not required they can be used as conventional register locations by the user.

DATA POINTER SELECT

Bit:

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DPS.0

Mnemonic: DPS Address: 86h

BIT	NAME	FUNCTION
7-1	-	Reserved.
0	DPS	This bit is used to select either the DPL,DPH pair or the DPL1,DPH1 pair as the active Data Pointer. When set to 1, DPL1, DPH1 will be selected, otherwise DPL, DPH will be selected.

POWER CONTROL

Bit:

7	6	5	4	3	2	1	0

SMOD	SMOD0	BOF	-	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial port baud rate in mode 1, 2, and 3.
6	SMOD0	0: Framing Error Detection Disable. SCON.7 (SM0/FE) bit is used as SM0 (standard 8052 function). 1: Framing Error Detection Enable. SCON.7 (SM0/FE) bit is used to reflect as Frame Error (FE) status flag.
5	BOF	0: Cleared by software. 1: Set automatically when a brownout reset or interrupt has occurred. Also set at power on.
4	-	Reserved.
3	GF1	General purpose user flags.
2	GF0	General purpose user flags.
1	PD	1: The CPU goes into the POWER DOWN mode. In this mode, all the clocks are stopped and program execution is frozen.
0	IDL	1: The CPU goes into the IDLE mode. In this mode, the clocks CPU clock stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

TIMER CONTROL

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 Overflow Flag. This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 Overflow Flag. This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
3	IE1	Interrupt 1 Edge Detect Flag: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
2	IT1	Interrupt 1 Type Control. Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect Flag. Set by hardware when an edge/level is detected on

		$\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
0	IT0	Interrupt 0 Type Control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL

Bit:

7	6	5	4	3	2	1	0
GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
TIMER1				TIMER0			

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.
5	M1	Timer 1 mode select bit 1. See table below.
4	M0	Timer 1 mode select bit 0. See table below.
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 control bit is set.
2	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the T0 pin.
1	M1	Timer 0 mode select bit 1. See table below.
0	M0	Timer 0 mode select bit 0. See table below.

M1, M0: Mode Select bits:

M1	M0	MODE
0	0	Mode 0: 8-bit timer/counter TLx serves as 5-bit pre-scale.
0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx.
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer0 control bits. TH0 is an 8-bit timer only controlled by Timer1 control bits. (Timer 1) Timer/Counter 1 is stopped.

TIMER 0 LSB

Bit:

7	6	5	4	3	2	1	0
TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

BIT	NAME	FUNCTION
7-0	TL0.[7:0]	Timer 0 LSB.

TIMER 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

BIT	NAME	FUNCTION
7-0	TL1.[7:0]	Timer 1 LSB.

TIMER 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

BIT	NAME	FUNCTION
7-0	TH0.[7:0]	Timer 0 MSB.

TIMER 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

BIT	NAME	FUNCTION
7-0	TH1.[7:0]	Timer 1 MSB.

CLOCK CONTROL

Bit:	7	6	5	4	3	2	1	0
	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0

Mnemonic: CKCON Address: 8Eh

BIT	NAME	FUNCTION
7-5	WD1~0	Watchdog timer mode select bits: These bits determine the time-out period for the watchdog timer. In all four time-out options the reset time-out is 512 clocks more than the interrupt time-out period.

WD1	WD0	Interrupt time-out	Reset time-out
0	0	2^6	$2^6 + 512$
0	1	2^9	$2^9 + 512$
1	0	2^{13}	$2^{13} + 512$
1	1	2^{15}	$2^{15} + 512$

BIT	NAME	FUNCTION
5	T2M	Timer 2 clock select: 0: Timer 2 uses a divide by 12 clocks. 1: Timer 2 uses a divide by 4 clocks.
4	T1M	Timer 1 clock select: 0: Timer 1 uses a divide by 12 clocks. 1: Timer 1 uses a divide by 4 clocks.
3	T0M	Timer 0 clock select: 0: Timer 0 uses a divide by 12 clocks. 1: Timer 0 uses a divide by 4 clocks.
2~0	MD2~0	Stretch MOVX select bits: These three bits are used to select the stretch value for the MOVX instruction. Using a variable MOVX length enables the user to access slower external memory devices or peripherals without the need for external circuits. The $\overline{RD}$ or $\overline{WR}$ strobe will be stretched by the selected interval. When accessing the on-chip SRAM, the MOVX instruction is always in 2 machine cycles regardless of the stretch setting. By default, the stretch has value of 1. If the user needs faster accessing, then a stretch value of 0 should be selected. MD2 MD1 MD0 Stretch value MOVX duration 0 0 0 0 2 machine cycles 0 0 1 1 3 machine cycles *(Default)* 0 1 0 2 4 machine cycles 0 1 1 3 5 machine cycles 1 0 0 4 6 machine cycles 1 0 1 5 7 machine cycles 1 1 0 6 8 machine cycles 1 1 1 7 9 machine cycles

PORT 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7	P1.7	Dedicated I/O pin.
6	P1.6	Dedicated I/O pin.
5	P1.5	PWM1 or I/O pin by alternative.
4	P1.4	PWM0 or I/O pin by alternative.

BIT	NAME	FUNCTION
3	P1.3	SCL or I/O pin by alternative.
2	P1.2	SDA or I/O pin by alternative.
1	P1.1	T2EX or I/O pin by alternative.
0	P1.0	T2 or I/O pin by alternative.

PORT 5

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	P5.1/ XTAL1	P5.0/ XTAL2/ CLKOUT

Mnemonic: P5 Address: 94h

BIT	NAME	FUNCTION
7~2	-	Reserved.
1	P5.1	XTAL1 clock input or I/O pin by alternative.
0	P5.0	XTAL2 or CLKOUT pin or I/O pin by alternative.

SERIAL PORT CONTROL

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial port mode select bit 0 or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.
6	SM1	Serial Port mode select bit 1. See table below.
5	SM2	Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, the SM2 bit controls the serial port clock. If set to 0, then the serial port runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052. When set to 1, the serial clock become divide by 4 of the oscillator clock. This results in faster synchronous serial communication.
4	REN	Receive enable: 0: Disable serial reception. 1: Enable serial reception.
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is

BIT	NAME	FUNCTION
		the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software.

SM1, SM0: Mode Select bits:

MODE	SM1	SM0	DESCRIPTION	LENGTH	BAUD RATE
0	0	0	Synchronous	8	F_{CPU} divided by 4 or 12
1	0	1	Asynchronous	10	Variable
2	1	0	Asynchronous	11	F_{CPU} divided by 32 or 64
3	1	1	Asynchronous	11	Variable

SERIAL DATA BUFFER

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

BIT	NAME	FUNCTION
7-0	SBUF.[7:0]	Serial data on the serial port is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive resister, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

PORT 3 OUTPUT MODE 1

Bit:	7	6	5	4	3	2	1	0
	P3M1.7	P3M1.6	P3M1.5	P3M1.4	P3M1.3	P3M1.2	P3M1.1	P3M1.0

Mnemonic: P3M1 Address: 9Eh

BIT	NAME	FUNCTION
7-0	P3M1.7-0	To control the output configuration of P3 [7:0].

PORT 3 OUTPUT MODE 2

Bit:	7	6	5	4	3	2	1	0
	P3M2.7	P3M2.6	P3M2.5	P3M2.4	P3M2.3	P3M2.2	P3M2.1	P3M2.0

Mnemonic: P3M2 Address: 9Fh

BIT	NAME	FUNCTION
7-0	P3M2.7-0	See as below table.

Port Output Configuration Settings:

PXM1.Y	PXM2.Y	PORT INPUT/OUTPUT MODE
0	0	Quasi-bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance) PORTS.PxS=0, TTL input PORTS.PxS=1, Schmitt input
1	1	Open Drain

Note:

1. X = 0-3, 5. Y = 0-7.
2. CONFIG0.PMODE bit will determine the port1~3 and port 5 are Quasi or Open drain upon reset. See detail PMODE descriptions.

PORT 2

Bit:	7	6	5	4	3	2	1	0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

Mnemonic: P2 Address: A0h

P2.7-0: Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.

BIT	NAME	FUNCTION
7	P2.7	A15 or I/O pin by alternative.
6	P2.6	A14 or I/O pin by alternative.
5	P2.5	A13 or I/O pin by alternative.
4	P2.4	A12 or I/O pin by alternative.
3	P2.3	A11 or I/O pin by alternative.
2	P2.2	A10 or I/O pin by alternative.
1	P2.1	A9 or I/O pin by alternative.
0	P2.0	A8 or I/O pin by alternative.

KEYBOARD INTERRUPT

Bit:	7	6	5	4	3	2	1	0
	KBI.7	KBI.6	KBI.5	KBI.4	KBI.3	KBI.2	KBI.1	KBI.0

Mnemonic: KBI Address: A1h

BIT	NAME	FUNCTION
7	KBI.7	1: Enable P0.7 as a cause of a Keyboard interrupt.
6	KBI.6	1: Enable P0.6 as a cause of a Keyboard interrupt.
5	KBI.5	1: Enable P0.5 as a cause of a Keyboard interrupt.
4	KBI.4	1: Enable P0.4 as a cause of a Keyboard interrupt.

3	KBI.3	1: Enable P0.3 as a cause of a Keyboard interrupt.
2	KBI.2	1: Enable P0.2 as a cause of a Keyboard interrupt.
1	KBI.1	1: Enable P0.1 as a cause of a Keyboard interrupt.
0	KBI.0	1: Enable P0.0 as a cause of a Keyboard interrupt.

AUX FUNCTION REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	KBF	BOD	BOI	LPBOV	SRST	BOV1	BOV0	BOS

Mnemonic: AUXR1 Address: A2h

BIT	NAME	FUNCTION
7	KBF	Keyboard Interrupt Flag: 1: When any pin of port 0 that is enabled for the Keyboard Interrupt function triggers (trigger level is depending on SFR KBL configuration). Must be cleared by software.
6	BOD	Brown Out Disable: 0: Enable Brownout Detect function. 1: Disable Brownout Detect function and save power. BOD is initialized at all resets with the inverse value of bit CBOD in config0.3 bit. User is able to re-configure this bit after reset.
5	BOI	Brown Out Interrupt: 0: Disable Brownout Detect Interrupt function. 1: This prevents brownout detection from causing a chip reset and allows the Brownout Detect function to be used as an interrupt.
4	LPBOV	Low Power Brown Out Detect control: 0: When BOD is enable, the Brown Out detect is always turned on by normal run or Power Down mode. 1: When BOD is enable, the 1/16 time will be turned on Brown Out detect circuit by Power Down mode. When uC is entry Power Down mode, the BOD will enable internal RC OSC (20KHz).
3	SRST	Software reset: 1: Reset the chip as if a hardware reset occurred. **SRST** require Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

2~1	BOV.1~0	Brownout voltage selection bits, see below table. BOV.1 / BOV.0 / Brownout Voltage 0 / x / Brownout voltage is 2.6V 1 / 0 / Brownout voltage is 3.8V 1 / 1 / Brownout voltage is 4.5V These bits are initialized at all resets with the inverse values of bits CBOV.1-0 in config1.3-2 bits. User is able to re-configure these bits after reset.
0	BOS	Brownout Status bit(Read only) 0: V_{DD} is above V_{BOR+} 1: V_{DD} is below V_{BOR-}

CAPTURE CONTROL 0 REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	CCT0.1	CCT0.0	-	-

Mnemonic: CAPCON0 Address: A3h

BIT	NAME	FUNCTION
7-4	-	Reserved.
3-2	CCT0[1:0]	Capture 0 edge select: 00 : Rising edge trigger. 01 : Falling edge trigger. 10 : Either rising or falling edge trigger. 11 : Reserved
1-0	-	Reserved.

CAPTURE CONTROL 1 REGISTER

Bit:	7	6	5	4	3	2	1	0
	0	T0CC	-	-	ENF0	-	-	CPTF0

Mnemonic: CAPCON1 Address: A4h

BIT	NAME	FUNCTION
7	-	***Must be 0.***
6	T0CC	Timer 0 Clear Counter bit. 0: Timer 0 is not clear when input capture/cap sensor trigger. 1: Timer 0 will be cleared when input capture/cap sensor trigger.
5-4	-	Reserved.
3	ENF0	Enable filter for capture input 0.

2-1	-	Reserved.
0	CPTF0	External input capture 0 interrupt flag. It can be cleared by software.

PORT 4

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	P4.3	P4.2	P4.1	P4.0

Mnemonic: P4 Address: A5h

BIT	NAME	FUNCTION
7~4	-	Reserved.
3~0	P4.3~0	Port 4 is a bi-directional I/O port with internal pull-ups. Port 4 can not use bit-addressable instruction (SETB or CLR).

INTERRUPT ENABLE

Bit:	7	6	5	4	3	2	1	0
	EA	-	ET2	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

BIT	NAME	FUNCTION
7	EA	Global enable. Enable/Disable all interrupts.
6	-	Reserved.
5	ET2	Enable Timer 2 interrupt.
4	ES	Enable Serial Port 0 interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

SLAVE ADDRESS

Bit:	7	6	5	4	3	2	1	0
	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0

Mnemonic: SADDR Address: A9h

BIT	NAME	FUNCTION
7~0	SADDR	The SADDR should be programmed to the given or broadcast address for serial port 0 to which the slave processor is designated.

PORT 3

Bit:	7	6	5	4	3	2	1	0
	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0

Mnemonic: P3 Address: B0h

P3.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7	P3.7	/RD or I/O pin by alternative.
6	P3.6	/WR or I/O pin by alternative.
5	P3.5	T1 or I/O pin by alternative.
4	P3.4	T0 or I/O pin by alternative.
3	P3.3	/INT1 or I/O pin by alternative.
2	P3.2	/INT0 or I/O pin by alternative.
1	P3.1	TxD or I/O pin by alternative.
0	P3.0	RxD or I/O pin by alternative.

PORT 0 OUTPUT MODE 1

Bit:	7	6	5	4	3	2	1	0
	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0

Mnemonic: P0M1 Address: B1h

BIT	NAME	FUNCTION
7-0	P0M1	To control the output configuration of P0 bits [7:0]

PORT 0 OUTPUT MODE 2

Bit:	7	6	5	4	3	2	1	0
	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0

Mnemonic: P0M2 Address: B2h

BIT	NAME	FUNCTION
7-0	P0M2	To control the output configuration of P0 bits [7:0]

PORT 1 OUTPUT MODE 1

Bit:	7	6	5	4	3	2	1	0
	P1M1.7	P1M1.6	P1M1.5	P1M1.4	P1M1.3	P1M1.2	P1M1.1	P1M1.0

Mnemonic: P1M1 Address: B3h

BIT	NAME	FUNCTION
7-0	P1M1	To control the output configuration of P1 bits [7:0].

PORT 1 OUTPUT MODE 2

Bit:	7	6	5	4	3	2	1	0
	P1M2.7	P1M2.6	P1M2.5	P1M2.4	P1M2.3	P1M2.2	P1M2.1	P1M2.0

Mnemonic: P1M2 Address: B4h

BIT	NAME	FUNCTION
7-0	P1M2	To control the output configuration of P1 bits [7:0].

PORT 2 OUTPUT MODE 1

Bit:	7	6	5	4	3	2	1	0
	P2M1.7	P2M1.6	P2M1.5	P2M1.4	P2M1.3	P2M1.2	P2M1.1	P2M1.0

Mnemonic: P2M1 Address: B5h

BIT	NAME	FUNCTION
7-0	P2M1	To control the output configuration of P2 bits [7:0]

PORT 2 OUTPUT MODE 2

Bit:	7	6	5	4	3	2	1	0
	P2M2.7	P2M2.6	P2M2.5	P2M2.4	P2M2.3	P2M2.2	P2M2.1	P2M2.0

Mnemonic: P2M2 Address: B6h

BIT	NAME	FUNCTION
7-0	P2M2	To control the output configuration of P2 bits [7:0]

INTERRUPT HIGH PRIORITY

Bit:	7	6	5	4	3	2	1	0
	-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Mnemonic: IP0H Address: B7h

BIT	NAME	FUNCTION
7~6	-	Reserved.
5	PT2H	1: To set interrupt high priority of Timer 2 is highest priority level.
4	PSH	1: To set interrupt high priority of Serial port is highest priority level.
3	PT1H	1: Ro set interrupt high priority of Timer 1 is highest priority level.
2	PX1H	1: To set interrupt high priority of External interrupt 1 is highest priority level.
1	PT0H	1: To set interrupt high priority of Timer 0 is highest priority level.
0	PX0H	1: To set interrupt high priority of External interrupt 0 is highest priority level.

INTERRUPT PRIORITY 0

Bit:	7	6	5	4	3	2	1	0
	-	-	PT2	PS	PT1	PX1	PT0	PX0

Mnemonic: IP0 Address: B8h

BIT	NAME	FUNCTION
7~6	-	Reserved.
5	PT2	1: To set interrupt priority of Timer 2 is higher priority level.
4	PS	1: To set interrupt priority of Serial port is higher priority level.

3	PT1	1: To set interrupt priority of Timer 1 is higher priority level.
2	PX1	1: To set interrupt priority of External interrupt 1 is higher priority level.
1	PT0	1: To set interrupt priority of Timer 0 is higher priority level.
0	PX0	1: To set interrupt priority of External interrupt 0 is higher priority level.

SLAVE ADDRESS MASK ENABLE

Bit:	7	6	5	4	3	2	1	0
	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0

Mnemonic: SADEN Address: B9h

BIT	NAME	FUNCTION
7~0	SADEN	This register enables the Automatic Address Recognition feature of the Serial port 0. When a bit in the SADEN is set to 1, the same bit location in SADDR will be compared with the incoming serial data. When SADEN is 0, then the bit becomes a "don't care" in the comparison. This register enables the Automatic Address Recognition feature of the Serial port 0. When all the bits of SADEN are 0, interrupt will occur for any incoming address.

I2C DATA REGISTER

Bit:	7	6	5	4	3	2	1	0
	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0

Mnemonic: I2DAT Address: BCh

BIT	NAME	FUNCTION
7-0	I2DAT.[7:0]	The data register of I2C.

I2C STATUS REGISTER

Bit:	7	6	5	4	3	2	1	0
	I2STATUS.7	I2STATUS.6	I2STATUS.5	I2STATUS.4	I2STATUS.3	-	-	-

Mnemonic: I2STATUS Address: BDh

BIT	NAME	FUNCTION
7-0	I2STATUS.[7:0]	The status register of I2C: The three least significant bits are always 0. The five most significant bits contain the status code. There are 23 possible status codes. When I2STATUS contains F8H, no serial interrupt is requested. All other I2STATUS values correspond to defined I2C states. When each of these states is entered, a status interrupt is requested (SI = 1). A valid status code is present in I2STATUS one machine cycle after SI is set by hardware and is still present one machine cycle after SI has been reset by software. In addition, states 00H stands for a Bus Error. A Bus Error occurs when a START or STOP condition is present at an illegal position in the formation frame. Example of illegal position are during the serial transfer of an address byte, a data byte or an acknowledge bit.

I2C BAUD RATE CONTROL REGISTER

Bit:	7	6	5	4	3	2	1	0

I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0

Mnemonic: I2CLK Address: BEh

BIT	NAME	FUNCTION
7-0	I2CLK.[7:0]	The I2C clock rate bits.

I2C TIMER COUNTER REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	ENTI	DIV4	TIF

Mnemonic: I2TIMER Address: BFh

BIT	NAME	FUNCTION
7~3	-	Reserved.
2	ENTI	Enable I2C 14-bits Timer Counter: 0: Disable 14-bits Timer Counter count. 1: Enable 14-bits Timer Counter count. After enable ENTI and ENSI, the 14-bit counter will be counted. When SI flag of I2C is set, the counter will stop to count and 14-bits Timer Counter will be cleared.
1	DIV4	I2C Timer Counter clock source divide function: 0: The 14-bits Timer Counter source clock is F_{CPU} clock. 1: The 14-bits Timer Counter source clock is divided by 4.
0	TIF	The I2C Timer Counter count flag: 0: The 14-bits Timer Counter is not overflow. 1: The 14-bits Timer Counter is overflow. Before enable I2C Timer (both ENTI, ENSI = [1,1]) the SI must be cleared. If I2C interrupt is enabled. The I2C interrupt service routine will be executed. This bit is cleared by software.

I2C CONTROL REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	ENSI	STA	STO	SI	AA	-	-

Mnemonic: I2CON Address: C0h

BIT	NAME	FUNCTION
7	-	Reserved.
6	ENSI	0: Disable I2C Serial Function. The SDA and SCL output are in a high impedance state. SDA and SCL input signals are ignored, I2C is not in the addressed slave mode or it is not addressable, and STO bit in I2CON is forced to “0”. No other bits are affected. P1.3 (SCL) and P1.2 (SDA) may be used as open drain I/O ports. 1: Enable I2C Serial Function. The P1.2 and P1.3 port latches must be to logic 1.
5	STA	START flag: 0: The STA bit is reset, no START condition or repeated START condition will

		be generated. 1: The STA bit is set to enter a master mode. The I2C hardware checks the status of I2C bus and generates a START condition if the bus is free. If bus is not free, then I2C waits for a STOP condition and generates a START condition after a delay. If STA is set while I2C is already in a master mode and one or more bytes are transmitted or received, I2C transmits a repeated START condition. STA may be set any time. STA may also be set when I2C interface is an addressed slave mode.
4	STO	The bit STO bit is set while I2C is in a master mode. A STOP condition is transmitted to the I2C bus. When the STOP condition is detected on the bus, the I2C hardware clears the STO flag. In a slave mode, the STO flag may be set to recover from a bus error condition. In this case, no STOP condition is transmitted to the I2C bus. However, the I2C hardware behaves as if a STOP condition has been received and it switches to the not addressable slave receiver mode. The STO flag is automatically cleared by hardware. If the STA and STO bits are both set, then a STOP condition is transmitted to the I2C bus if I2C is in a master mode (in a slave mode, I2C generates an internal STOP condition which is not transmitted). I2C then transmits a START condition.
3	SI	0: When the SI flag is reset, no serial interrupt is requested, and there is no stretching on the serial clock on the SCL line. 1: When a new I2C bus state is present in the I2STATUS register, the SI flag is set by hardware, and, if the EA and ES bits (in IE register) are both set, a serial interrupt is requested when SI is set. The only state that does not cause SI to be set is state F8H, which indicates that no relevant state information is available. When SI is set, the low period of the serial clock on the SCL line is stretched, and the serial transfer is suspended. A high level on the SCL line is unaffected by the serial interrupt flag. SI must be cleared by software.
2	AA	Assert Acknowledge Flag: 0: A not acknowledge (high level to SDA) will be returned during the acknowledge clock pulse on SCL when: 1) A data has been received while I2C is in the master receiver mode. 2) A data byte has been received while I2C is in the addressed slave receiver mode. 1: An acknowledge (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line when: 1) The own slave address has been received. 2) A data byte has been received while I2C is in the master receiver mode. 3) A data byte has been received while I2C is in the addressed slave receiver mode. 4) The General Call address has been received while the general call bit (GC) in I2ADDR is set.
1~0	-	Reserved.

I2C ADDRESS REGISTER

Bit:	7	6	5	4	3	2	1	0
	I2ADDR.7	I2ADDR.6	I2ADDR.5	I2ADDR.4	I2ADDR.3	I2ADDR.2	I2ADDR.1	GC

Mnemonic: I2ADDR Address: C1h

BIT	NAME	FUNCTION

7~1	I2ADDR.[7:1]	I2C Address register: The 8051 uC can read from and write to this 8-bit, directly addressable SFR. The content of this register is irrelevant when I2C is in master mode. In the slave mode, the seven most significant bits must be loaded with the MCU's own address. The I2C hardware will react if either of the address is matched.
0	GC	General Call Function. 0: Disable General Call Function. 1: Enable General Call Function.

ROMMAP

Bit:	7	6	5	4	3	2	1	0
	WS	1	-	-	-	1	1	0

Mnemonic: ROMMAP Address: C2h

BIT	NAME	FUNCTION
7	WS	Wait State Signal Enable. Setting this bit enables the $\overline{WAIT}$ signal on P4.0. The device will sample the wait state control signal $\overline{WAIT}$ via P4.0 during MOVX instruction. This bit is **time access protected.**
6~0	-	Reserved.

```
TA      REG     C7H
ROMMAP  REG     C2H
CKCON   REG     8EH
MOV     TA,#AAH
MOV     TA,#55H
ORL     ROMMAP,#10000000B ; Set  WS bit  to enable wait signal.
```

POWER MANAGEMENT REGISTER

Bit:	7	6	5	4	3	2	1	0
	CD1	CD0	SWB	-	-	ALE-OFF	-	-

Mnemonic: PMR Address: C4h

BIT	NAME	FUNCTION

7~6	CD1~0	Clock Divide Control. These bit selects the number of clocks required to generate one machine cycle. There are three modes including divide by 4, 64 or 1024. Switching between modes must first go back devide by 4 mode. For instance, to go from 64 to 1024 clocks/machine cycle the device must first go from 64 to 4 clocks/machine cycle, and then from 4 to 1024 clocks/machine cycle.
5	SWB	Switchback Enable. Setting this bit allows an enabled external interrupt or serial port/I2C activity to force the CD1, CD0 to divide by 4 state (0,X). The device will switch modes at the start of the jump to interrupt service routine while an external interrupt is enabled and actually recognized by microcontroller. While a serial port/I2C reception, the switchback occurs at the start of the instruction following the falling edge of the start bit. Note: Changing SWB bit is ignored during serial port/I2C activities.
4~3	-	Reserved.
2	ALE-0FF	This bit disables the expression of the ALE signal on the device pin during all on-board program and data memory accesses. External memory accesses will automatically enable ALE independent of ALE-OFF. 0 = ALE expression is enable. 1 = ALE expression is disable.
1~0	-	Reserved.

CD1,	CD0	Clocks/machine Cycle
0	X	4
1	0	64
1	1	1024

STATUS

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	SPTA0	SPRA0

Mnemonic: STATUS Address: C5h

BIT	NAME	FUNCTION
7-2	-	Reserved.
1	SPTA0	Serial Port 0 Transmit Activity. This bit is set during serial port 0 is currently transmitting data. It is cleared when TI bit is set by hardware. Changing the Clock Divide Control bits CD0, CD1 will be ignored when this bit is set to 1 and SWB = 1.
0	SPRA0	Serial Port 0 Receive Activity. This bit is set during serial port 0 is currently receiving a data. It is cleared when RI bit is set by hardware. Changing the Clock Divide Control bits CD0, CD1 will be ignored when this bit is set to 1 and SWB = 1.

NVM LOW BYTE ADDRESS

Bit:	7	6	5	4	3	2	1	0

-	NVMADD R.6	NVMADD R.5	NVMADD R.4	NVMADD R.3	NVMADD R.2	NVMADD R.1	NVMADD R.0

Mnemonic: NVMADDR Address: C6h

BIT	NAME	FUNCTION
7	-	Reserved
6~0	NVMADDR.[6:0]	The NVM address: The register indicates NVM data memory address on On-Chip code memory space.

TIMED ACCESS

Bit:

7	6	5	4	3	2	1	0
TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0

Mnemonic: TA Address: C7h

BIT	NAME	FUNCTION
7-0	TA.[7:0]	The Timed Access register: The Timed Access register controls the access to protected bits. To access protected bits, the user must first write AAH to the TA. This must be immediately followed by a write of 55H to TA. Now a window is opened in the protected bits for three machine cycles, during which the user can write to these bits.

TIMER 2 CONTROL

Bit:

7	6	5	4	3	2	1	0
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C / $\overline{T2}$	CP / $\overline{RL2}$

Mnemonic: T2CON Address: C8h

BIT	NAME	FUNCTION
7	TF2	Timer 2 overflow flag: Timer 2 overflow flag: This bit is set when Timer 2 overflows. It is also set when the count is equal to the capture register in down count mode. It can be set only if RCLK and TCLK are both 0. It is cleared only by software. Software can also set or clear this bit.
6	EXF2	Timer 2 External Flag: A negative transition on the T2EX pin (P1.1) or timer 2 overflow will cause this flag to set based on the CP / $\overline{RL2}$, EXEN2 and DCEN bits. If set by a negative transition, this flag must be cleared by software. Setting this bit in software or detection of a negative transition on T2EX pin will force a timer interrupt if enabled.
5	RCLK	Receive Clock Flag: This bit determines the serial port time-base when receiving data in serial modes 1 or 3. If it is 0, then timer 1 overflow is used for baud rate generation, otherwise timer 2 overflow is used. Setting this bit forces timer 2 in baud rate generator mode.

4	TCLK	Transmit Clock Flag: This bit determines the serial port time-base when transmitting data in modes 1 and 3. If it is set to 0, the timer 1 overflow is used to generate the baud rate clock otherwise timer 2 overflow is used. Setting this bit forces timer 2 in baud rate generator mode.
3	EXEN2	Timer 2 External Enable. This bit enables the capture/reload function on the T2EX pin if Timer 2 is not generating baud clocks for the serial port. If this bit is 0, then the T2EX pin will be ignored, otherwise a negative transition detected on the T2EX pin will result in capture or reload.
2	TR2	Timer 2 Run Control: This bit enables/disables the operation of timer 2. Halting this will preserve the current count in TH2, TL2.
1	C/$\overline{T2}$	Counter/Timer Select. This bit determines whether timer 2 will function as a timer or a counter. Independent of this bit, the timer will run at 2 clocks per tick when used in baud rate generator mode. If it is set to 0, then timer 2 operates as a timer at a speed depending on T2M bit (CKCON.5), otherwise it will count negative edges on T2 pin.
0	CP/$\overline{RL2}$	Compare/Reload Select: This bit determines whether the capture or reload function will be used for timer 2. If either RCLK or TCLK is set, this bit will be ignored and the timer will function in an auto-reload mode following each overflow. If the bit is 0 then auto-reload will occur when timer 2 overflows or a falling edge is detected on T2EX pin if EXEN2 = 1. If this bit is 1, then timer 2 captures will occur when a falling edge is detected on T2EX pin if EXEN2 = 1.

TIMER 2 MODE CONTROL

Bit:	7	6	5	4	3	2	1	0
	-	-	-	ICEN0	T2CR	1	T2OE	DCEN

Mnemonic: T2MOD Address: C9h

BIT	NAME	FUNCTION
7~5	-	Reserved.
4	ICEN0	External input capture 0 enable: This bit enables input capture 0 on T0 pin.
3	T2CR	Timer 2 Capture Reset: In the Timer 2 Capture Mode this bit enables/disables hardware automatically reset timer 2 while the value in TL2 and TH2 have been transferred into the capture register.
2	-	Must be 1.
1	T2OE	Timer 2 Output Enable. This bit enables/disables the Timer 2 clock out function.
0	DCEN	Down Count Enable: This bit, in conjunction with the T2EX pin, controls the direction that timer 2 counts in 16-bit auto-reload mode.

TIMER 2 CAPTURE LSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2L.	RCAP2L.	RCAP2L.	RCAP2L.	RCAP2L.	RCAP2L.	RCAP2L.	RCAP2L.

7	6	5	4	3	2	1	0

Mnemonic: RCAP2L Address: CAh

BIT	NAME	FUNCTION
7-0	RCAP2L	Timer 2 Capture LSB: This register is used to capture the TL2 value when a timer 2 is configured in capture mode.RCAP2L is also used as the LSB of a 16-bit reload value when timer 2 is configured in auto-reload mode.

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TIMER 2 CAPTURE MSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0

Mnemonic: RCAP2H Address: CBh

BIT	NAME	FUNCTION
7-0	RCAP2H	Timer 2 Capture MSB: This register is used to capture the TH2 value when a timer 2 is configured in capture mode. RCAP2H is also used as the MSB of a 16-bit reload value when timer 2 is configured in auto-reload mode.

TIMER 2 LSB

Bit:	7	6	5	4	3	2	1	0
	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0

Mnemonic: TL2 Address: CCh

BIT	NAME	FUNCTION
7-0	TL2	Timer 2 LSB.

TIMER 2 MSB

Bit:	7	6	5	4	3	2	1	0
	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0

Mnemonic: TH2 Address: CDh

BIT	NAME	FUNCTION
7-0	TL2	Timer 2 LSB.

NVM CONTROL

Bit:	7	6	5	4	3	2	1	0
	EER	EWR	EnNVM	-	-	-	-	-

Mnemonic: NVMCON Address: CEh

BIT	NAME	FUNCTION
7	EER	NVM page(n) erase bit: 0: Without erase NVM page(n). 1: Set this bit to erase page(n) of NVM. The NVM has **8** pages and each page have 16 bytes data memory. Initiate page select by programming NVMADDL registers, which will automatically enable page area. When user set this bit, the page erase process will begin and program counter will halt at this instruction. After the erase process is completed, program counter will continue executing next instruction.
6	EWR	NVM data write bit: 0: Without write NVM data.

		1: Set this bit to write NVM bytes and program counter will halt at this instruction. After write is finished, program counter will kept next instruction then executed.
5	EnNVM	To enable read NVM data memory area. 0: To disable the MOVX instruction to read NVM data memory. 1: To enable the MOVX instruction to read NVM data memory, the External RAM or AUX-RAM will be disabled.
4-0	-	Reserved

NVM DATA

Bit:	7	6	5	4	3	2	1	0
	NVMDAT.7	NVMDAT.6	NVMDAT.5	NVMDAT.4	NVMDAT3	NVMDAT.2	NVMDAT.1	NVMDAT.0

Mnemonic: NVMDATA Address: CFh

BIT	NAME	FUNCTION
7~0	NVMDAT.[7:0]	The NVM data write register. The read NVM data is by MOVC instruction.

PROGRAM STATUS WORD

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW Address: D0h

BIT	NAME	FUNCTION
7	CY	Carry flag: Set for an arithmetic operation which results in a carry being generated from the ALU. It is also used as the accumulator for the bit operations.
6	AC	Auxiliary carry: Set when the previous operation resulted in a carry from the high order nibble.
5	F0	User flag 0: The General purpose flag that can be set or cleared by the user.
4~3	RS1~RS0	Register bank select bits.
2	OV	Overflow flag: Set when a carry was generated from the seventh bit but not from the 8th bit as a result of the previous operation, or vice-versa.
1	F1	User Flag 1: The General purpose flag that can be set or cleared by the user software.
0	P	Parity flag: Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.

RS.1-0: Register Bank Selection Bits:

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

PWM CONTROL REGISTER 3

Bit:	7	6	5	4	3	2	1	0
	-	-	PWM1OE	PWM0OE	PCLK.1	PCLK.0	FP1	FP0

Mnemonic: PWMCON3 Address: D7h

BIT	NAME	FUNCTION
7~6	-	Reserved.
5	PWM1OE	PWM1 output enable bit. 0: PWM1 output disabled. 1: PWM1 output enabled.
4	PWM0OE	PWM0 output enable bit. 0: PWM0 output disabled. 1: PWM0 output enabled.
3~2	PCLK.1~0	PWM clock source selection bits, see below table. PCLK[1:0] / PWM clock source 00 / Fosc 01 / Timer 0 overflow 10 / Timer 1 overflow 11 / Reserved
1~0	FP1~0	Select PWM frequency pre-scale select bits, see belowtable. FP[1:0] / Fpwm 00 / F_{PCLK}/1 (default) 01 / F_{PCLK}/2 10 / F_{PCLK}/4 11 / F_{PCLK}/8

WATCHDOG CONTROL

Bit:	7	6	5	4	3	2	1	0
	WDRUN	POR	-	-	WDIF	WTRF	EWRST	WDCLR

Mnemonic: WDCON Address: D8h

BIT	NAME	FUNCTION

7	WDRUN	0: The Watchdog is stopped. 1: The Watchdog is running.
6	POR	Power-on reset flag. Hardware will set this flag on a power up condition. This flag can be read or written by software. A write by software is the only way to clear this bit once it is set.
5~4	-	Reserved.
3	WDIF	Watchdog Timer Interrupt flag: 0: If the interrupt is not enabled, then this bit indicates that the time-out period has elapsed. This bit must be cleared by software. 1: If the watchdog interrupt is enabled, hardware will set this bit to indicate that the watchdog interrupt has occurred.
2	WTRF	Watchdog Timer Reset flag: 1: Hardware will set this bit when the watchdog timer causes a reset. Software can read it but must clear it manually. A power-fail reset will also clear the bit. This bit helps software in determining the cause of a reset. If EWRST = 0, the watchdog timer will have no affect on this bit.
1	EWRST	0: Disable Watchdog Timer Reset. 1: Enable Watchdog Timer Reset.
0	WDCLR	Reset Watchdog Timer: This bit helps in putting the watchdog timer into a know state. It also helps in resetting the watchdog timer before a time-out occurs. Failing to set the EWRST before time-out will cause an interrupt (if EWDI (EIE.4) is set), and 512 clocks after that a watchdog timer reset will be generated (if EWRST is set). This bit is self-clearing by hardware.

The WDCON SFR is set to a 01xx0000B on a power-on-reset. WTRF (WDCON.2) is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF (WDCON.2) is not altered by an external reset. EWRST (WDCON.1) is set to 0 on all resets.

All the bits in this SFR have unrestricted read access. WDRUN, POR, EWRST, WDIF and WDCLR require Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

```
TA      REG     C7H
WDCON   REG     D8H
MOV     TA, #AAH            ; To access protected bits
MOV     TA, #55H
SETB    WDCON.0             ; Reset watchdog timer
ORL     WDCON, #00110000B   ; Select 26 bits watchdog timer
MOV     TA, #AAH
MOV     TA, #55H
ORL     WDCON, #10000010B   ; Enable watchdog
```

PWM 0 LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0

PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0

Mnemonic: PWM0L Address: DAh

BIT	NAME	FUNCTION
7~0	PWM0	PWM 0 Low Bits Register.

PWM 0 LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0

Mnemonic: PWM1L Address: DBh

BIT	NAME	FUNCTION
7~0	PWM1	PWM 1 Low Bits Register.

PWM CONTROL REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	PWMRUN	-	-	CLRPWM	-	-	-	-

Mnemonic: PWMCON1 Address: DCh

BIT	NAME	FUNCTION
7	PWMRUN	0: The PWM is not running. 1: The PWM counter is running.
6~5	-	Reserved.
4	CLRPWM	1: Clear 8-bit PWM counter to 000H. It is automatically cleared by hardware.
3~0	-	Reserved.

ACCUMULATOR

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

BIT	NAME	FUNCTION
7-0	ACC	The A or ACC register is the standard 8052 accumulator.

INPUT CAPTURE 0 LOW REGISTER

Bit:	7	6	5	4	3	2	1	0
	CCL0.7	CCL0.6	CCL0.5	CCL0.4	CCL0.3	CCL0.2	CCL0.1	CCL0.0

Mnemonic: CCL0 Address: E4h

BIT	NAME	FUNCTION
7-0	CCL0	Capture 0 low byte.

INPUT CAPTURE 0 HIGH REGISTER

Bit:	7	6	5	4	3	2	1	0
	CCH0.7	CCH0.6	CCH0.5	CCH0.4	CCH0.3	CCH0.2	CCH0.1	CCH0.0

Mnemonic: CCH0 Address: E4h

BIT	NAME	FUNCTION
7-0	CCH0	Capture 0 high byte.

IINTERRUPT ENABLE REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	ECPTF	EBO	-	EWDI	-	-	EKB	EI2

Mnemonic: EIE Address: E8h

BIT	NAME	FUNCTION
7	ECPTF	0: Disable capture interrupt. 1: Enable capture interrupt.
6	EBO	Enable brownout interrupt. 0: Disable brownout interrupt. 1: Enable brownout interrupt.
5	-	Reserved.
4	EWDI	0: Disable Watchdog Timer Interrupt. 1: Enable Watchdog Timer Interrupt.
3~2	–	Reserved.
1	EKB	0: Disable Keypad Interrupt. 1: Enable Keypad Interrupt.
0	EI2	0: Disable I2C Interrupt. 1: Enable I2C Interrupt.

KEYBOARD LEVEL

Bit:	7	6	5	4	3	2	1	0
	KBL.7	KBL.6	KBL.5	KBL.4	KBL.3	KBL.2	KBL.1	KBL.0

Mnemonic: KBL Address: E9h

BIT	NAME	FUNCTION
7~0	KBL.7~0	Keyboard trigger level. 0: Low level trigger.x pin. 1: High level trigger on KBI.x pin. [x = 0-7]

PORTS SHMITT REGISTER

Bit:	7	6	5	4	3	2	1	0

-	-	P5S	-	P3S	P2S	P1S	P0S

Mnemonic: PORTS Address: ECh

BIT	NAME	FUNCTION
7~6	-	Reserved.
5	P5S	1: Enables Schmitt trigger inputs on Port 5.
4	-	Reserved.
3	P3S	1: Enables Schmitt trigger inputs on Port 3.
2	P2S	1: Enables Schmitt trigger inputs on Port 2.
1	P1S	1: Enables Schmitt trigger inputs on Port 1.
0	P0S	1: Enables Schmitt trigger inputs on Port 0.

PORT 5 OUTPUT MODE 1

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	ENCLK	P5M1.1	P5M1.0

Mnemonic: P5M1 Address: EDh

BIT	NAME	FUNCTION
7~3	-	Reserved.
2	ENCLK	1: Enabled clock output to XTAL2 pin (P5.0).
1~0	P5M1.1~0	To control the output configuration of P5 bits [1:0].

PORT 5 OUTPUT MODE 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	P5M2.1	P5M2.0

Mnemonic: P5M2 Address: EEh

BIT	NAME	FUNCTION
7~2	-	Reserved.
1~0	P5M2.1~0	To control the output configuration of P5 bits [1:0].

B REGISTER

Bit:	7	6	5	4	3	2	1	0
	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0

Mnemonic: B Address: F0h

BIT	NAME	FUNCTION
7-0	B	The B register is the standard 8052 register that serves as a second accumulator.

INTERRUPT HIGH PRIORITY 1

Bit:	7	6	5	4	3	2	1	0

PCAPH	PBOH	-	PWDIH	-	-	PKBH	PI2H

Mnemonic: IP1H Address: F7h

BIT	NAME	FUNCTION
7	PCAPH	1: To set interrupt high priority of Input Capture 0 as highest priority level.
6	PBOH	1: To set interrupt high priority of Brownout is highest priority level.
5	-	Reserved.
4	PWDIH	1: To set interrupt high priority of Watchdog is highest priority level.
3~2	-	Reserved.
1	PKBH	1: To set interrupt high priority of Keypad is highest priority level.
0	PI2H	1: To set interrupt high priority of I2C is highest priority level.

INTERRUPT PRIORITY 1

Bit: 7 6 5 4 3 2 1 0

PCAP	PBO	-	PWDI	-	-	PKB	PI2

Mnemonic: IP1 Address: F8h

BIT	NAME	FUNCTION
7	PCAP	1: To set interrupt priority of Input Capture 0 as higher priority level.
6	PBO	1: To set interrupt priority of Brownout is higher priority level.
5	-	Reserved.
4	PWDI	1: To set interrupt priority of Watchdog is higher priority level.
3~2	-	Reserved.
1	PKB	1: To set interrupt priority of Keypad is higher priority level.
0	PI2	1: To set interrupt priority of I2C is higher priority level.

9. INSTRUCTION

The N79E352(R) executes all the instructions of the standard 8052 family. The operation of these instructions, their effect on the flag bits and the status bits is exactly the same. However, timing of these instructions is different. The reason for this is two fold. Firstly, in the N79E352(R), each machine cycle consists of 4 clock periods, while in the standard 8052 it consists of 12 clock periods. Also, in the N79E352(R) there is only one fetch per machine cycle i.e. 4 clocks per fetch, while in the standard 8052 there can be two fetches per machine cycle, which works out to 6 clocks per fetch.

The advantage the N79E352(R) has is that since there is only one fetch per machine cycle, the number of machine cycles in most cases is equal to the number of operands that the instruction has. In case of jumps and calls there will be an additional cycle that will be needed to calculate the new address. But overall the N79E352(R) reduces the number of dummy fetches and wasted cycles, thereby improving efficiency as compared to the standard 8052.

Table 9-1: Instructions that affect Flag settings

Instruction	Carry	Overflow	Auxiliary Carry	Instruction	Carry	Overflow	Auxiliary Carry
ADD	X	X	X	CLR C	0		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C, bit	X		
MUL	0	X		ANL C, bit	X		
DIV	0	X		ORL C, bit	X		
DA A	X			ORL C, bit	X		
RRC A	X			MOV C, bit	X		
RLC A	X			CJNE	X		
SETB C	1						

A "X" indicates that the modification is as per the result of instruction.

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Table 9-2: Instruction Timing for N79E352(R)

Instruction	HEX Op-Code	Bytes	N79E352(R) Machine Cycles	N79E352(R) Clock Cycles	8052 Clock Cycles	N79E352(R) vs. 8052 Speed Ratio
NOP	00	1	1	4	12	3
ADD A, R0	28	1	1	4	12	3
ADD A, R1	29	1	1	4	12	3
ADD A, R2	2A	1	1	4	12	3
ADD A, R3	2B	1	1	4	12	3
ADD A, R4	2C	1	1	4	12	3
ADD A, R5	2D	1	1	4	12	3
ADD A, R6	2E	1	1	4	12	3
ADD A, R7	2F	1	1	4	12	3
ADD A, @R0	26	1	1	4	12	3
ADD A, @R1	27	1	1	4	12	3
ADD A, direct	25	2	2	8	12	1.5
ADD A, #data	24	2	2	8	12	1.5

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Instruction Timing for N79E352(R), continued

Instruction	HEX Op-Code	Bytes	N79E352(R) Machine Cycles	N79E352(R) Clock Cycles	8052 Clock Cycles	N79E352(R) vs. 8052 Speed Ratio
ADDC A, R0	38	1	1	4	12	3
ADDC A, R1	39	1	1	4	12	3
ADDC A, R2	3A	1	1	4	12	3
ADDC A, R3	3B	1	1	4	12	3
ADDC A, R4	3C	1	1	4	12	3
ADDC A, R5	3D	1	1	4	12	3
ADDC A, R6	3E	1	1	4	12	3
ADDC A, R7	3F	1	1	4	12	3
ADDC A, @R0	36	1	1	4	12	3
ADDC A, @R1	37	1	1	4	12	3
ADDC A, direct	35	2	2	8	12	1.5
ADDC A, #data	34	2	2	8	12	1.5
ACALL addr11	71, 91, B1, 11, 31, 51, D1, F1	2	3	12	24	2
AJMP ADDR11	01, 21, 41, 61, 81, A1, C1, E1	2	3	12	24	2
ANL A, R0	58	1	1	4	12	3
ANL A, R1	59	1	1	4	12	3
ANL A, R2	5A	1	1	4	12	3
ANL A, R3	5B	1	1	4	12	3
ANL A, R4	5C	1	1	4	12	3
ANL A, R5	5D	1	1	4	12	3
ANL A, R6	5E	1	1	4	12	3
ANL A, R7	5F	1	1	4	12	3
ANL A, @R0	56	1	1	4	12	3
ANL A, @R1	57	1	1	4	12	3
ANL A, direct	55	2	2	8	12	1.5
ANL A, #data	54	2	2	8	12	1.5
ANL direct, A	52	2	2	8	12	1.5
ANL direct, #data	53	3	3	12	24	2
ANL C, bit	82	2	2	8	24	3
ANL C, /bit	B0	2	2	8	24	3
CJNE A, direct, rel	B5	3	4	16	24	1.5
CJNE A, #data, rel	B4	3	4	16	24	1.5
CJNE @R0, #data, rel	B6	3	4	16	24	1.5
CJNE @R1, #data, rel	B7	3	4	16	24	1.5
CJNE R0, #data, rel	B8	3	4	16	24	1.5
CJNE R1, #data, rel	B9	3	4	16	24	1.5
CJNE R2, #data, rel	BA	3	4	16	24	1.5
CJNE R3, #data, rel	BB	3	4	16	24	1.5
CJNE R4, #data, rel	BC	3	4	16	24	1.5
CJNE R5, #data, rel	BD	3	4	16	24	1.5
CJNE R6, #data, rel	BE	3	4	16	24	1.5

Instruction Timing for N79E352(R), continued

Instruction	HEX Op-Code	Bytes	N79E352(R) Machine Cycles	N79E352(R) Clock Cycles	8052 Clock Cycles	N79E352(R) vs. 8052 Speed Ratio
CLR A	E4	1	1	4	12	3
CPL A	F4	1	1	4	12	3
CLR C	C3	1	1	4	12	3
CLR bit	C2	2	2	8	12	1.5
CPL C	B3	1	1	4	12	3
CPL bit	B2	2	2	8	12	1.5
DEC A	14	1	1	4	12	3
DEC R0	18	1	1	4	12	3
DEC R1	19	1	1	4	12	3
DEC R2	1A	1	1	4	12	3
DEC R3	1B	1	1	4	12	3
DEC R4	1C	1	1	4	12	3
DEC R5	1D	1	1	4	12	3
DEC R6	1E	1	1	4	12	3
DEC R7	1F	1	1	4	12	3
DEC @R0	16	1	1	4	12	3
DEC @R1	17	1	1	4	12	3
DEC direct	15	2	2	8	12	1.5
DEC DPTR	A5	1	2	8	-	-
DIV AB	84	1	5	20	48	2.4
DA A	D4	1	1	4	12	3
DJNZ R0, rel	D8	2	3	12	24	2
DJNZ R1, rel	D9	2	3	12	24	2
DJNZ R5, rel	DD	2	3	12	24	2
DJNZ R2, rel	DA	2	3	12	24	2
DJNZ R3, rel	DB	2	3	12	24	2
DJNZ R4, rel	DC	2	3	12	24	2
DJNZ R6, rel	DE	2	3	12	24	2
DJNZ R7, rel	DF	2	3	12	24	2
DJNZ direct, rel	D5	3	4	16	24	1.5
INC A	04	1	1	4	12	3
INC R0	08	1	1	4	12	3
INC R1	09	1	1	4	12	3
INC R2	0A	1	1	4	12	3
INC R3	0B	1	1	4	12	3
INC R4	0C	1	1	4	12	3

Instruction Timing for N79E352(R), continued

Instruction	HEX Op-Code	Bytes	N79E352(R) Machine Cycles	N79E352(R) Clock Cycles	8052 Clock Cycles	N79E352(R) vs. 8052 Speed Ratio
INC R6	0E	1	1	4	12	3
INC R7	0F	1	1	4	12	3
INC @R0	06	1	1	4	12	3
INC @R1	07	1	1	4	12	3
INC direct	05	2	2	8	12	1.5
INC DPTR	A3	1	2	8	24	3
JMP @A+DPTR	73	1	2	8	24	3
JZ rel	60	2	3	12	24	2
JNZ rel	70	2	3	12	24	2
JC rel	40	2	3	12	24	2
JNC rel	50	2	3	12	24	2
JB bit, rel	20	3	4	16	24	1.5
JNB bit, rel	30	3	4	16	24	1.5
JBC bit, rel	10	3	4	16	24	1.5
LCALL addr16	12	3	4	16	24	1.5
LJMP addr16	02	3	4	16	24	1.5
MUL AB	A4	1	5	20	48	2.4
MOV A, R0	E8	1	1	4	12	3
MOV A, R1	E9	1	1	4	12	3
MOV A, R2	EA	1	1	4	12	3
MOV A, R3	EB	1	1	4	12	3
MOV A, R4	EC	1	1	4	12	3
MOV A, R5	ED	1	1	4	12	3
MOV A, R6	EE	1	1	4	12	3
MOV A, R7	EF	1	1	4	12	3
MOV A, @R0	E6	1	1	4	12	3
MOV A, @R1	E7	1	1	4	12	3
MOV A, direct	E5	2	2	8	12	1.5
MOV A, #data	74	2	2	8	12	1.5
MOV R0, A	F8	1	1	4	12	3
MOV R1, A	F9	1	1	4	12	3
MOV R2, A	FA	1	1	4	12	3
MOV R3, A	FB	1	1	4	12	3
MOV R4, A	FC	1	1	4	12	3
MOV R5, A	FD	1	1	4	12	3
MOV R6, A	FE	1	1	4	12	3
MOV R7, A	FF	1	1	4	12	3

Instruction Timing for N79E352(R), continued

Instruction	HEX Op-Code	Bytes	N79E352(R) Machine Cycles	N79E352(R) Clock Cycles	8052 Clock Cycles	N79E352(R) vs. 8052 Speed Ratio
MOV R1, direct	A9	2	2	8	12	1.5
MOV R2, direct	AA	2	2	8	12	1.5
MOV R3, direct	AB	2	2	8	12	1.5
MOV R4, direct	AC	2	2	8	12	1.5
MOV R5, direct	AD	2	2	8	12	1.5
MOV R6, direct	AE	2	2	8	12	1.5
MOV R7, direct	AF	2	2	8	12	1.5
MOV R0, #data	78	2	2	8	12	1.5
MOV R1, #data	79	2	2	8	12	1.5
MOV R2, #data	7A	2	2	8	12	1.5
MOV R3, #data	7B	2	2	8	12	1.5
MOV R4, #data	7C	2	2	8	12	1.5
MOV R5, #data	7D	2	2	8	12	1.5
MOV R6, #data	7E	2	2	8	12	1.5
MOV R7, #data	7F	2	2	8	12	1.5
MOV @R0, A	F6	1	1	4	12	3
MOV @R1, A	F7	1	1	4	12	3
MOV @R0, direct	A6	2	2	8	12	1.5
MOV @R1, direct	A7	2	2	8	12	1.5
MOV @R0, #data	76	2	2	8	12	1.5
MOV @R1, #data	77	2	2	8	12	1.5
MOV direct, A	F5	2	2	8	12	1.5
MOV direct, R0	88	2	2	8	12	1.5
MOV direct, R1	89	2	2	8	12	1.5
MOV direct, R2	8A	2	2	8	12	1.5
MOV direct, R3	8B	2	2	8	12	1.5
MOV direct, R4	8C	2	2	8	12	1.5
MOV direct, R5	8D	2	2	8	12	1.5
MOV direct, R6	8E	2	2	8	12	1.5
MOV direct, R7	8F	2	2	8	12	1.5
MOV direct, @R0	86	2	2	8	12	1.5
MOV direct, @R1	87	2	2	8	12	1.5
MOV direct, direct	85	3	3	12	24	2
MOV direct, #data	75	3	3	12	24	2
MOV DPTR, #data 16	90	3	3	12	24	2
MOVC A, @A+DPTR	93	1	2	8	24	3

Instruction Timing for N79E352(R), continued

Instruction	HEX Op-Code	Bytes	N79E352(R) Machine Cycles	N79E352(R) Clock Cycles	8052 Clock Cycles	N79E352(R) vs. 8052 Speed Ratio
MOVX A, @R0	E2	1	2 - 9	8 - 36	24	3 - 0.66
MOVX A, @R1	E3	1	2 - 9	8 - 36	24	3 - 0.66
MOVX A, @DPTR	E0	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @R0, A	F2	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @R1, A	F3	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @DPTR, A	F0	1	2 - 9	8 - 36	24	3 - 0.66
MOV C, bit	A2	2	2	8	12	1.5
MOV bit, C	92	2	2	8	24	3
ORL A, R0	48	1	1	4	12	3
ORL A, R1	49	1	1	4	12	3
ORL A, R2	4A	1	1	4	12	3
ORL A, R3	4B	1	1	4	12	3
ORL A, R4	4C	1	1	4	12	3
ORL A, R5	4D	1	1	4	12	3
ORL A, R6	4E	1	1	4	12	3
ORL A, R7	4F	1	1	4	12	3
ORL A, @R0	46	1	1	4	12	3
ORL A, @R1	47	1	1	4	12	3
ORL A, direct	45	2	2	8	12	1.5
ORL A, #data	44	2	2	8	12	1.5
ORL direct, A	42	2	2	8	12	1.5
ORL direct, #data	43	3	3	12	24	2
ORL C, bit	72	2	2	8	24	3
ORL C, /bit	A0	2	2	6	24	3
PUSH direct	C0	2	2	8	24	3
POP direct	D0	2	2	8	24	3
RET	22	1	2	8	24	3
RETI	32	1	2	8	24	3
RL A	23	1	1	4	12	3
RLC A	33	1	1	4	12	3
RR A	03	1	1	4	12	3
RRC A	13	1	1	4	12	3
SETB C	D3	1	1	4	12	3
SETB bit	D2	2	2	8	12	1.5
SWAP A	C4	1	1	4	12	3
SJMP rel	80	2	3	12	24	2
SUBB A, R0	98	1	1	4	12	3

Instruction Timing for N79E352(R), continued

Instruction	HEX Op-Code	Bytes	N79E352(R) Machine Cycles	N79E352(R) Clock Cycles	8052 Clock Cycles	N79E352(R) vs. 8052 Speed Ratio
SUBB A, R2	9A	1	1	4	12	3
SUBB A, R3	9B	1	1	4	12	3
SUBB A, R4	9C	1	1	4	12	3
SUBB A, R5	9D	1	1	4	12	3
SUBB A, R6	9E	1	1	4	12	3
SUBB A, R7	9F	1	1	4	12	3
SUBB A, @R0	96	1	1	4	12	3
SUBB A, @R1	97	1	1	4	12	3
SUBB A, direct	95	2	2	8	12	1.5
SUBB A, #data	94	2	2	8	12	1.5
XCH A, R0	C8	1	1	4	12	3
XCH A, R1	C9	1	1	4	12	3
XCH A, R2	CA	1	1	4	12	3
XCH A, R3	CB	1	1	4	12	3
XCH A, R4	CC	1	1	4	12	3
XCH A, R5	CD	1	1	4	12	3
XCH A, R6	CE	1	1	4	12	3
XCH A, R7	CF	1	1	4	12	3
XCH A, @R0	C6	1	1	4	12	3
XCH A, @R1	C7	1	1	4	12	3
XCHD A, @R0	D6	1	1	4	12	3
XCHD A, @R1	D7	1	1	4	12	3
XCH A, direct	C5	2	2	8	12	1.5
XRL A, R0	68	1	1	4	12	3
XRL A, R1	69	1	1	4	12	3
XRL A, R2	6A	1	1	4	12	3
XRL A, R3	6B	1	1	4	12	3
XRL A, R4	6C	1	1	4	12	3
XRL A, R5	6D	1	1	4	12	3
XRL A, R6	6E	1	1	4	12	3
XRL A, R7	6F	1	1	4	12	3
XRL A, @R0	66	1	1	4	12	3
XRL A, @R1	67	1	1	4	12	3
XRL A, direct	65	2	2	8	12	1.5
XRL A, #data	64	2	2	8	12	1.5
XRL direct, A	62	2	2	8	12	1.5
XRL direct, #data	63	3	3	12	24	2

9.1 Instruction Timing

The instruction timing for the N79E352(R) is an important aspect, especially for those users who wish to use software instructions to generate timing delays. Also, it provides the user with an insight into the timing differences between the N79E352(R) and the standard 8052. In the N79E352(R) each machine cycle is four clock periods long. Each clock period is designated a state. Thus each machine cycle is made up of four states, C1, C2 C3 and C4, in that order. Due to the reduced time for each instruction execution, both the clock edges are used for internal timing. Hence it is important that the duty cycle of the clock be as close to 50% as possible to avoid timing conflicts. As mentioned earlier, the N79E352(R) does one op-code fetch per machine cycle. Therefore, in most of the instructions, the number of machine cycles needed to execute the instruction is equal to the number of bytes in the instruction. Of the 256 available op-codes, 128 of them are single cycle instructions. Thus more than half of all op-codes in the N79E352(R) are executed in just four clock periods. Most of the two-cycle instructions are those that have two byte instruction codes. However there are some instructions that have only one byte instructions, yet they are two cycle instructions. One instruction which is of importance is the MOVX instruction. In the standard 8052, the MOVX instruction is always two machine cycles long. However in the N79E352(R), the user has a facility to stretch the duration of this instruction from 2 machine cycles to 9 machine cycles. The $\overline{RD}$ and $\overline{WR}$ strobe lines are also proportionately elongated. This gives the user flexibility in accessing both fast and slow peripherals without the use of external circuitry and with minimum software overhead. The rest of the instructions are either three, four or five machine cycle instructions. Note that in the N79E352(R), based on the number of machine cycles, there are five different types, while in the standard 8052 there are only three. However, in the N79E352(R) each machine cycle is made of only 4 clock periods compared to the 12 clock periods for the standard 8052. Therefore, even though the number of categories has increased, each instruction is at least 1.5 to 3 times faster than the standard 8052 in terms of clock periods.

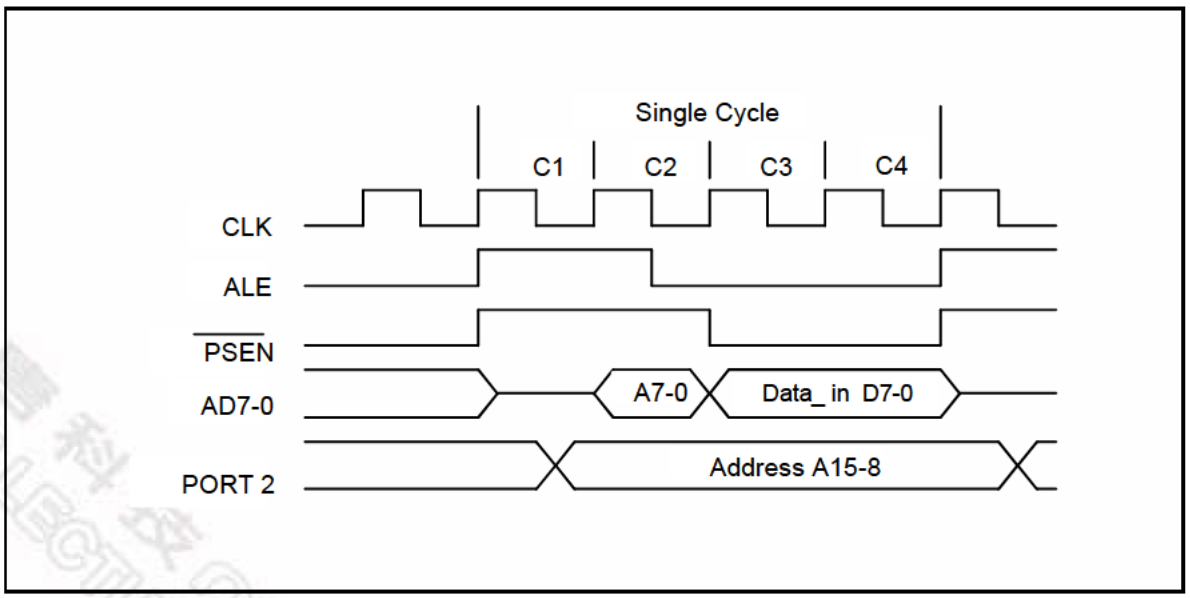


Figure 9-1: Single Cycle Instruction Timing

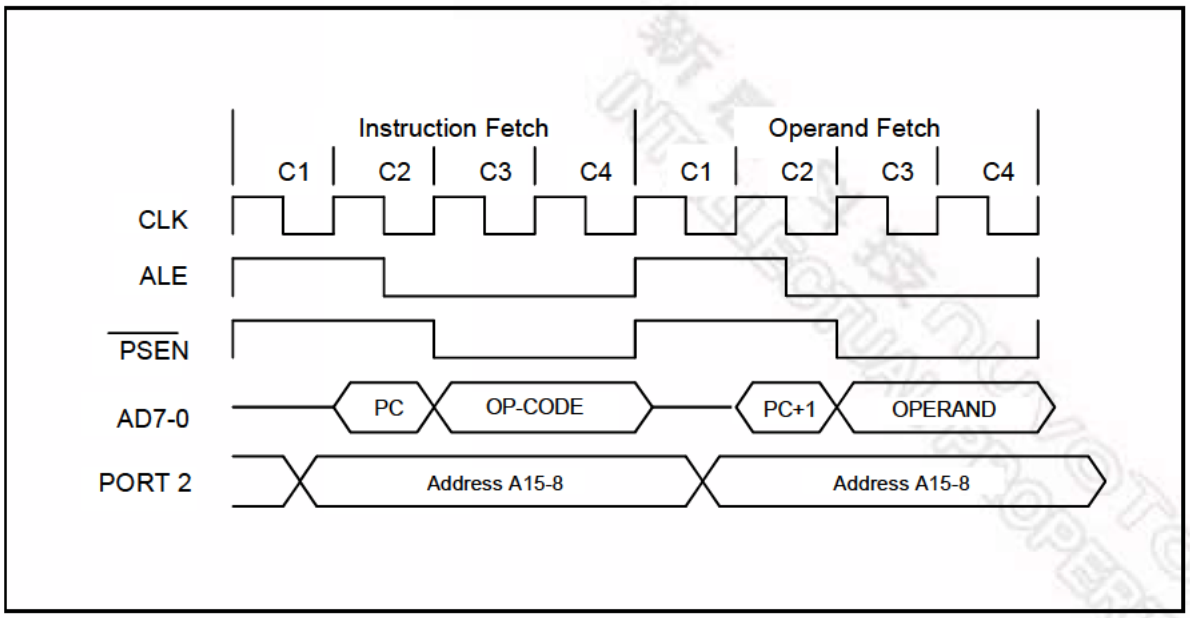


Figure 9-2: Two Cycle Instruction Timing

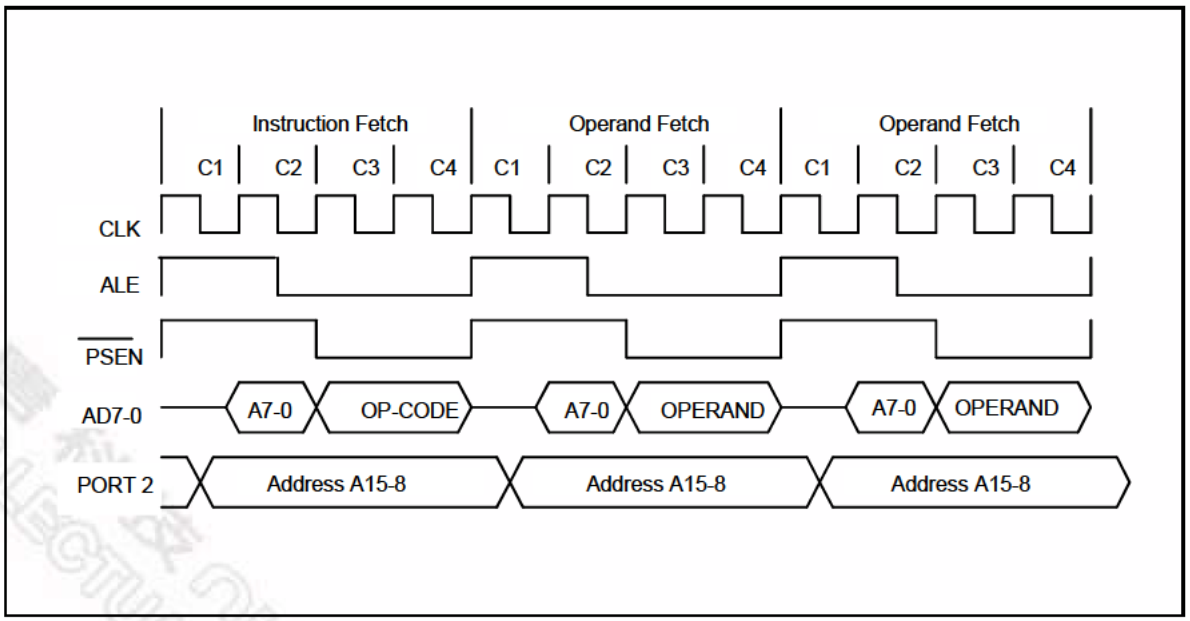


Figure 9-3: Three Cycle Instruction Timing

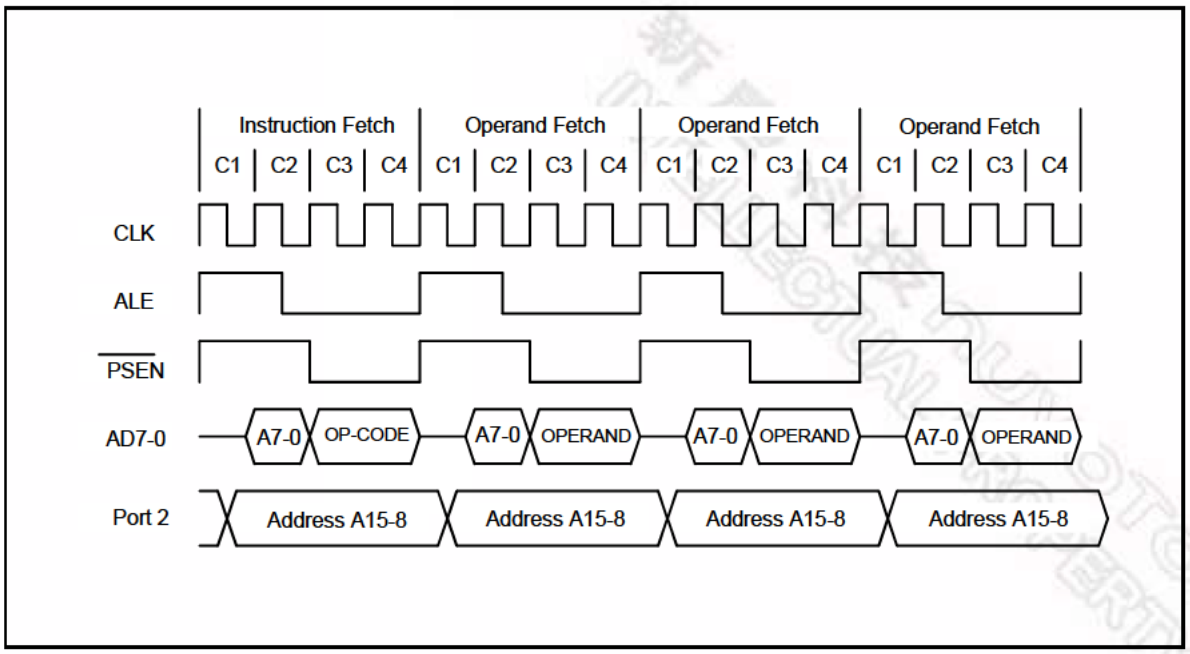


Figure 9-4: Four Cycle Instruction Timing

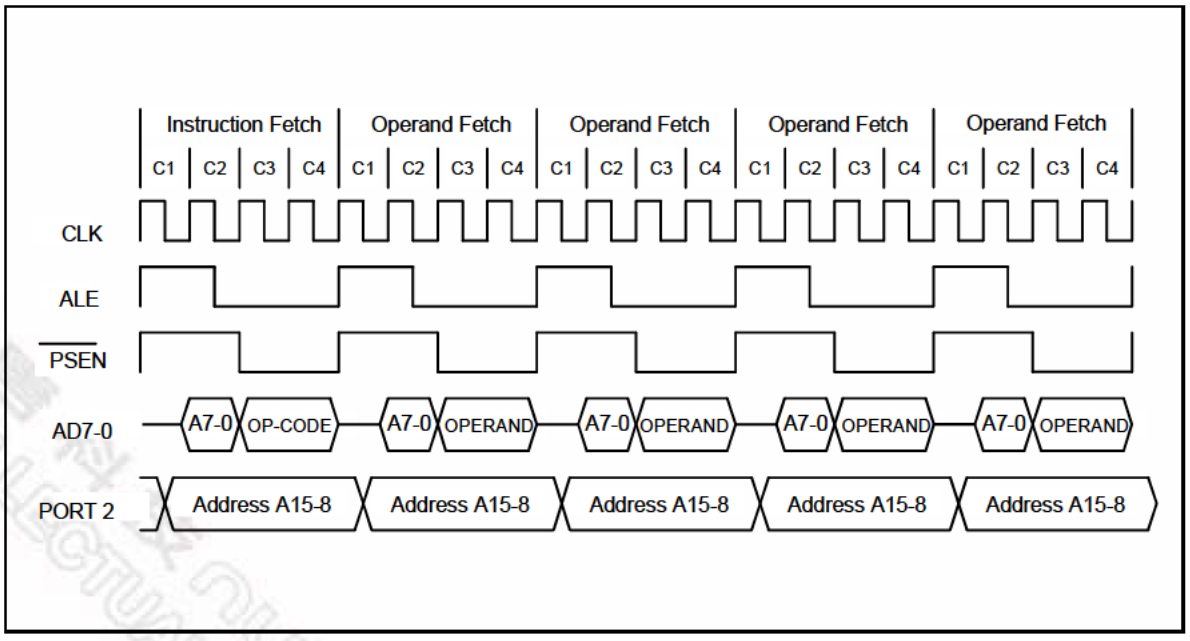


Figure 9-5: Five Cycle Instruction Timing

9.2 MOVX Instruction

The N79E352(R), like the standard 8052, uses the MOVX instruction to access external Data Memory. This Data Memory includes both off-chip memory as well as memory mapped peripherals. While the results of the MOVX instruction are the same as in the standard 8052, the operation and the timing of the strobe signals have been modified in order to give the user much greater flexibility.

The MOVX instruction is of two types, the MOVX @Ri and MOVX @DPTR. In the MOVX @Ri, the address of the external data comes from two sources. The lower 8-bits of the address are stored in the Ri register of the selected working register bank. The upper 8-bits of the address come from the port 2 SFR. In the MOVX @DPTR type, the full 16-bit address is supplied by the Data Pointer.

Since the N79E352(R) has two Data Pointers, DPTR and DPTR1, the user has to select between the two by setting or clearing the DPS bit. The Data Pointer Select bit (DPS) is the LSB of the DPS SFR, which exists at location 86h. No other bits in this SFR have any effect, and they are set to 0. When DPS is 0, then DPTR is selected, and when set to 1, DPTR1 is selected. The user can switch between DPTR and DPTR1 by toggling the DPS bit. The quickest way to do this is by the INC instruction. The advantage of having two Data Pointers is most obvious while performing block move operations. The accompanying code shows how the use of two separate Data Pointers speeds up the execution time for code performing the same task.

Block Move with single Data Pointer:

; SH and SL are the high and low bytes of Source Address
; DH and DL are the high and low bytes of Destination Address
; CNT is the number of bytes to be moved

			Machine Cycles of N79E352(R) #
MOV	R2, #CNT	; Load R2 with the count value	2
MOV	R3, #SL	; Save low byte of Source Address in R3	2
MOV	R4, #SH	; Save high byte of Source address in R4	2
MOV	R5, #DL	; Save low byte of Destination Address in R5	2
MOV	R6, #DH	; Save high byte of Destination address in R6	2
LOOP:			
MOV	DPL, R3	; Load DPL with low byte of Source address	2
MOV	DPH, R4	; Load DPH with high byte of Source address	2
MOVX	A, @DPTR	; Get byte from Source to Accumulator	2
INC	DPTR	; Increment Source Address to next byte	2
MOV	R3, DPL	; Save low byte of Source address in R3	2
MOV	R4, DPH	; Save high byte of Source Address in R4	2
MOV	DPL, R5	; Load low byte of Destination Address in DPL	2
MOV	DPH, R6	; Load high byte of Destination Address in DPH	2
MOVX	@DPTR, A	; Write data to destination	2
INC	DPTR	; Increment Destination Address	2
MOV	DPL, R5	; Save low byte of new destination address in R5	2
MOV	DPH, R6	; Save high byte of new destination address in R6	2
DJNZ	R2, LOOP	; Decrement count and do LOOP again if count <> 0	2

Machine cycles in standard 8052 = 10 + (26 * CNT)
Machine cycles in N79E352(R) = 10 + (26 * CNT)
If CNT = 50
Clock cycles in standard 8052= ((10 + (26 *50)) * 12 = (10 + 1300) * 12 = 15720
Clock cycles in N79E352(R) = ((10 + (26 * 50)) * 4 = (10 + 1300) * 4 = 5240

Block Move with Two Data Pointers in N79E352(R):

```
; SH and SL are the high and low bytes of Source Address
; DH and DL are the high and low bytes of Destination Address
; CNT is the number of bytes to be moved
```

			Machine Cycles of N79E352(R) #
MOV	R2, #CNT	; Load R2 with the count value	2
MOV	DPS, #00h	; Clear DPS to point to DPTR	2
MOV	DPTR, #DHDL	; Load DPTR with Destination address	3
INC	DPS	; Set DPS to point to DPTR1	2
MOV	DPTR, #SHSL	; Load DPTR1 with Source address	3
LOOP:			
MOVX	A, @DPTR	; Get data from Source block	2
INC	DPTR	; Increment source address	2
DEC	DPS	; Clear DPS to point to DPTR	2
MOVX	@DPTR, A	; Write data to Destination	2
INC	DPTR	; Increment destination address	2
INC	DPS	; Set DPS to point to DPTR1	2
DJNZ	R2, LOOP	; Check if all done	3

Machine cycles in N79E352(R) = 12 + (15 * CNT)
If CNT = 50
Clock cycles in N79E352(R) = (12 + (15 * 50)) * 4 = (12 + 750) * 4 = 3048

We can see that in the first program the standard 8052 takes 15720 cycles, while the N79E352(R) takes only 5240 cycles for the same code. In the second program, written for the N79E352(R), program execution requires only 3048 clock cycles. If the size of the block is increased then the saving is even greater.

9.3 External Data Memory Access Timing

The timing for the MOVX instruction is another feature of the N79E352(R). In the standard 8052, the MOVX instruction has a fixed execution time of 2 machine cycles. However in the N79E352(R), the duration of the access can be varied by the user.

The instruction starts off as a normal op-code fetch of 4 clocks. In the next machine cycle, the N79E352(R) puts out the address of the external Data Memory and the actual access occurs here. The user can change the duration of this access time by setting the STRETCH value. The Clock Control SFR (CKCON) has three bits that control the stretch value. These three bits are M2-0 (bits 2-0 of CKCON). These three bits give the user 8 different access time options. The stretch can be varied from 0 to 7, resulting in MOVX instructions that last from 2 to 9 machine cycles in length. Note that the stretching of the instruction only results in the elongation of the MOVX instruction, as if the state of the CPU was held for the desired period. There is no effect on any other instruction or its timing. By

default, the Stretch value is set at 1, giving a MOVX instruction of 3 machine cycles. If desired by the user the stretch value can be set to 0 to give the fastest MOVX instruction of only 2 machine cycles.

Table 9-3: Data Memory Cycle Stretch Values

M2	M1	M0	Machine Cycles	$\overline{RD}$ or $\overline{WR}$ strobe width in Clocks	$\overline{RD}$ or $\overline{WR}$ strobe width @ 20 MHz
0	0	0	2	2	100 nS
0	0	1	3 (default)	4	200 nS
0	1	0	4	8	400 nS
0	1	1	5	12	600 nS
1	0	0	6	16	800 nS
1	0	1	7	20	1000 nS
1	1	0	8	24	1200 nS
1	1	1	9	28	1400 nS

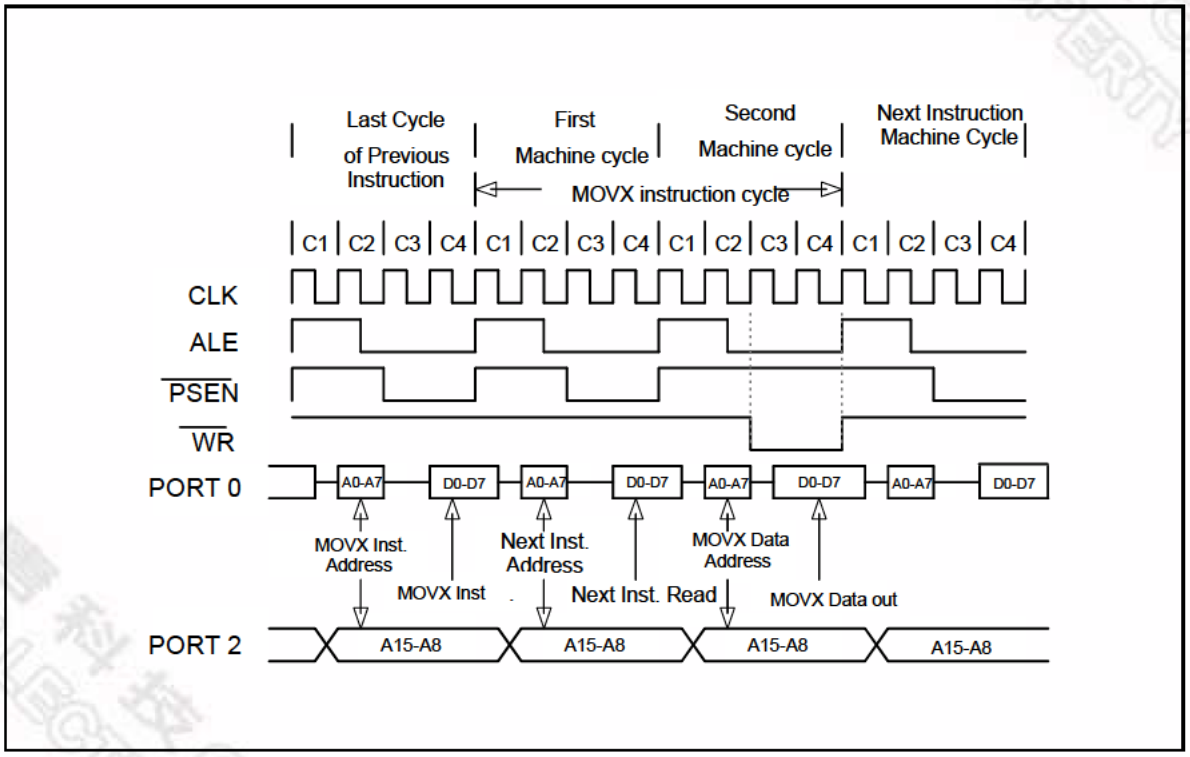


Figure 9-6: Data Memory Write with Stretch Value = 0

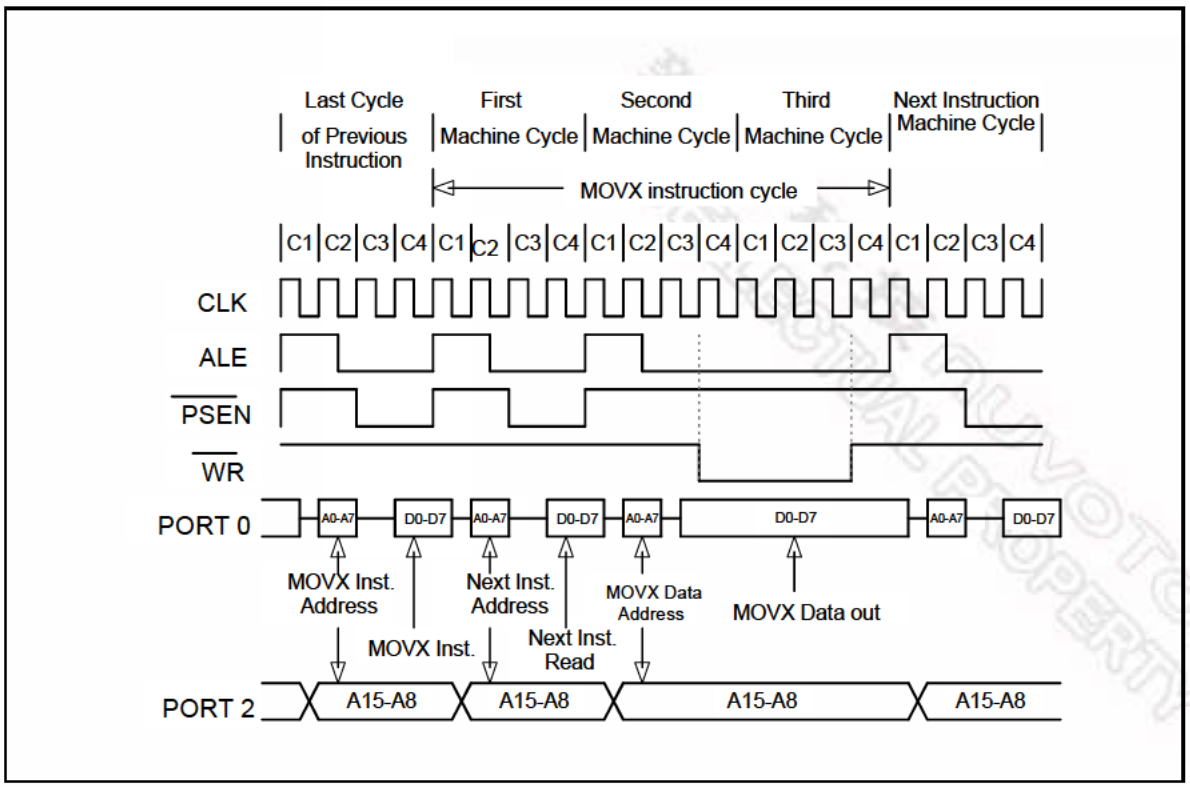


Figure 9-7: Data Memory Write with Stretch Value = 1

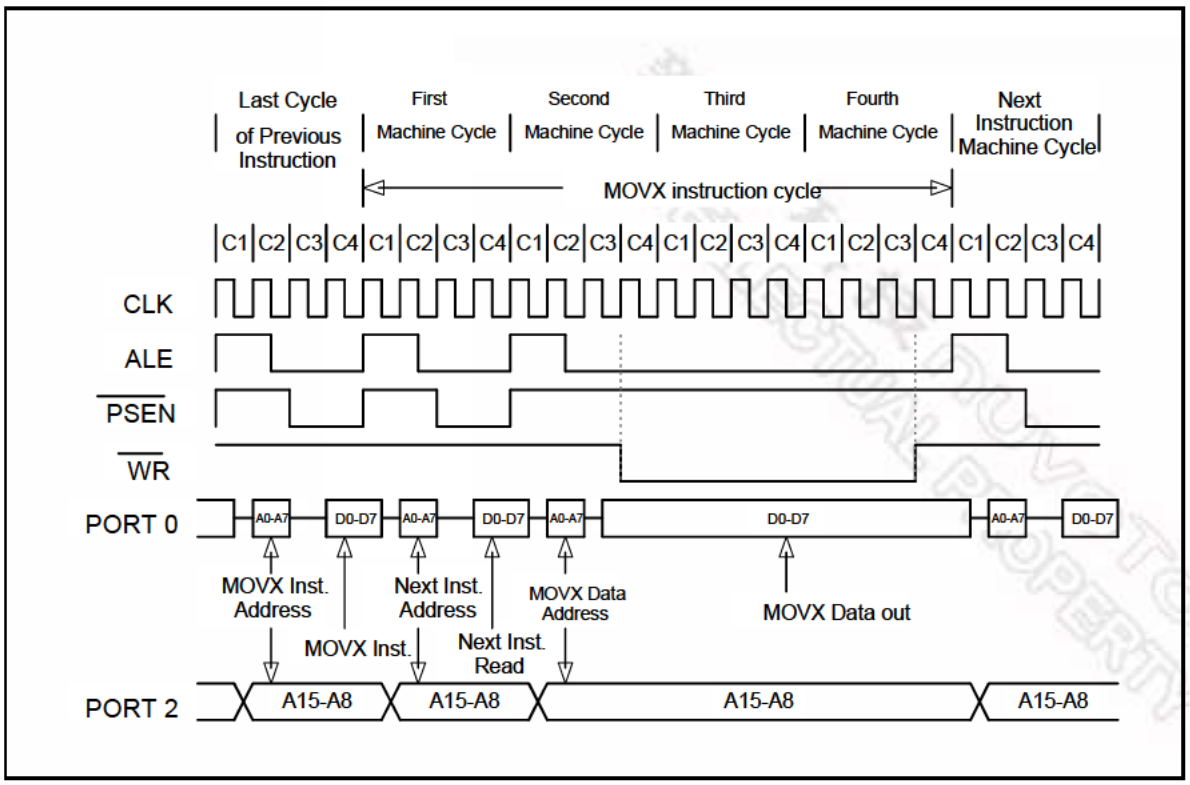


Figure 9-8: Data Memory Write with Stretch Value = 2

9.4 Wait State Control Signal

Either with the software using stretch value to change the required machine cycle of MOVX instruction, the N79E352(R) provides another hardware signal $\overline{\text{WAIT}}$ to implement the wider duration of external data access timing. This wait state control signal is the alternate function of P4.0. The wait state control signal can be enabled by setting WS (SFR ROMMAP.7) bit. When enabled, the setting of stretch value decides the minimum length of MOVX instruction cycle and the device will sample the $\overline{\text{WAIT}}$ pin at each C2 state before the rising edge of read/write strobe signal during MOVX instruction. Once this signal being recongnized, one more machine cycle (wait state cycle) will be inserted into next cycle. The inserted wait state cycles are unlimited, so the MOVX instruction cycle will end in which the wait state control signal is deactivated. Using wait state control signal allows a dynamically access timimg to a selected external peripheral. The WS bit is accessed by the Timed Access Protection procedure.

10. POWER MANAGEMENT

The N79E352(R) has several features that help the user to control the power consumption of the device. The power saving features are basically the POWER DOWN mode, ECONOMY mode and the IDLE mode of operation.

10.1 Idle Mode

The user can put the device into idle mode by writing 1 to the bit PCON.0. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle mode, the clock to the CPU is halted, but not to the Interrupt, Timer, Watchdog timer and Serial port blocks. This forces the CPU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The port pins hold the logical states they had at the time Idle was activated. The Idle mode can be terminated in two ways. Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the Idle bit, terminate the Idle mode, and the Interrupt Service Routine(ISR) will be executed. After the ISR, execution of the program will continue from the instruction which put the device into Idle mode.

The Idle mode can also be exited by activating the reset. The device can be put into reset either by applying a high on the external RST pin, a Power on reset condition or a Watchdog timer reset. The external reset pin has to be held high for at least two machine cycles i.e. 8 clock periods to be recognized as a valid reset. In the reset condition the program counter is reset to 0000h and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution starts immediately. In the Idle mode, the Watchdog timer continues to run, and if enabled, a time-out will cause a watchdog timer interrupt which will wake up the device. The software must reset the Watchdog timer in order to preempt the reset which will occur after 512 clock periods of the time-out. When the N79E352(R) is exiting from an Idle mode with a reset, the instruction following the one which put the device into Idle mode is not executed. So there is no danger of unexpected writes.

10.2 Economy Mode

The power consumption of microcontroller relates to operating frequency. The N79E352(R) offers a Economy mode to reduce the internal clock rate dynamically without external components. By default, one machine cycle needs 4 clocks. In Economy mode, software can select 4, 64 or 1024 clocks per machine cycle. It keeps the CPU operating at a acceptable speed but eliminates the power consumption. In the Idle mode, the clock of the core logic is stopped, but all clocked peripherals such as watchdog timer are still running at a rate of clock/4. In the Economy mode, all clocked peripherals run at the same reduced clocks rate as in core logic. So the Economy mode may provide a lower power consumption than idle mode.

Software invokes the Economy mode by setting the appropriate bits in the SFRs. Setting the bits CD0(PMR.6), CD1(PMR.7) decides the instruction cycle rate as below:

CD1	CD0	Clocks/Machine Cycle
0	X	4 (default)
1	0	64
1	1	1024

The selection of instruction rate is going to take effect after a delay of one instruction cycle. Switching to divide by 64 or 1024 mode must first go from divide by 4 mode. This means software can not switch directly between clock/64 and clock/1024 mode. The CPU has to return clock/4 mode first, then go to clock/64 or clock/1024 mode.

In Economy mode, the serial port can not receive/transmit data correctly because the baud rate is changed. In some systems, the external interrupts may require the fastest process such that the

reducing of operating speed is restricted. In order to solve these dilemmas, the N79E352(R) offers a switchback feature which allows the CPU back to clock/4 mode immediately when triggered by serial operation (uart and I2C) or external interrupts. The switchback feature is enabled by setting the SWB bit (PMR.5). A serial port/I2C reception/transmission or qualified external interrupt which is enabled and acknowledged without block conditions will cause CPU to return to divide by 4 mode. For the serial port reception, a switchback is generated by a falling edge associated with start bit if the serial port reception is enabled. When a serial port transmission, an instruction which writes a byte of data to serial port buffer will cause a switchback to ensure the correct transmission. The switchback feature is unaffected by serial port interrupt flags. Similarly for I2C reception/transmission, a switchback is generated when a start condition is determined. After a switchback is generated, the software can manually return the CPU to Economy mode. Note that the modification of clock control bits CD0 and CD1 will be ignored during I2C or serial port transmit/receive when switchback is enabled. The Watchdog timer reset, power-on/fail reset, software reset, brownout reset or external reset will force the CPU to return to divide by 4 mode.

10.3 Power Down Mode

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity is completely stopped and the power consumption is reduced to the lowest possible value. In this state the ALE and $\overline{\text{PSEN}}$ pins are pulled low. The port pins output the values held by their respective SFRs.

The N79E352(R) will exit the Power Down mode with a reset or by an external interrupt pin. An external reset can be used to exit the Power down state. The high on RST pin terminates the Power Down mode, and restarts the clock. The program execution will restart from 0000h. In the Power down mode, the clock is stopped, so the Watchdog timer cannot be used to provide the reset to exit Power down mode when its clock source is external OSC or crystal.

The sources that can wake up from the power down mode are external interrupts, keyboard interrupt (KBI), brownout reset (BOR), and watchdog timer interrupt (if WDTCK = 0).

The N79E352(R) can be woken from the Power Down mode by forcing an external interrupt pin activated, provided the corresponding interrupt is enabled, while the global enable(EA) bit is set and the external input has been set to a level detect mode. If these conditions are met, then the low level on the external pin re-starts the oscillator. Then device executes the interrupt service routine for the corresponding external interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after the one which put the device into Power Down mode and continues from there.

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11. RESET CONDITIONS

The user has several hardware related options for placing the N79E352(R) into reset condition. In general, most register bits go to their reset value irrespective of the reset condition, but there are a few flags whose state depends on the source of reset. The user can use these flags to determine the cause of reset using software.

11.1 Sources of reset

11.1.1 External Reset

The device samples the RST pin every machine cycle during state C4. The RST pin must be held high for at least two machine cycles before the reset circuitry applies an internal reset signal. Thus, this reset is a synchronous operation and requires the clock to be running.

The device remains in the reset state as long as RST pin is high and remains high up to two machine cycles after RST is deactivated. Then, the device begins program execution at 0000h. There are no flags associated with the external reset, but, since the other two reset sources do have flags, the external reset is the cause if those flags are clear.

11.1.2 Power-On Reset (POR)

When the power supply rises to the configured level, V_{RST}, the device will perform a power on reset and set the POR flag. The software should clear the POR flag, or it will be difficult to determine the source of future resets.

11.1.3 Brown-Out Reset (BOR)

If the power supply falls below brownout voltage of V_{BOV}, the device goes into the reset state. When the power supply returns to proper levels, the device performs a brownout reset.

11.1.4 Watchdog Timer Reset

The Watchdog Timer is a free-running timer with programmable time-out intervals. The program must clear the Watchdog Timer before the time-out interval is reached to restart the count. If the time-out interval is reached, an interrupt flag is set. 512 clocks later, if the Watchdog Reset is enabled and the Watchdog Timer has not been cleared, the Watchdog Timer generates a reset. The reset condition is maintained by the hardware for two machine cycles, and the WTRF bit in WDCON is set. Afterwards, the device begins program execution at 0000h.

11.1.5 Software Reset

N79E352(R) is enhanced by a software reset. This allows the program code to reset the whole system in software approach. Just writer 1 to SRET bit in AUXR1.3, a software reset will perform. Note that SRST require Timed Access procedure to write. Please refer TA register description

11.2 Reset State

When the device is reset, most registers return to their initial state. The Watchdog Timer is disabled if the reset source was a power-on reset. The Program Counter is set to 0000h, and the stack pointer is reset to 07h. After this, the device remains in the reset state as long as the reset conditions are satisfied.

Reset does not affect the on-chip RAM, however, so RAM is preserved as long as VDD remains above approximately 2V, the minimum operating voltage for the RAM. If VDD falls below 2V, the RAM contents are also lost. In either case, the stack pointer is always reset, so the stack contents are lost.

The WDCON SFR bits are set/cleared in reset condition depending on the source of the reset.

	External reset	Watchdog reset	Power on reset
WDCON	0xxx0x00b	0xxx0100b	01xx0000b

The POR bit WDCON.6 is set only by the power on reset. WTRF bit WDCON.2 is set when the Watchdog timer causes a reset. A power on reset will also clear this bit. The EWRST bit WDCON.1 is cleared by all reset. This disables the Watchdog timer resets.

All the bits in this SFR have unrestricted read access. WDRUN, POR, EWRST, WDIF and WDCLR require Timed Access procedure to write. The remaining bits have unrestricted write accesses.

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12. PROGRAMMABLE TIMERS/COUNTERS

The N79E352(R) has three 16-bit programmable timer/counters and one programmable Watchdog timer. The Watchdog timer is operationally quite different from the other two timers.

12.1 Timer/Counters 0 & 1

Each of these Timer/Counters has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. The two can be configured to operate either as timers, counting machine cycles or as counters counting external inputs.

When configured as a "Timer", the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the system clock or 1/4 of the system clock. In the "Counter" mode, the register is incremented on the falling edge of the external input pin, T0 in case of Timer 0, and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the maximum rate at which counting will take place is 1/24 of the master clock frequency. In either the "Timer" or "Counter" mode, the count register will be updated at C3. Therefore, in the "Timer" mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The "Timer" or "Counter" function is selected by the "C / $\overline{T}$" bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own; bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1. In addition each Timer/Counter can be set to operate in any one of four possible modes. The mode selection is done by bits M0 and M1 in the TMOD SFR.

12.2 Time-base Selection

The N79E352(R) gives the user two modes of operation for the timer. The timers can be programmed to operate like the standard 8051 family, counting at the rate of 1/12 of the clock speed. This will ensure that timing loops on the N79E352(R) and the standard 8051 can be matched. This is the default mode of operation of the N79E352(R) timers. The user also has the option to count in the turbo mode, where the timers will increment at the rate of 1/4 clock speed. This will straight-away increase the counting speed three times. This selection is done by the T0M and T1M bits in CKCON SFR. A reset sets these bits to 0, and the timers then operate in the standard 8051 mode. The user should set these bits to 1 if the timers are to operate in turbo mode.

12.2.1 Mode 0

In Mode 0, the timer/counters act as a 8 bit counter with a 5 bit, divide by 32 pre-scale. In this mode we have a 13 bit timer/counter. The 13 bit counter consists of 8 bits of THx and 5 lower bits of TLx. The upper 3 bits of TLx are ignored.

The negative edge of the clock increments the count in the TLx register. When the fifth bit in TLx moves from 1 to 0, then the count in the THx register is incremented. When the count in THx moves from FFh to 00h, then the overflow flag TFx in TCON SFR is set. The counted input is enabled only if TRx is set and either GATE = 0 or $\overline{INTx}$ = 1. When C / $\overline{T}$ is set to 0, then it will count clock cycles, and if C / $\overline{T}$ is set to 1, then it will count 1 to 0 transitions on T0 (P3.4) for timer 0 and T1 (P3.5) for timer 1. When the 13 bit count reaches 1FFFh the next count will cause it to roll-over to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupts will occur. Note that when used as a timer, the time-base may be either clock cycles/12 or clock cycles/4 as selected by the bits TxM of the CKCON SFR.

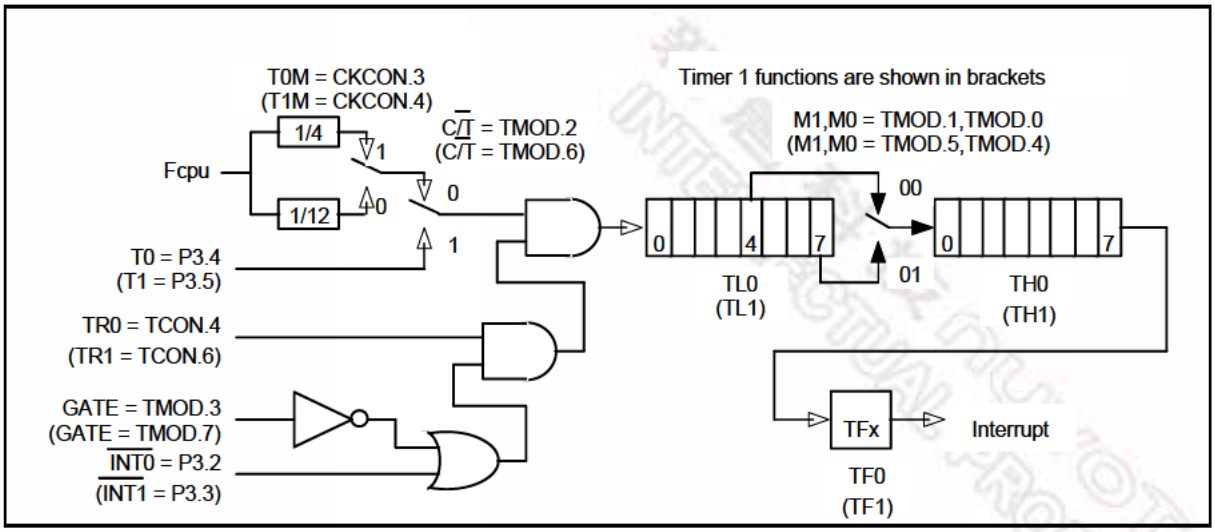


Figure 12-1: Timer/Counter Mode 0 & Mode 1

12.2.2 Mode 1

Mode 1 is similar to Mode 0 except that the counting register forms a 16 bit counter, rather than a 13 bit counter. This means that all the bits of THx and TLx are used. Roll-over occurs when the timer moves from a count of FFFFh to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupt will occur. The selection of the time-base in the timer mode is similar to that in Mode 0. The gate function operates similarly to that in Mode 0.

12.2.3 Mode 2

In Mode 2, the timer/counter is in the Auto Reload Mode. In this mode, TLx acts as a 8 bit count register, while THx holds the reload value. When the TLx register overflows from FFh to 00h, the TFx bit in TCON is set and TLx is reloaded with the contents of THx, and the counting process continues from here. The reload operation leaves the contents of the THx register unchanged. Counting is enabled by the TRx bit and proper setting of GATE and $\overline{INTx}$ pins. As in the other two modes 0 and 1 mode 2 allows counting of either clock cycles (clock/12 or clock/4) or pulses on pin Tn.

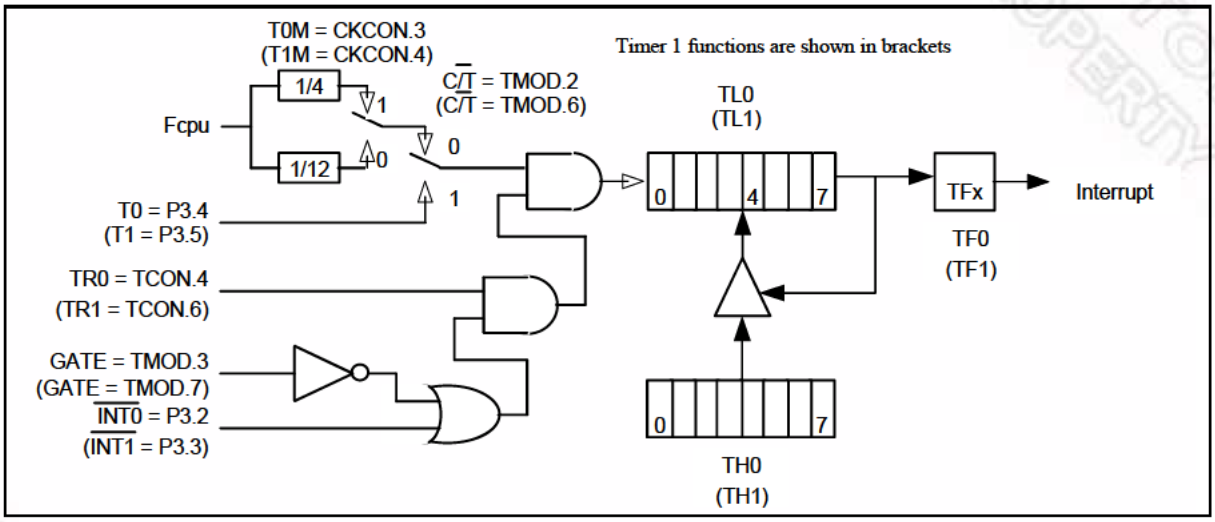


Figure 12-2: Timer/Counter Mode 2

12.2.4 Mode 3

Mode 3 has different operating methods for the two timer/counters. For timer/counter 1, mode 3 simply freezes the counter. Timer/Counter 0, however, configures TL0 and TH0 as two separate 8 bit count registers in this mode. The logic for this mode is shown in the figure. TL0 uses the Timer/Counter 0 control bits C / $\overline{T}$, GATE, TR0, $\overline{INT0}$ and TF0. The TL0 can be used to count clock cycles (clock/12 or clock/4) or 1-to-0 transitions on pin T0 as determined by C/T (TMOD.2). TH0 is forced as a clock cycle counter (clock/12 or clock/4) and takes over the use of TR1 and TF1 from Timer/Counter 1. Mode 3 is used in cases where an extra 8 bit timer is needed. With Timer 0 in Mode 3, Timer 1 can still be used in Modes 0, 1 and 2., but its flexibility is somewhat limited. While its basic functionality is maintained, it no longer has control over its overflow flag TF1 and the enable bit TR1. Timer 1 can still be used as a timer/counter and retains the use of GATE and INT1 pin. In this condition it can be turned on and off by switching it out of and into its own Mode 3. It can also be used as a baud rate generator for the serial port.

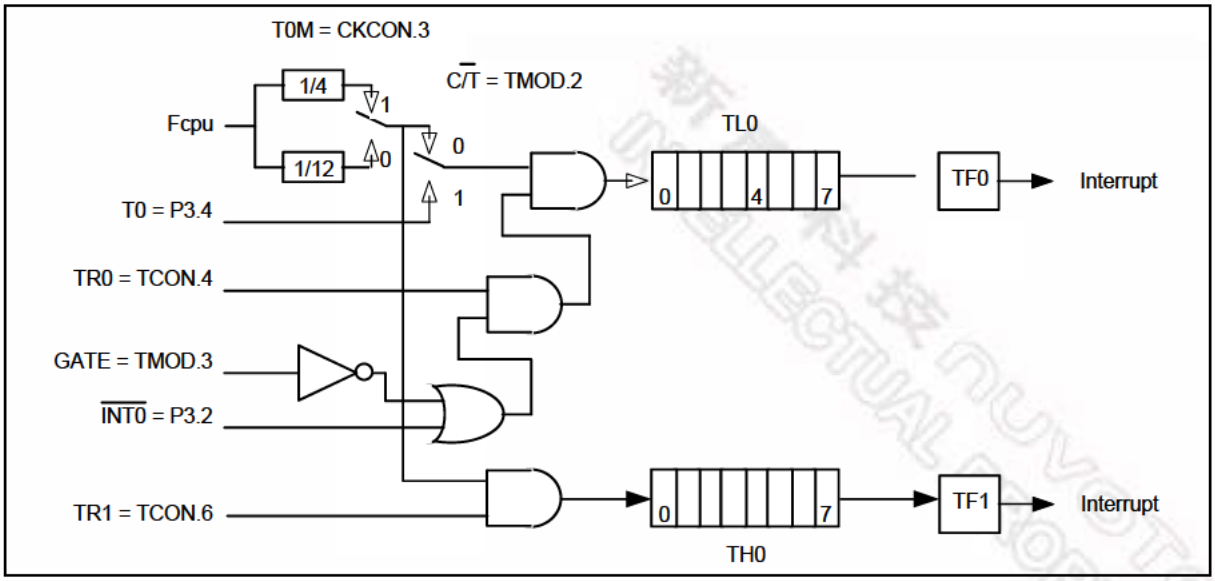


Figure 12-3: Timer/Counter 0 Mode 3

12.3 Timer/Counter 2

Timer/Counter 2 is a 16 bit up/down counter which is configured by the T2MOD register and controlled by the T2CON register. Timer/Counter 2 is equipped with a capture/reload capability. As with the Timer 0 and Timer 1 counters, there exists considerable flexibility in selecting and controlling the clock, and in defining the operating mode. The clock source for Timer/Counter 2 may be selected for either the external T2 pin (C/T2 = 1) or the crystal oscillator, which is divided by 12 or 4 (C/T2 = 0). The clock is then enabled when TR2 is a 1, and disabled when TR2 is a 0.

12.3.1 Capture Mode

The capture mode is enabled by setting the CP / $\overline{RL2}$ bit in the T2CON register to a 1. In the capture mode, Timer/Counter 2 serves as a 16 bit up counter. When the counter rolls over from FFFFh to 0000h, the TF2 bit is set, which will generate an interrupt request. If the EXEN2 bit is set, then a negative transition of T2EX pin will cause the value in the TL2 and TH2 register to be captured by the RCAP2L and RCAP2H registers. This action also causes the EXF2 bit in T2CON to be set, which will also generate an interrupt. Setting the T2CR bit (T2MOD.3), the N79E352(R) allows hardware to reset timer 2 automatically after the value of TL2 and TH2 have been captured.

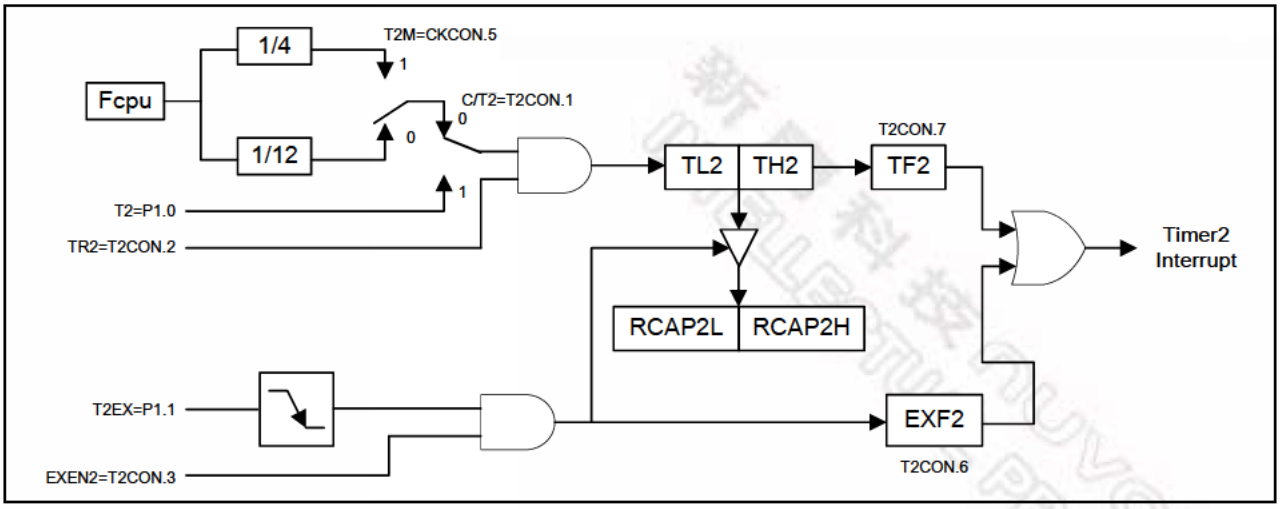


Figure 12-4: Timer 2 16-Bit Capture Mode

12.3.2 Auto-Reload Mode, Counting up

The auto-reload mode as an up counter is enabled by clearing the CP / $\overline{RL2}$ bit in the T2CON register and clearing the DCEN bit in T2MOD register. In this mode, Timer/Counter 2 is a 16 bit up counter. When the counter rolls over from FFFFh, a reload is generated that causes the contents of the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers. The reload action also sets the TF2 bit. If the EXEN2 bit is set, then a negative transition of T2EX pin will also cause a reload. This action also sets the EXF2 bit in T2CON.

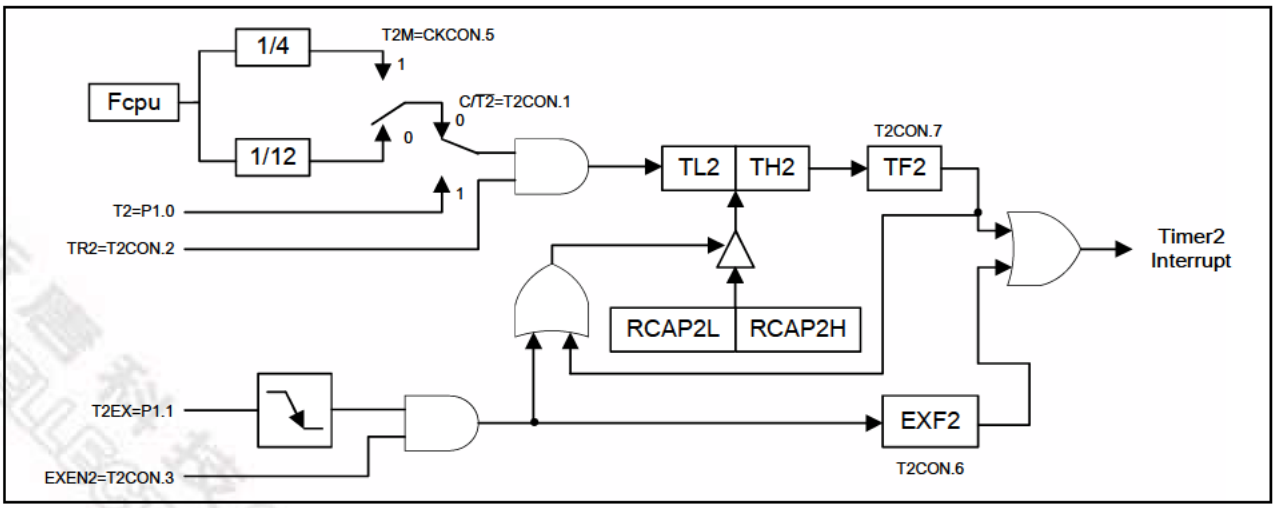


Figure 12-5: Timer 2 16-Bit Auto-reload Mode, Counting Up

12.3.3 Auto-Reload Mode, Counting Up/Down

Timer/Counter 2 will be in auto-reload mode as an up/down counter if CP / $\overline{RL2}$ bit in T2CON is cleared and the DCEN bit in T2MOD is set. In this mode, Timer/Counter 2 is an up/down counter whose direction is controlled by the T2EX pin. A 1 on this pin cause the counter to count up. An overflow while counting up will cause the counter to be reloaded with the contents of the capture

registers. The next down count following the case where the contents of Timer/Counter equal the capture registers will load an FFFFh into Timer/Counter 2. In either event a reload will set the TF2 bit. A reload will also toggle the EXF2 bit. However, the EXF2 bit can not generate an interrupt while in this mode.

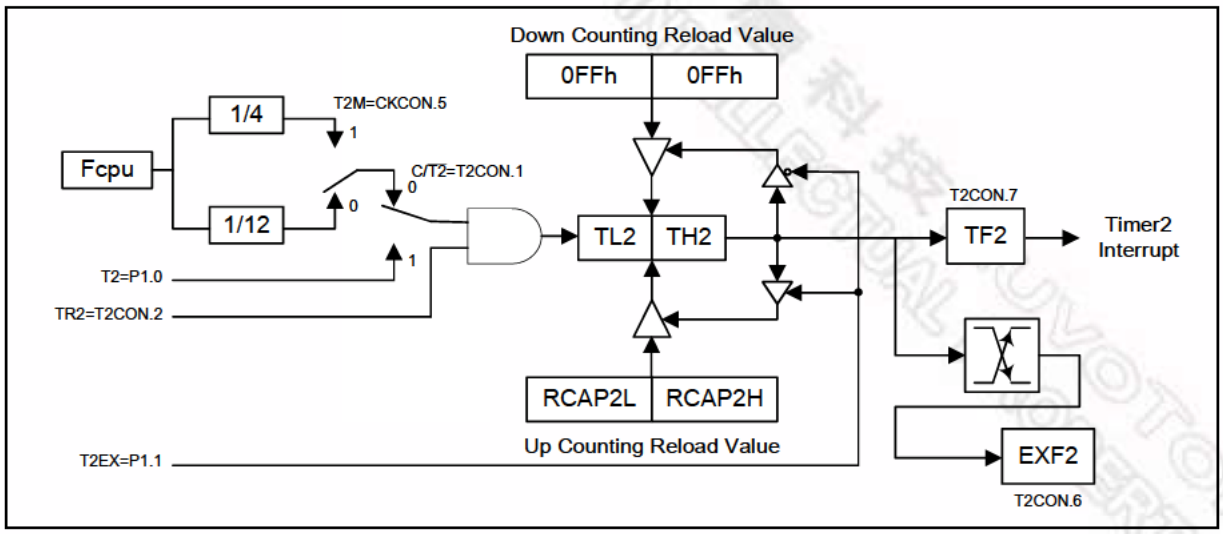


Figure 12-6: Timer 2 16-Bit Auto-reload Up/Down Counter

12.3.4 Baud Rate0 Generator Mode

The baud rate generator mode is enabled by setting either the RCLK or TCLK bits in T2CON register. While in the baud rate generator mode, Timer/Counter 2 is a 16 bit counter with auto reload when the count rolls over from FFFFh. However, rolling over does not set the TF2 bit. If EXEN2 bit is set, then a negative transition of the T2EX pin will set EXF2 bit in the T2CON register and cause an interrupt request.

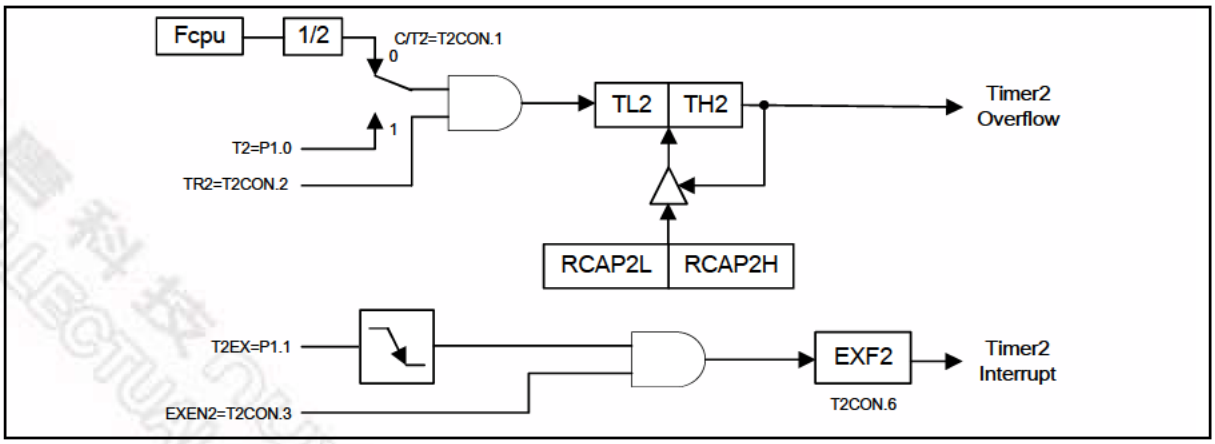


Figure 12-7: Baud Rate Generator Mode

12.3.5 Programmable Clock-out

Timer 2 is equipped with a new clock-out feature which outputs a 50% duty cycle clock on P1.0. It can be invoked as a programmable clock generator. To configure Timer 2 with clock-out mode, software must initiate it by setting bit T2OE = 1, C/T2 = 0 and CP/RL = 0. Setting bit TR2 will start the timer. This mode is similar to the baud rate generator mode, it will not generate an interrupt while Timer 2 overflow. So it is possible to use Timer 2 as a baud rate generator and a clock generator at the same time. The clock-out frequency is determined by the following equation:

The Clock-Out Frequency = Oscillator Frequency / [4 X 65536-(RCAP2H, RCAP2L)]

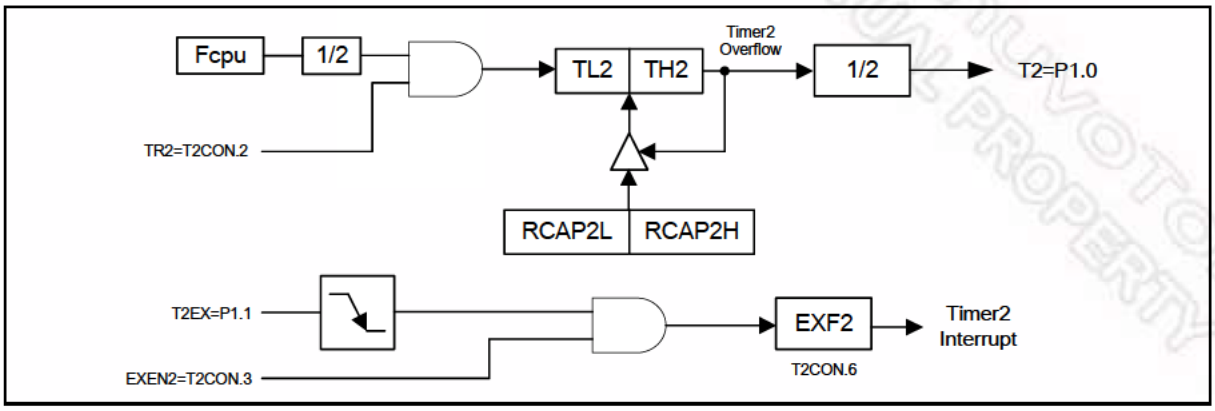


Figure 12-8: Programmable Clock-Out Mode

13. NVM MEMORY

The N79E352(R) has NVM data memory of 128 bytes for customer's data store used. The NVM data memory has 8 pages area and each page has 16 bytes.

13.1 Operation

User is required to enable EnNVM (NVMCON.5) bit for NVM read. This is due to overlapping of NVM data memory and external data memory physical address, the following table is defined. EnNVM bit (NVMCON.5) will enable read access to NVM data memory area.

EnNVM	Data Memory Area
0	Enable External RAM read/write access by MOVX
1	Enable NVM data Memory read access by MOVX only. If EER or EWR is set and NVM flash erase or write control is busy, to set this bit read NVM data is invalid.

Table 13-1: MOVX instruction to Enable Read Data Memory Area Definition Table

The NVM memory can be read/write by customer program to access. Read NVM data is by MOVX A,@DPTR/R0/R1 instructions, and write data is by SFR of NVMADDR, NVMDAT and NVMCON. Before write data to NVM memory, the page must be erased by providing page address on NVMADDR, which address of On-Chip Code Memory space will decode, then set EER of NVMCON.7. This will automatically hold fetch program code and PC Counter, and execute page erase. After finished, this bit will be cleared by hardware. The erase time is ~ 5ms.

For writing data to NVM memory, user must set address and data to NVMADDR and NVMDAT, then set EWR of NVMCON.6 to initiate nvm data write. The uC will hold program code and PC Counter, and then write data to mapping address. Upon write completion, the EWR bit will be cleared by hardware, the uC will continue execute next instruction. The program time is ~50us.

NVM data Flash Memory is permanently operating from 11.0592MHz internal clock source. In order to reduce power consumption, the on chip oscillator will only be enabled when during program or erase, through EWR or EER in NVMCON SFR. EWR or EER bits are cleared by hardware after program or erase completed. The program/erase time is automatically controlled by hardware.

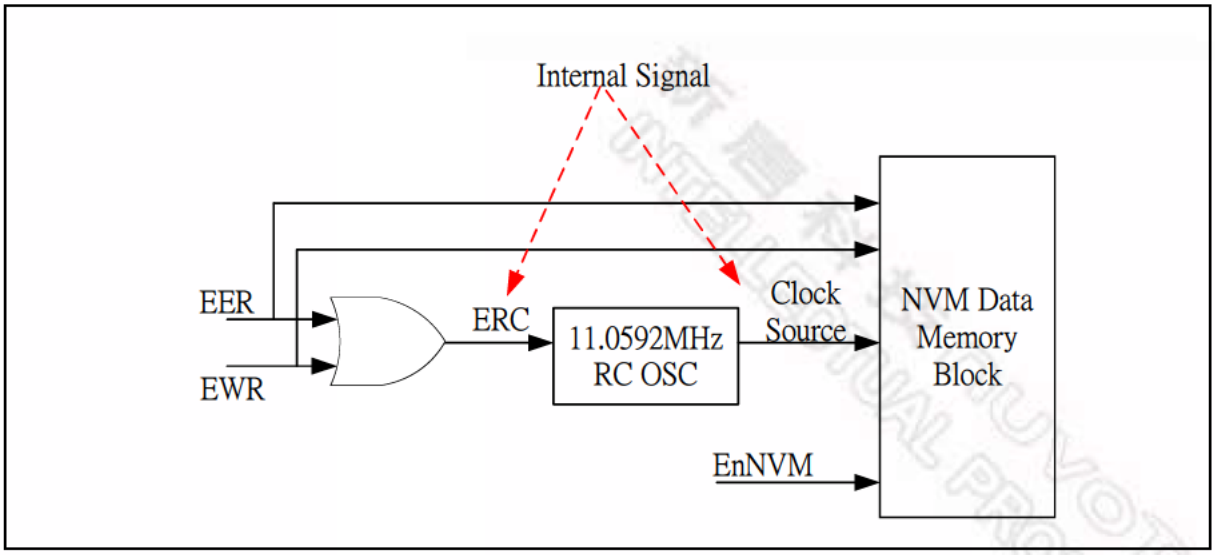


Figure 13-1: NVM control

Instructions	EnNVM = 0	EnNVM = 1	
		Addr within NVM address range	Addr out of NVM address range
MOVX A, @DPTR (Read)	Ext memory	NVM	Ext memory
MOVX A, @R0 (Read)	Ext memory	NVM	Ext memory[1]
MOVX A, @R1 (Read)	Ext memory	NVM	Ext memory[1]
MOVX @DPTR, A (Write)	Ext memory	Ext memory	Ext memory
MOVX @R0, A (Write)	Ext memory	Ext memory[1]	Ext memory[1]
MOVX @R1, A (Write)	Ext memory	Ext memory[1]	Ext memory[1]

Table 13-2: MOVX read/write access destination

Note: 1. Higher address bytes will come from SFR port 2 values.

For security purposes this NVM data flash provide an independent “Lock bit” located in Security bits, it is used to protect the customer’s data code in NVM. It may be enabled in CONFIG1.6 after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, NVM Flash EPROM data can not be accessed again by hardware writer mode.

14. WATCHDOG TIMER

The Watchdog Timer is a free-running Timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs a flag is set, which can cause an interrupt if enabled, and a system reset can also be caused if it is enabled. The interrupt will occur if the individual interrupt enable and the global enable are set. The interrupt and reset functions are independent of each other and may be used separately or together depending on the user's software.

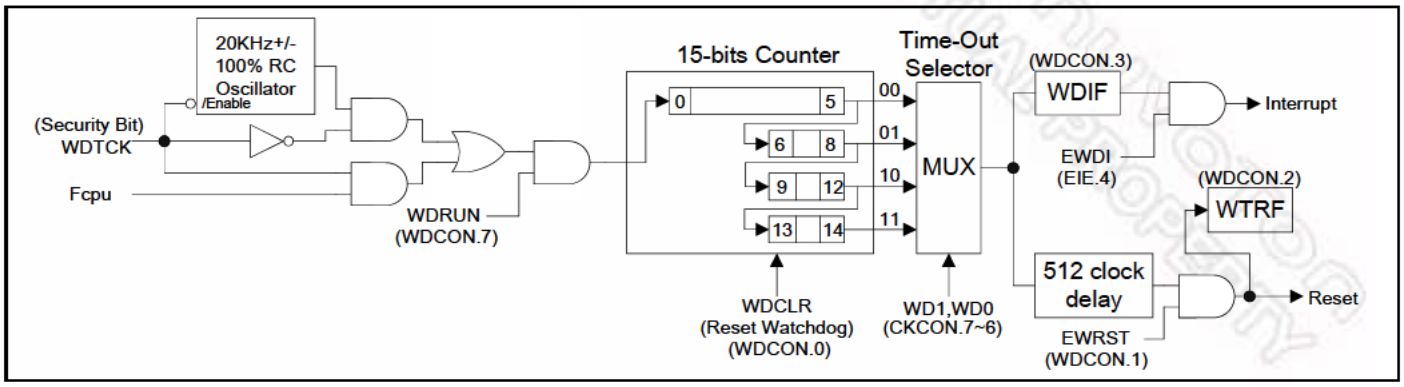


Figure 14-1: Watchdog Timer

The Watchdog Timer should first be restarted by using WDCLR. This ensures that the timer starts from a known state. The WDCLR bit is used to restart the Watchdog Timer. This bit is self clearing, i.e. after writing a 1 to this bit the software will automatically clear it. The Watchdog Timer will now count clock cycles. The time-out interval is selected by the two bits WD1 and WD0 (CKCON.7 and CKCON.6). When the selected time-out occurs, the Watchdog interrupt flag WDIF (WDCON.3) is set. After the time-out has occurred, the Watchdog Timer waits for an additional 512 clock cycles. If the Watchdog Reset EWRST (WDCON.1) is enabled, then 512 clocks after the time-out, if there is no WDCLR, a system reset due to Watchdog Timer will occur. This will last for two machine cycles, and the Watchdog Timer reset flag WTRF (WDCON.2) will be set. This indicates to the software that the Watchdog was the cause of the reset.

When used as a simple timer, the reset and interrupt functions are disabled. The timer will set the WDIF flag each time the timer completes the selected time interval. The WDIF flag is polled to detect a time-out and the WDCLR allows software to restart the timer. The Watchdog Timer can also be used as a very long timer. The interrupt feature is enabled in this case. Every time the time-out occurs an interrupt will occur if the global interrupt enable EA is set.

The main use of the Watchdog Timer is as a system monitor. This is important in real-time control applications. In case of some power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. Using the watchdog timer interrupt during software development will allow the user to select ideal watchdog reset locations. The code is first written without the watchdog interrupt or reset. Then the Watchdog interrupt is enabled to identify code locations where interrupt occurs. The user can now insert instructions to reset the Watchdog Timer, which will allow the code to run without any Watchdog Timer interrupts. Now the Watchdog Timer reset is enabled and the Watchdog interrupt may be disabled. If any errant code is

executed now, then the reset Watchdog Timer instructions will not be executed at the required instants and Watchdog reset will occur.

The Watchdog Timer time-out selection will result in different time-out values depending on the clock speed. The reset will occur, when enabled, 512 clocks after the time-out has occurred.

WD1	WD0	WATCHDOG INTERVAL	NUMBER OF CLOCKS	TIME @ 20 KHZ
0	0	2^6	64	3.2 mS
0	1	2^9	512	25.6 mS
1	0	2^{13}	8192	409.6 mS
1	1	2^{15}	32768	1638.4 mS

Table 14-1: Time-out values for the Watchdog timer.

The default Watchdog time-out is 2^6 clocks, which is the shortest time-out period. The EWRST, WDIF and WDCLR bits are protected by the Timed Access procedure. This prevents software from accidentally enabling or disabling the watchdog timer. More importantly, it makes it highly improbable that errant code can enable or disable the Watchdog Timer.

The security bit WDTCK is located at bit 7 of CONFIG0 register. This bit is for user to configure the clock source of watchdog timer either from the internal RC or from the uC clock.

15. UART SERIAL PORT

Serial port in the N79E352(R) is a full duplex port. The N79E352(R) provides the user with additional features such as the Frame Error Detection and the Automatic Address Recognition. The serial ports are capable of synchronous as well as asynchronous communication. In Synchronous mode the N79E352(R) generates the clock and operates in a half duplex mode. In the asynchronous mode, full duplex operation is available. This means that it can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF Special Function Register. However any write to SBUF will be to the transmit register, while a read from SBUF will be from the receive buffer register. The serial port can operate in four different modes as described below.

15.1 Mode 0

This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RXD line. TXD is used to transmit the shift clock. The TxD clock is provided by the N79E352(R) whether the device is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is transmitted/received first. The baud rate is fixed at 1/12 or 1/4 of the oscillator frequency. This baud rate is determined by the SM2 bit (SCON.5). When this bit is set to 0, then the serial port runs at 1/12 of the clock. When set to 1, the serial port runs at 1/4 of the clock. This additional facility of programmable baud rate in mode 0 is the only difference between the standard 8051 and the N79E352(R).

The functional block diagram is shown below. Data enters and leaves the Serial port on the RxD line. The TxD line is used to output the shift clock. The shift clock is used to shift data into and out of the N79E352(R) and the device at the other end of the line. Any instruction that causes a write to SBUF will start the transmission. The shift clock will be activated and data will be shifted out on the RxD pin till all 8 bits are transmitted. If SM2 = 1, then the data on RxD will appear 1 clock period before the falling edge of shift clock on TxD. The clock on TxD then remains low for 2 clock periods, and then goes high again. If SM2 = 0, the data on RxD will appear 3 clock periods before the falling edge of shift clock on TxD. The clock on TxD then remains low for 6 clock periods, and then goes high again. This ensures that at the receiving end the data on RxD line can either be clocked on the rising edge of the shift clock on TxD or latched when the TxD clock is low.

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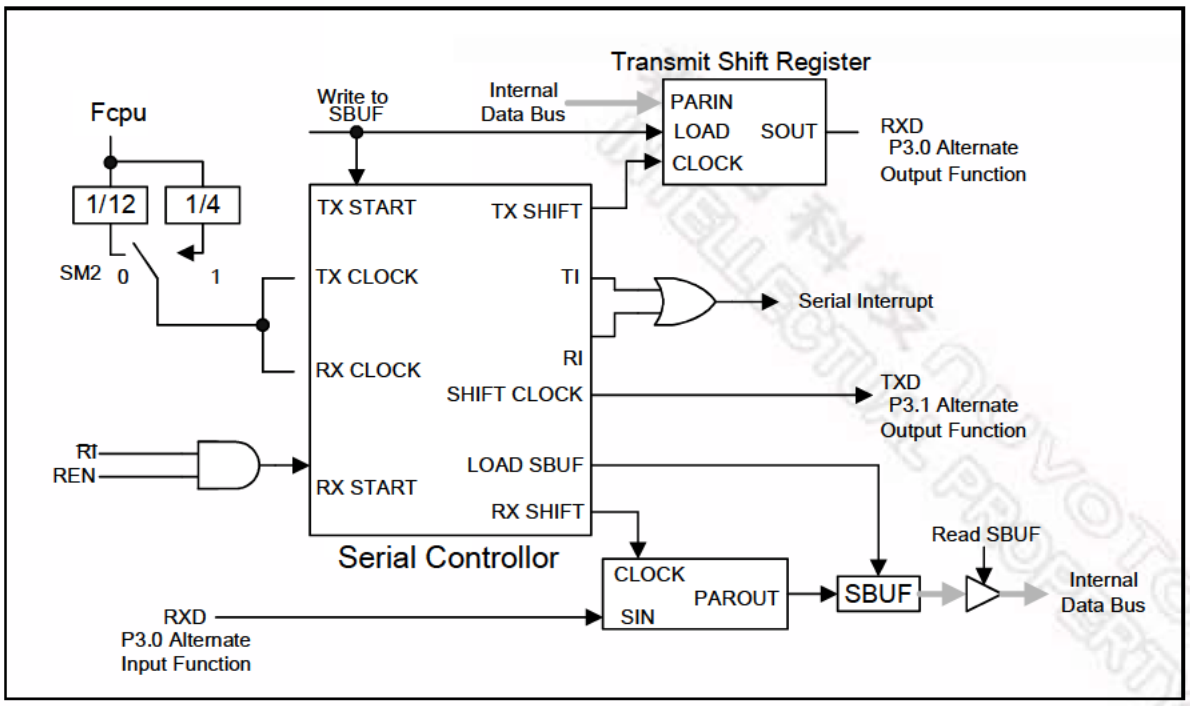


Figure 15-1: Uart Serial Port Mode 0

The TI flag is set high in C1 following the end of transmission of the last bit. The serial port will receive data when REN is 1 and RI is zero. The shift clock (TxD) will be activated and the serial port will latch data on the rising edge of shift clock. The external device should therefore present data on the falling edge on the shift clock. This process continues till all the 8 bits have been received. The RI flag is set in C1 following the last rising edge of the shift clock on TxD. This will stop reception, till the RI is cleared by software.

15.2 Mode 1

In Mode 1, the full duplex asynchronous mode is used. Serial communication frames are made up of 10 bits transmitted on TXD and received on RXD. The 10 bits consist of a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in the SFR SCON. The baud rate in this mode is variable. The serial baud can be programmed to be 1/16 or 1/32 of the Timer 1 overflow or 1/16 of Timer 2 overflow. Since the Timer 1 and 2 can be set to different reload values, a wide variation in baud rates is possible.

Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at C1 following the first roll-over of divide by 16 counter. The next bit is placed on TxD pin at C1 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counter and not directly to the write to SBUF signal. After all 8 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the C1 state after the stop bit has been put out on TxD pin. This will be at the 10th rollover of the divide by 16 counter after a write to SBUF.

Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counter.

The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three basis. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port. If the first bit detected after the falling edge of RxD pin is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF.

After shifting in 8 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and
2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

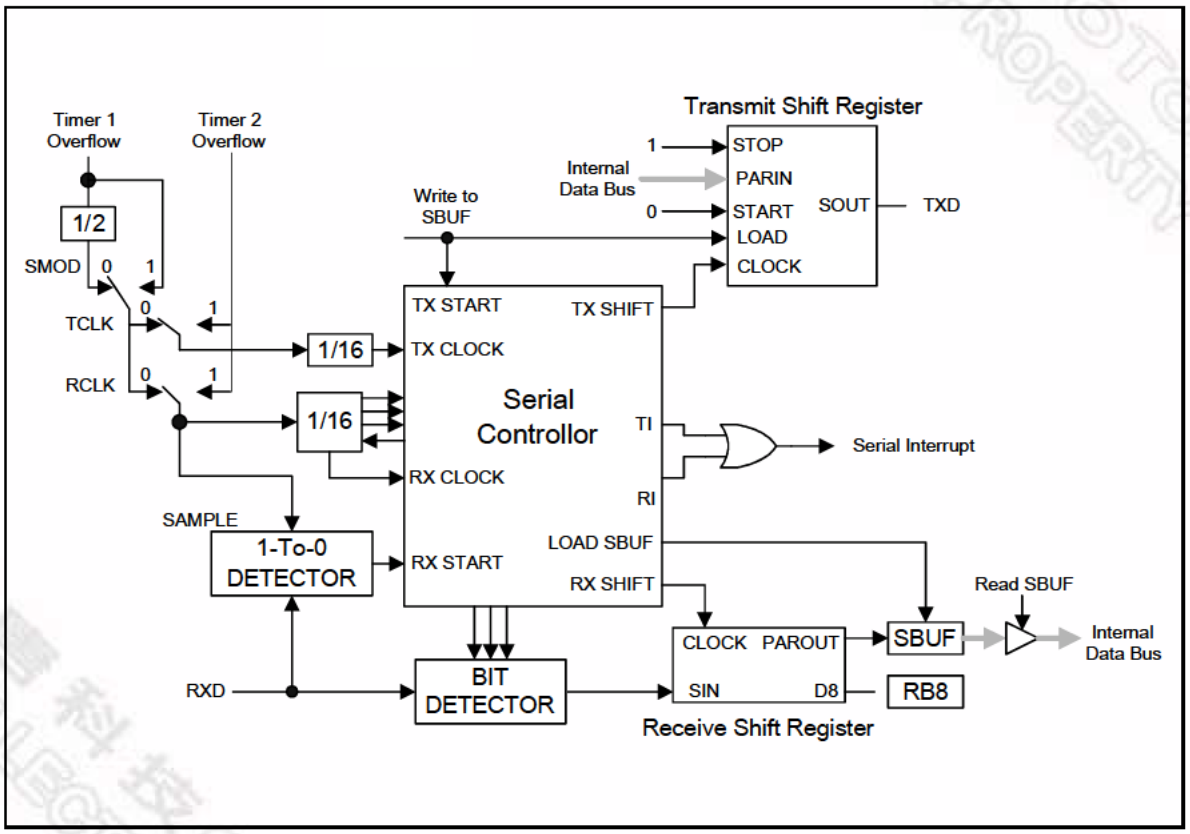


Figure 15-2: Uart Serial Port Mode 1

15.3 Mode 2

This mode uses a total of 11 bits in asynchronous full-duplex communication. The functional description is shown in the figure below. The frame consists of one start bit (0), 8 data bits (LSB first), a programmable 9th bit (TB8) and a stop bit (0). The 9th bit received is put into RB8. The baud rate is programmable to 1/32 or 1/64 of the oscillator frequency, which is determined by the SMOD bit in

PCON SFR. Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at C1 following the first roll-over of the divide by 16 counter. The next bit is placed on TxD pin at C1 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counter, and not directly to the write to SBUF signal. After all 9 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the C1 state after the stop bit has been put out on TxD pin. This will be at the 11th rollover of the divide by 16 counter after a write to SBUF. Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counter. The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three basis. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port.

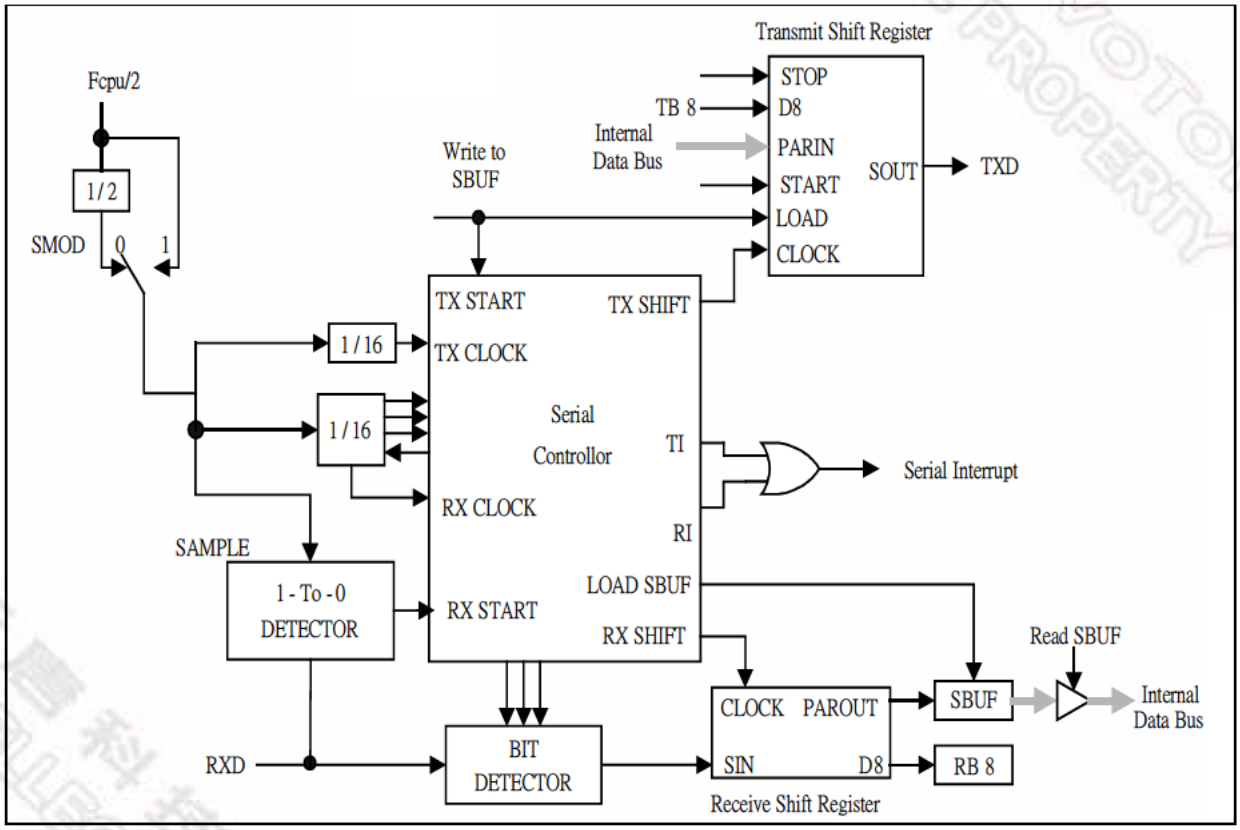


Figure 15-3: Uart Serial Port Mode 2

If the first bit detected after the falling edge of RxD pin, is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF. After shifting in 9 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and
2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

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15.4 Mode 3

This mode is similar to Mode 2 in all respects, except that the baud rate is programmable. The user must first initialize the Serial related SFR SCON before any communication can take place. This involves selection of the Mode and baud rate. The Timer 1 should also be initialized if modes 1 and 3 are used. In all four modes, transmission is started by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if REN = 1. The external device will start the communication by transmitting the start bit.

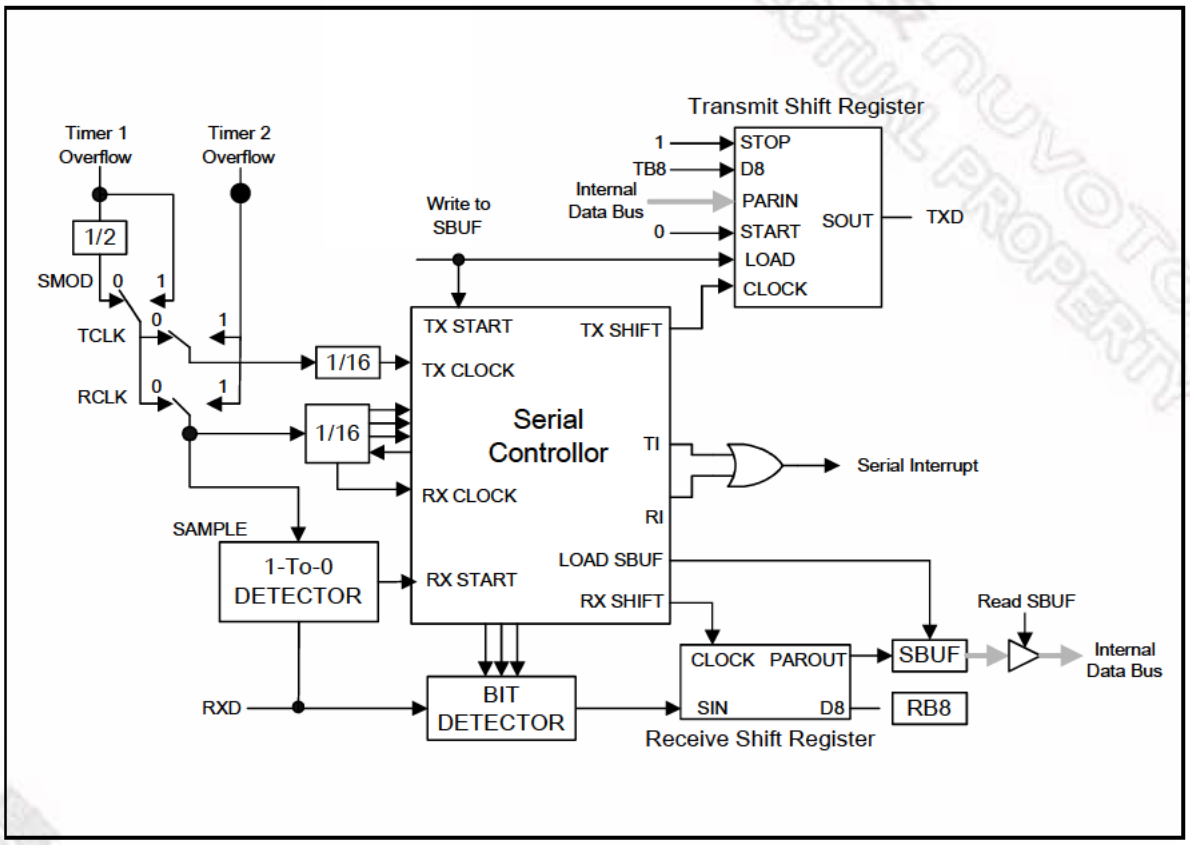


Figure 15-4: Uart Serial Port Mode 3

SM1	SM0	Mode	Type	Baud Clock	Frame Size	Start Bit	Stop Bit	9th bit Function
0	0	0	Synch.	4 or 12 TCLKS	8 bits	No	No	None
0	1	1	Asynch.	Timer 1 or 2	10 bits	1	1	None
1	0	2	Asynch.	32 or 64 TCLKS	11 bits	1	1	0, 1
1	1	3	Asynch.	Timer 1 or 2	11 bits	1	1	0, 1

Table 15-1: Uart Serial Port Modes

15.5 Framing Error Detection

A Frame Error occurs when a valid stop bit is not detected. This could indicate incorrect serial data communication. Typically the frame error is due to noise and contention on the serial communication line. The N79E352(R) has the facility to detect such framing errors and set a flag which can be checked by software.

The Frame Error FE bit is located in SCON.7. This bit is normally used as SM0 in the standard 8051 family. However, in the N79E352(R) it serves a dual function and is called SM0/FE. There are actually two separate flags, one for SM0 and the other for FE. The flag that is actually accessed as SCON.7 is determined by SMOD0 (PCON.6) bit. When SMOD0 is set to 1, then the FE flag is indicated in SM0/FE. When SMOD0 is set to 0, then the SM0 flag is indicated in SM0/FE.

The FE bit is set to 1 by hardware but must be cleared by software. Note that SMOD0 must be 1 while reading or writing to FE. If FE is set, then any following frames received without any error will not clear the FE flag. The clearing has to be done by software.

15.6 Multiprocessor Communications

Multiprocessor communications makes use of the 9th data bit in modes 2 and 3. In the N79E352(R), the RI flag is set only if the received byte corresponds to the Given or Broadcast address. This hardware feature eliminates the software overhead required in checking every received address, and greatly simplifies the software programmer task.

In the multiprocessor communication mode, the address bytes are distinguished from the data bytes by transmitting the address with the 9th bit set high. When the master processor wants to transmit a block of data to one of the slaves, it first sends out the address of the targeted slave (or slaves). All the slave processors should have their SM2 bit set high when waiting for an address byte. This ensures that they will be interrupted only by the reception of a address byte. The Automatic address recognition feature ensures that only the addressed slave will be interrupted. The address comparison is done in hardware not software.

The addressed slave clears the SM2 bit, thereby clearing the way to receive data bytes. With SM2 = 0, the slave will be interrupted on the reception of every single complete frame of data. The unaddressed slaves will be unaffected, as they will be still waiting for their address. In Mode 1, the 9th bit is the stop bit, which is 1 in case of a valid frame. If SM2 is 1, then RI is set only if a valid frame is received and the received byte matches the Given or Broadcast address.

The Master processor can selectively communicate with groups of slaves by using the Given Address. All the slaves can be addressed together using the Broadcast Address. The addresses for each slave are defined by the SADDR and SADEN SFRs. The slave address is an 8-bit value specified in the SADDR SFR. The SADEN SFR is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR.

The following example shows how the user can define the Given Address to address different slaves.

Slave 1:

SADDR 1010 0100
SADEN 1111 1010
Given 1010 0x0x

Slave 2:

SADDR 1010 0111
SADEN 1111 1001
Given 1010 0xx1

The Given address for slave 1 and 2 differ in the LSB. For slave 1, it is a don't care, while for slave 2 it is 1. Thus to communicate only with slave 1, the master must send an address with LSB = 0 (1010 0000). Similarly the bit 1 position is 0 for slave 1 and don't care for slave 2. Hence to communicate only with slave 2 the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. The bit 3 position is don't care for both the slaves. This allows two different addresses to select both slaves (1010 0001 and 1010 0101).

The master can communicate with all the slaves simultaneously with the Broadcast Address. This address is formed from the logical ORing of the SADDR and SADEN SFRs. The zeros in the result are defined as don't cares In most cases the Broadcast Address is FFh. In the previous case, the Broadcast Address is (1111111X) for slave 1 and (11111111) for slave 2.

The SADDR and SADEN SFRs are located at address A9h and B9h respectively. On reset, these two SFRs are initialized to 00h. This results in Given Address and Broadcast Address being set as XXXX XXXX(i.e. all bits don't care). This effectively removes the multiprocessor communications feature, since any selectivity is disabled.

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16. I2C SERIAL PORT

The I2C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus are:

– Bidirectional data transfer between masters and slaves

– Multimaster bus (no central master)

– Arbitration between simultaneously transmitting masters without corruption of serial data on the bus

– Serial clock synchronization allows devices with different bit rates to communicate via one serial bus

– Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer

– The I2C bus may be used for test and diagnostic purposes

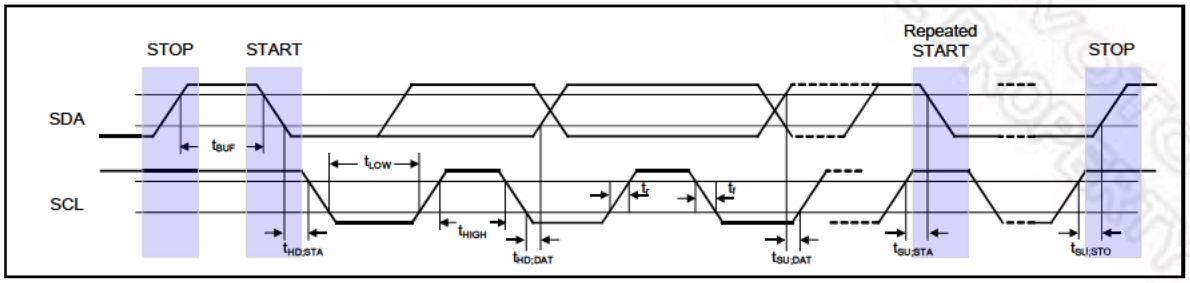


Figure 16-1: I2C Bus Timing

The device's on-chip I2C logic provides the serial interface that meets the I2C bus standard mode specification. The I2C logic handles bytes transfer autonomously. It also keeps track of serial transfers, and a status register (I2STATUS) reflects the status of the I2C bus.

The I2C port, SCL and SDA are at P1.2 and P1.3. When the I/O pins are used as I2C port, user must set the pins to logic high in advance. When I2C port is enabled by setting ENS to high, the internal states will be controlled by I2CON and I2C logic hardware. Once a new status code is generated and stored in I2STATUS, the I2C interrupt flag (SI) will be set automatically. If both EA and EI2C are also in logic high, the I2C interrupt is requested. The 5 most significant bits of I2STATUS stores the internal state code, the lowest 3 bits are always zero and the content keeps stable until SI is cleared by software.

16.1 I2C Bus

The I2C bus is a serial I/O port, which supports all transfer modes from and to the I2C bus. The I2C port handles byte transfers autonomously. To enable this port, the bit ENSI in I2CON should be set to '1'. The CPU interfaces to the I2C port through the following six special function registers: I2CON (control register, C0H), I2STATUS (status register, BDH), I2DAT (data register, BCH), I2ADDR (address registers, C1H), I2CLK (clock rate register BEH) and I2TIMER (Timer counter register, BFH). The H/W interfaces to the I2C bus via two pins: SDA (P1.2, serial data line) and SCL (P1.3, serial clock line). Pull up resistor is needed for Pin P1.2 and P1.3 for I2C operation as these are 2 open drain pins (on I2C mode).

16.2 The I2C Control Registers:

The I2C has 1 control register (I2CON) to control the transmit/receive flow, 1 data register (I2DAT) to buffer the Tx/Rx data, 1 status register (I2STATUS) to catch the state of Tx/Rx, recognizable slave address register for slave mode use and 1 clock rate control block for master mode to generate the variable baud rate.

16.2.1 The Address Registers, I2ADDR

I2C port is equipped with one slave address register. The contents of the register are irrelevant when I2C is in master mode. In the slave mode, the seven most significant bits must be loaded with the MCU's own slave address. The I2C hardware will react if the contents of I2ADDR are matched with the received slave address.

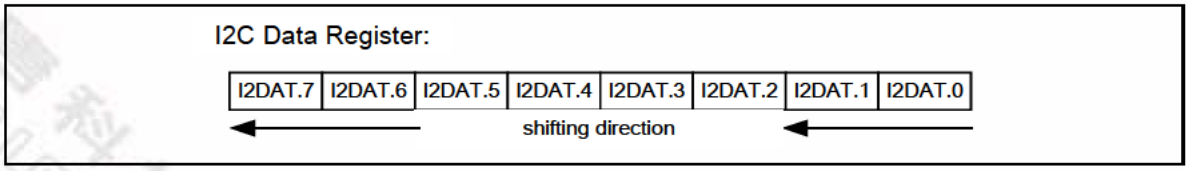
The I2C ports support the "General Call" function. If the GC bit is set the I2C port1 hardware will respond to General Call address (00H). Clear GC bit to disable general call function.

When GC bit is set, the I2C is in Slave mode, it can be received the general call address by 00H after Master send general call address to I2C bus, then it will follow status of GC mode. If it is in Master mode, the AA bit must be cleared when it will send general call address of 00H to I2C bus.

16.2.2 The Data Register, I2DAT

This register contains a byte of serial data to be transmitted or a byte which has just been received. The CPU can read from or write to this 8-bit directly addressable SFR while it is not in the process of shifting a byte. This occurs when the bus is in a defined state and the serial interrupt flag (SI) is set. Data in I2DAT remains stable as long as SI bit is set. While data is being shifted out, data on the bus is simultaneously being shifted in; I2DAT always contains the last data byte present on the bus. Thus, in the event of arbitration lost, the transition from master transmitter to slave receiver is made with the correct data in I2DAT.

I2DAT and the acknowledge bit form a 9-bit shift register, the acknowledge bit is controlled by the hardware and cannot be accessed by the CPU. Serial data is shifted through the acknowledge bit into I2DAT on the rising edges of serial clock pulses on the SCL line. When a byte has been shifted into I2DAT, the serial data is available in I2DAT, and the acknowledge bit (ACK or NACK) is returned by the control logic during the ninth clock pulse. Serial data is shifted out from I2DAT on the falling edges of SCL clock pulses, and is shifted into I2DAT on the rising edges of SCL clock pulses.



16.2.3 The Control Register, I2CON

The CPU can read from and write to this 8-bit, directly addressable SFR. Two bits are affected by hardware: the SI bit is set when the I2C hardware requests a serial interrupt, and the STO bit is cleared when a STOP condition is present on the bus. The STO bit is also cleared when ENS = "0".

ENSI — Set to enable I2C serial function block. When ENS=1 the I2C serial function enables. The port latches of SDA1 and SCL1 must be set to logic high.

STA — I2C START Flag. Setting STA to logic 1 to enter master mode, the I2C hardware sends a START or repeat START condition to bus when the bus is free.

STO — I2C STOP Flag. In master mode, setting STO to transmit a STOP condition to bus then I2C hardware will check the bus condition if a STOP condition is detected this flag will be cleared by hardware automatically. In a slave mode, setting STO resets I2C hardware to the defined "not addressed" slave mode. This means it is NO LONGER in the slave receiver mode to receive data from the master transmit device.

SI — I2C Port 1 Interrupt Flag. When a new I2C bus state is present in the S1STA register, the SI flag is set by hardware, and if the EA and EI2C1 bits are both set, the I2C1 interrupt is requested. SI must be cleared by software.

AA — Assert Acknowledge control bit. When AA=1 prior to address or data received, an acknowledged (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line when 1.) A slave is acknowledging the address sent from master, 2.) The receiver devices are acknowledging the data sent by transmitter. When AA=0 prior to address or data received, a Not acknowledged (high level to SDA) will be returned during the acknowledge clock pulse on the SCL line.

16.2.4 The Status Register, I2STATUS

I2STATUS is an 8-bit read-only register. The three least significant bits are always 0. The five most significant bits contain the status code. There are 26 possible status codes. When I2STATUS contains F8H, no serial interrupt is requested. All other I2STATUS values correspond to defined I2C bus states. When each of these states is entered, a status interrupt is requested (SI = 1). A valid status code is present in I2STATUS one machine cycle after SI is set by hardware and is still present one machine cycle after SI has been reset by software.

16.2.5 The I2C Clock Baud Rate Bits, I2CLK

The data baud rate of I2C is determines by I2CLK register when I2C is in a master mode. It is not important when I2C is in a slave mode. In the slave modes, I2C will automatically synchronize with any clock frequency up to 400 KHz from master I2C device.

The data baud rate of I2C setting is Data Baud Rate of I2C = Fcpu / (I2CLK+1). The Fcpu=Fosc/4. If Fosc = 16MHz, the I2CLK = 40(28H), so data baud rate of I2C = 16MHz/(4X (40 +1)) = 97.56Kbits/sec. The block diagram is as below figure.

16.2.6 I2C Time-out Counter, I2Timerx

The I2C logic block provides a 14-bit timer-out counter that helps user to deal with bus pending problem. When SI is cleared user can set ENTI=1 to start the time-out counter. If I2C bus is pended too long to get any valid signal from devices on bus, the time-out counter overflows cause TIF=1 to request an I2C interrupt. The I2C interrupt is requested in the condition of either SI=1 or TIF=1. Flags SI and TIF must be cleared by software.

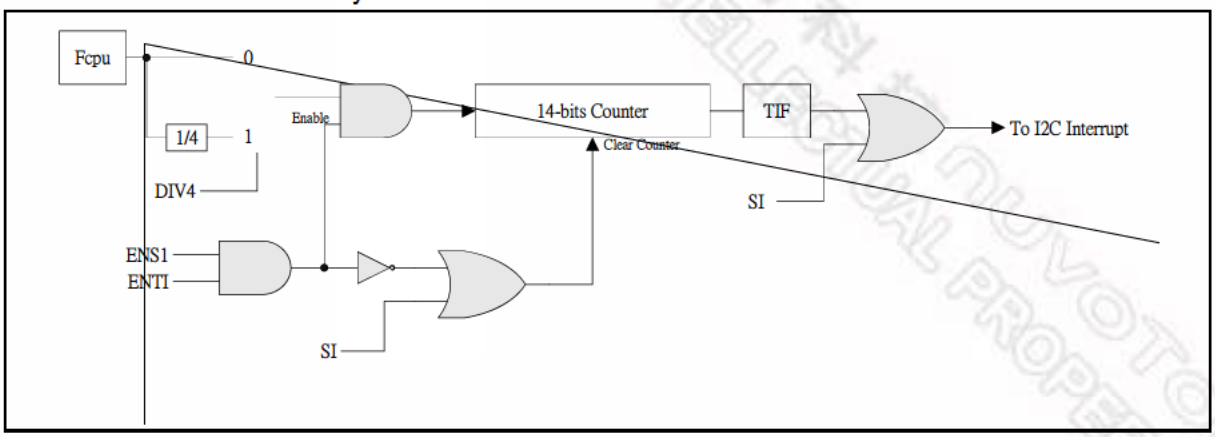


Figure 16-2: I2C Timer Count Block Diagram

16.3 Modes of Operation

The on-chip I2C ports support five operation modes, Master transmitter, Master receiver, Slave transmitter, Slave receiver, and GC call.

In a given application, I2C port may operate as a master or as a slave. In the slave mode, the I2C port hardware looks for its own slave address and the general call address. If one of these addresses is detected, and if the slave is willing to receive or transmit data from/to master(by setting the AA bit), acknowledge pulse will be transmitted out on the 9th clock, hence an interrupt is requested on both master and slave devices if interrupt is enabled. When the microcontroller wishes to become the bus master, the hardware waits until the bus is free before the master mode is entered so that a possible slave action is not interrupted. If bus arbitration is lost in the master mode, I2C port switches to the slave mode immediately and can detect its own slave address in the same serial transfer.

16.3.1 Master Transmitter Mode

Serial data output through SDA while SCL outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the data direction bit. In this case the data direction bit (R/W) will be logic 0, and it is represented by “W” in the flow diagrams. Thus the first byte transmitted is SLA+W. Serial data is transmitted 8 bits at a time. After each byte is transmitted, an acknowledge bit is received. START and STOP conditions are output to indicate the beginning and the end of a serial transfer.

16.3.2 Master Receiver Mode

In this case the data direction bit (R/W) will be logic 1, and it is represented by “R” in the flow diagrams. Thus the first byte transmitted is SLA+R. Serial data is received via SDA while SCL outputs the serial clock. Serial data is received 8 bits at a time. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are output to indicate the beginning and end of a serial transfer.

16.3.3 Slave Receiver Mode

Serial data and the serial clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.

16.3.4 Slave Transmitter Mode

The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted via SDA while the serial clock is input through SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

16.4 Data Transfer Flow in Five Operating Modes

The five operating modes are: Master/Transmitter, Master/Receiver, Slave/Transmitter, Slave/Receiver and GC Call. Bits STA, STO and AA in I2CON register will determine the next state of the I2C hardware after SI flag is cleared. Upon complexion of the new action, a new status code will be updated and the SI flag will be set. If the I2C interrupt control bits (EA and EI2) are enable, appropriate action or software branch of the new status code can be performed in the Interrupt service routine.

Data transfers in each mode are shown in the following figures.

*** Legend for the following five figures:

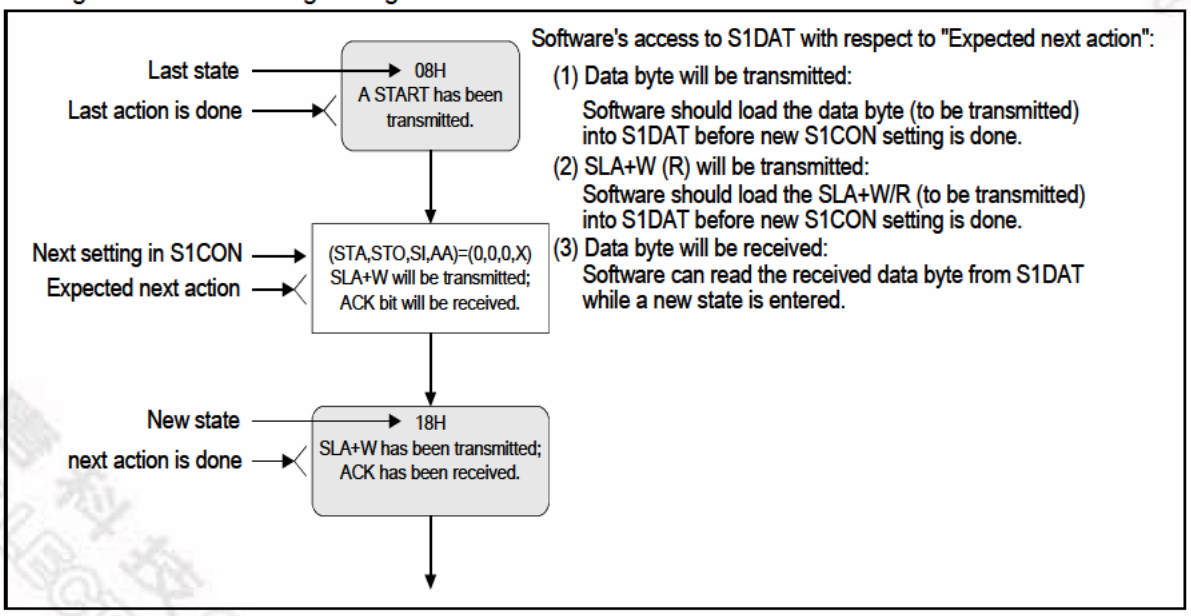


Figure 16-3: Legen for the following four figures

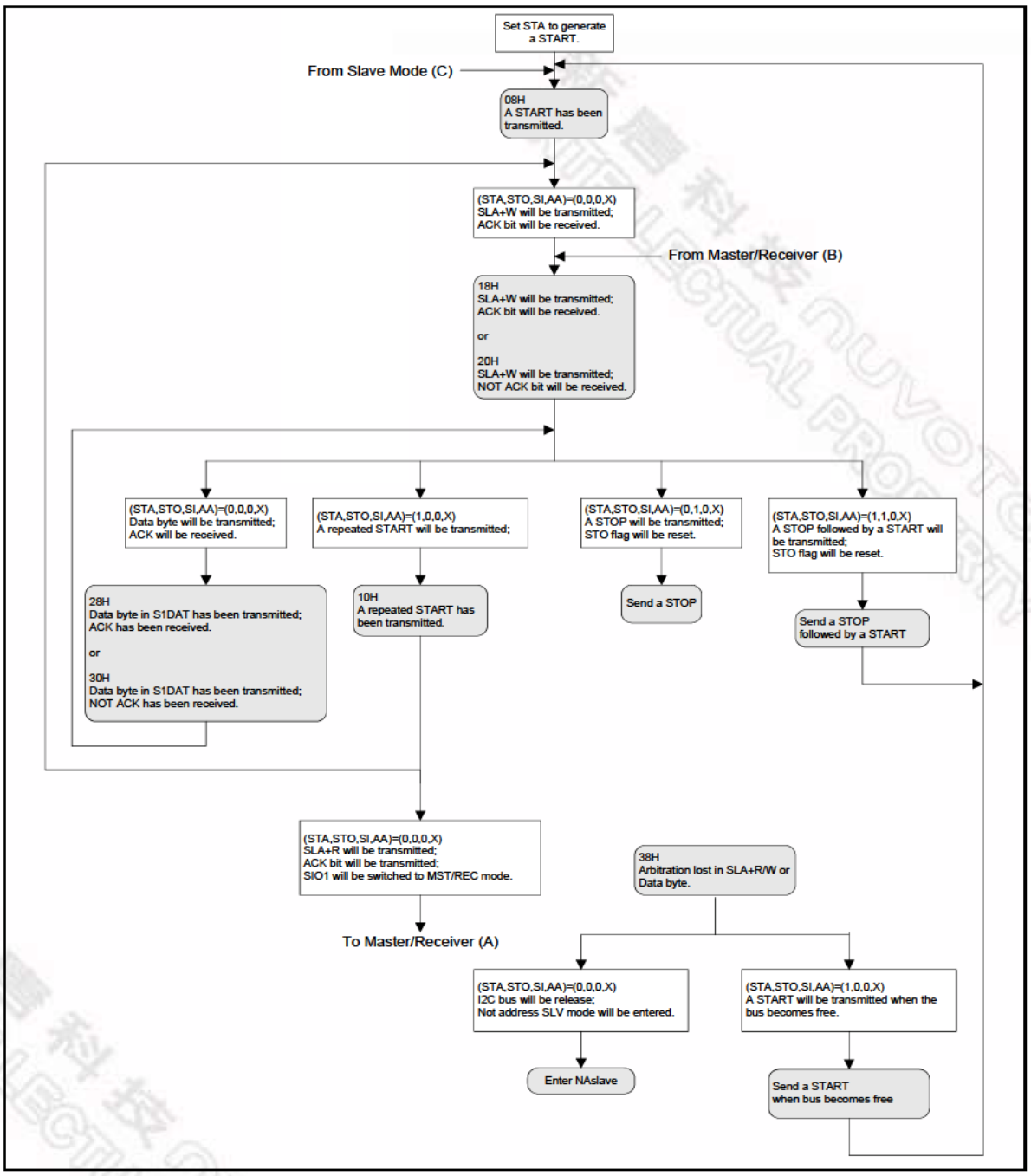


Figure 16-4: Master Transmitter Mode

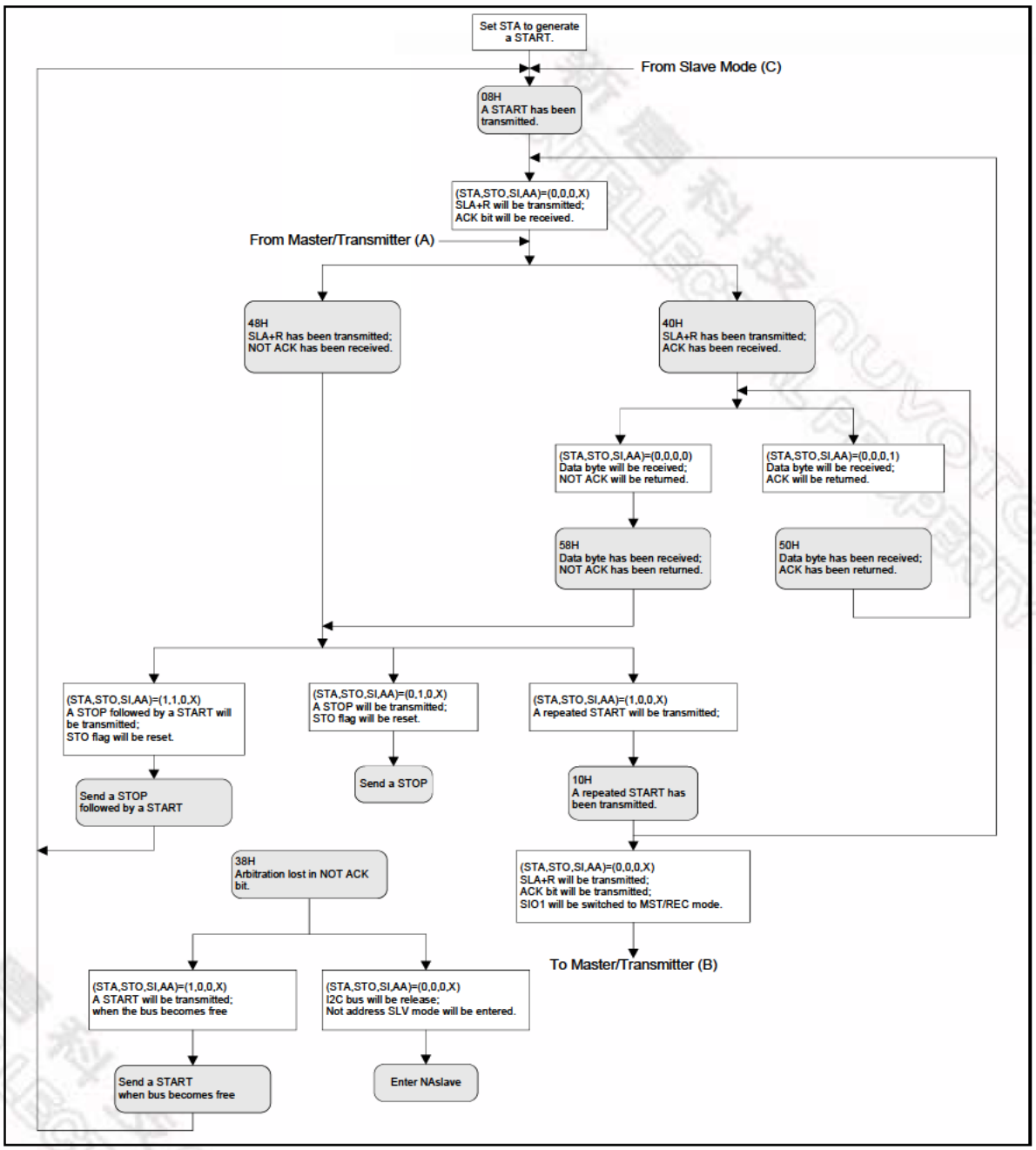


Figure 16-5: Master Receiver Mode

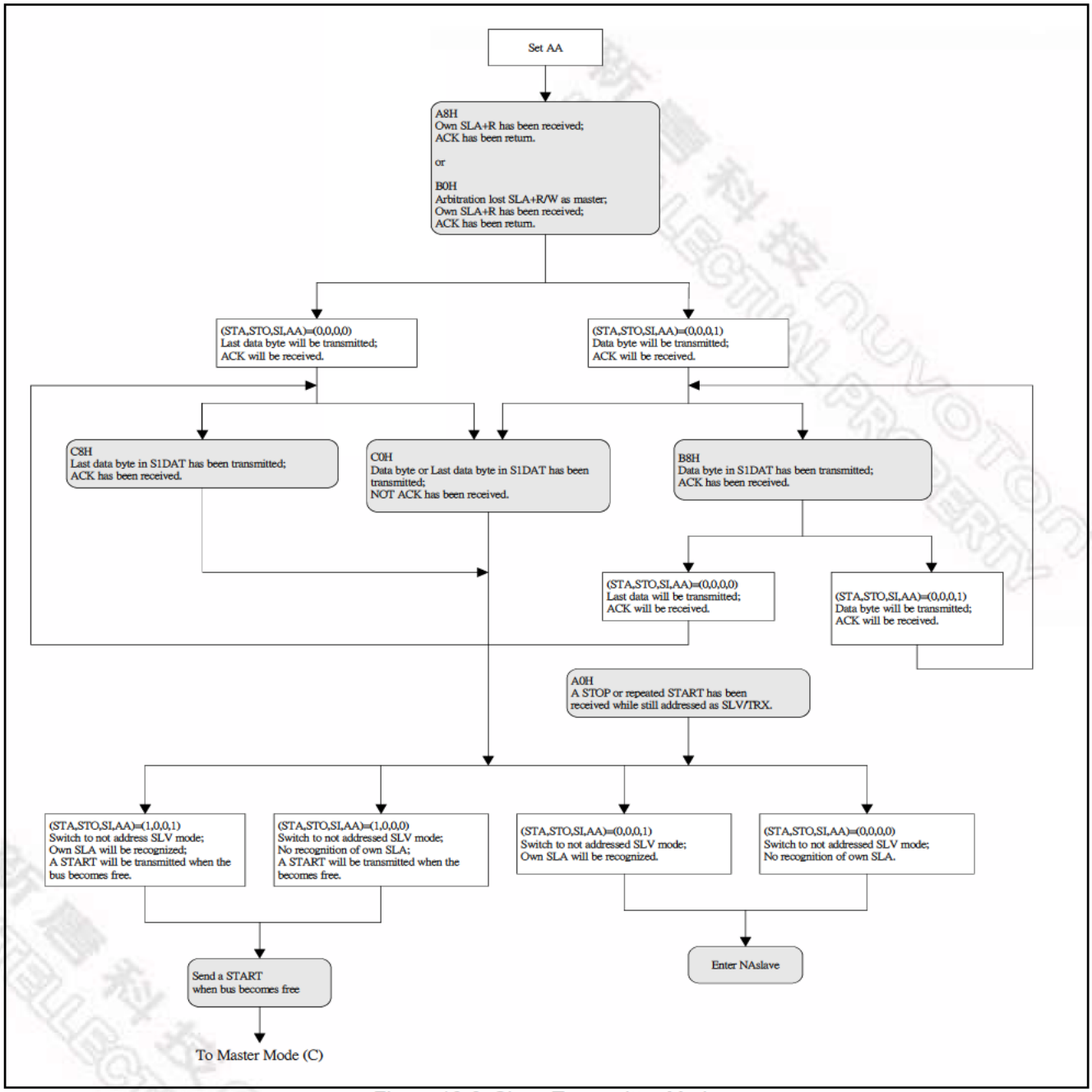


Figure 16-6: Slave Transmitter Mode

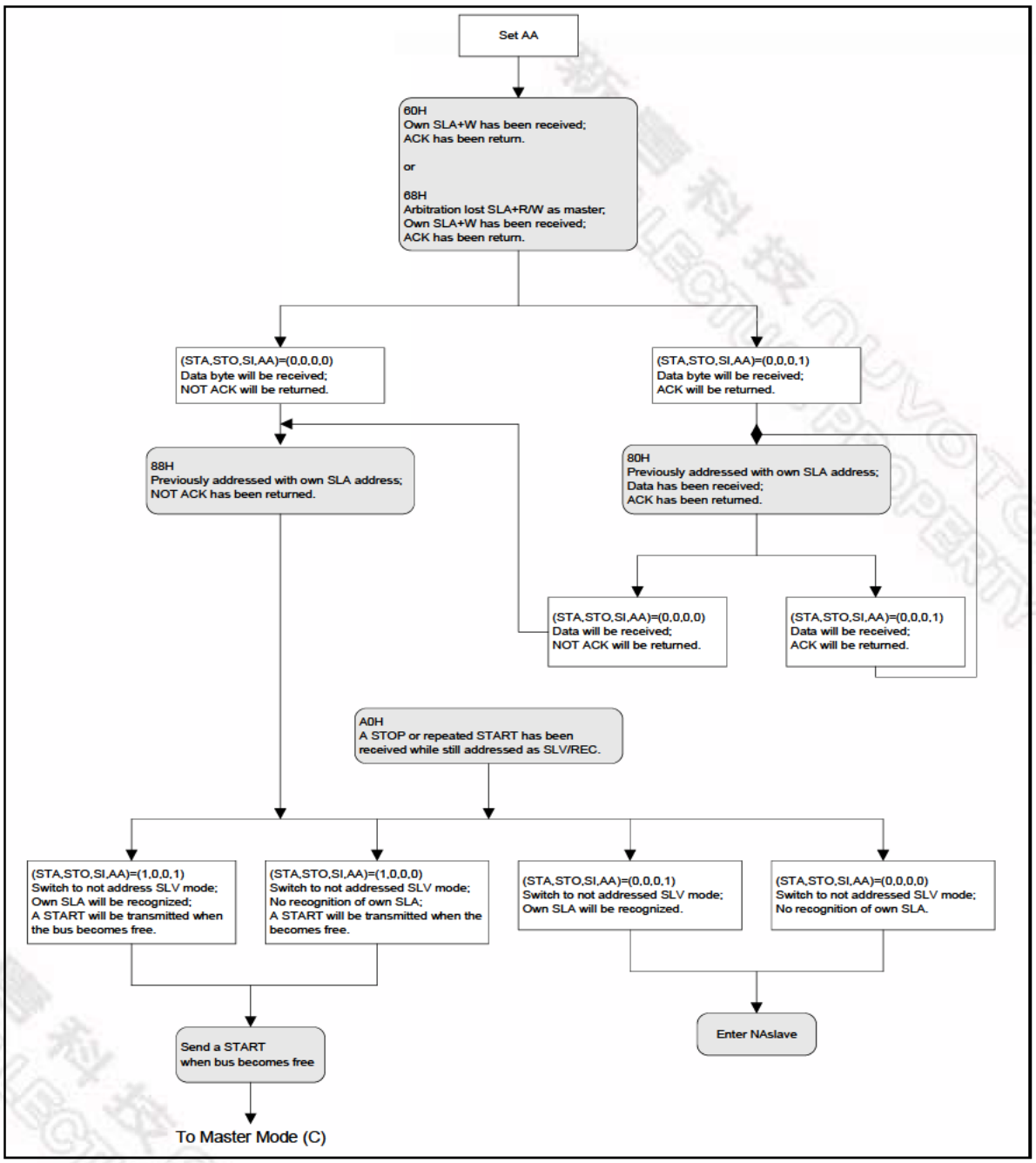


Figure 16-7: Slave Receiver Mode

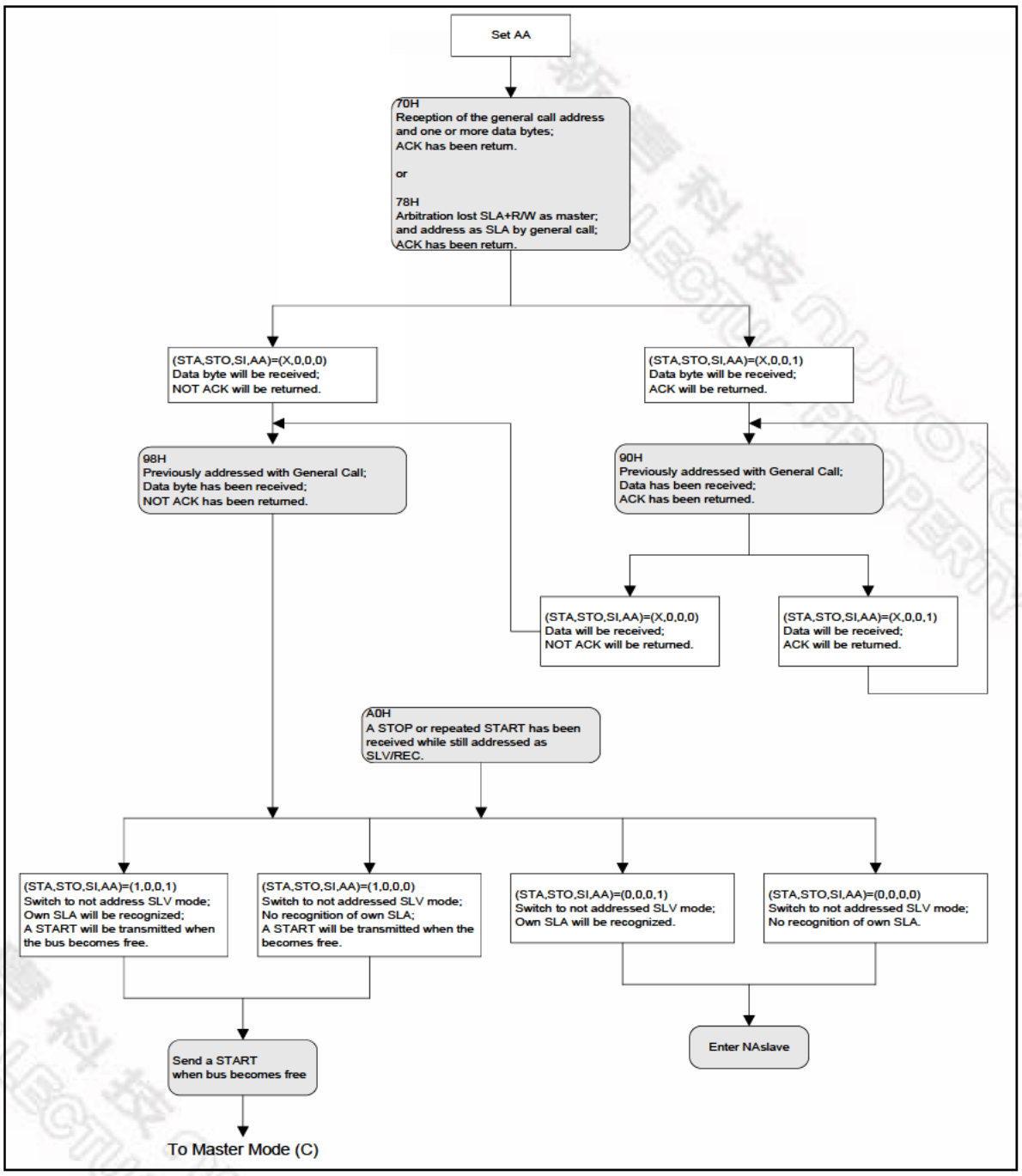


Figure 16-8: GC Mode

17. TIMED ACCESS PROTECTION

The N79E352(R) has several new features, like the Watchdog timer, on-chip ROM size adjustment, wait state control signal and Power on/fail reset flag, which are crucial to proper operation of the system. If left unprotected, errant code may write to the Watchdog control bits resulting in incorrect operation and loss of control. In order to prevent this, the N79E352(R) has a protection scheme which controls the write access to critical bits. This protection scheme is done using a timed access.

In this method, the bits which are to be protected have a timed write enable window. A write is successful only if this window is active, otherwise the write will be discarded. This write enable window is open for 3 machine cycles if certain conditions are met. After 3 machine cycles, this window automatically closes. The window is opened by writing AAh and immediately 55h to the Timed Access(TA) SFR. This SFR is located at address C7h. The suggested code for opening the timed access window is

```
TA      REG    0C7h          ; define new register TA, located at 0C7h
MOV     TA, #0AAh
MOV     TA, #055h
```

When the software writes AAh to the TA SFR, a counter is started. This counter waits for 3 machine cycles looking for a write of 55h to TA. If the second write (55h) occurs within 3 machine cycles of the first write (AAh), then the timed access window is opened. It remains open for 3 machine cycles, during which the user may write to the protected bits. Once the window closes the procedure must be repeated to access the other protected bits.

Examples of Timed Assessing are shown below

Example 1: Valid access

```
MOV     TA, #0AAh          3 M/C
MOV     TA, #055h          3 M/C
MOV     WDCON, #00h        3 M/C
```

Note: M/C = Machine Cycles

Example 2: Valid access

```
MOV     TA, #0AAh          3 M/C
MOV     TA, #055h          3 M/C
NOP                        1 M/C
SETB    EWRST              2 M/C
```

Example 3: Valid access

```
MOV     TA, #0Aah          3 M/C
MOV     TA, #055h          3 M/C
ORL     WDCON, #00000010B  3M/C
```

Example 4: Invalid access

```
MOV     TA, #0AAh          3 M/C
MOV     TA, #055h          3 M/C
NOP                        1 M/C
NOP                        1 M/C
CLR     POR                2 M/C
```

Example 5: Invalid Access

```
MOV     TA, #0AAh          3 M/C
NOP                        1 M/C
```

```
MOV   TA, #055h          3 M/C
SETB  EWRST              2 M/C
```

In the first two examples, the writing to the protected bits is done before the 3 machine cycle window closes. In Example 3, however, the writing to the protected bit occurs after the window has closed, and so there is effectively no change in the status of the protected bit. In Example 4, the second write to TA occurs 4 machine cycles after the first write, therefore the timed access window in not opened at all, and the write to the protected bit fails.

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18. INTERRUPTS

N79E352(R) has four priority level interrupts structure with 11 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled.

18.1 Interrupt Sources

The External Interrupts $\overline{INT0}$ and $\overline{INT1}$ can be either edge triggered or level triggered, programmable through bits IT0 and IT1 (SFR TCON). The bits IE0 and IE1 in TCON register are the flags which are checked to generate the interrupt. In the edge triggered mode, the INTx inputs are sampled in every machine cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IEx in TCON is set. The flag bit requests the interrupt. Since the external interrupts are sampled every machine cycle, they have to be held high or low for at least one complete machine cycle. The IEx flag is automatically cleared when the service routine is called. If the level triggered mode is selected, then the requesting source has to hold the pin low till the interrupt is serviced. The IEx flag will not be cleared by the hardware on entering the service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source.

The Timer 0 and 1 Interrupts are generated by the TF0 and TF1 flags. These flags are set by the overflow in the Timer 0 and Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced. The Watchdog timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog Timer interrupt flag WDIF (WDCON.3) is set. If the interrupt is enabled by the enable bit EIE.4, then an interrupt will occur.

The timer 2 interrupt is generated through TF2 (timer 2 overflow/compare match). The hardware does not clear these flags when a timer 2 interrupt is executed.

The uart serial block can generate interrupt on reception or transmission. There are two interrupt sources from the uart block, which are obtained by the RI and TI bits in the SCON SFR. These bits are not automatically cleared by the hardware, and the user will have to clear these bits using software.

This device also provide an independent I2C serial port. When new I2C state is present in I2STATUS, the SI flag is set by hardware, and if EA and EI2 bits are both set, the I2C interrupt is requested. SI must be cleared by software.

Keyboard interrupt is generated when any of the keypad connected to P0 pins is pressed. Each keypad interrupt can be individually enabled or disabled. User will have to software clear the flag bit.

The input capture 0 interrupt is generated through CPTF0 flag. CPTF0 flag is set by input capture events. The hardware does not clear this flag when the capture interrupt is executed. Software has to clear the flag.

Brownout detect can cause brownout flag, BOF, to be asserted if power voltage drop below brownout voltage level. Interrupt will occur if BOI (AUXR1.5), EBO (EIE.6) and global interrupt enable are set.

Source	Vector Address	Source	Vector Address
External Interrupt 0	0003H	Timer 0 Overflow	000BH
External Interrupt 1	0013H	Timer 1 Overflow	001BH
Serial Port	0023H	Brownout Interrupt	002BH
I2C Interrupt	0033H	KBI Interrupt	003BH
Timer 2 Overflow	0043H	-	004BH
Watchdog Timer	0053H	-	005BH

	0063H	Input Capture 0 Interrupt	006BH

Table 18- 1: N79E352(R) interrupt vector table

18.2 Priority Level Structure

There are four priority levels for the interrupts, highest, high, low and lowest. The interrupt sources can be individually set to either high or low levels. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as shown on Table 18- 2: Four-level interrupts priority.

The interrupt flags are sampled every machine cycle. In the same machine cycle, the sampled interrupts are polled and their priority is resolved. If certain conditions are met then the hardware will execute an internally generated LCALL instruction which will vector the process to the appropriate interrupt vector address. The conditions for generating the LCALL are;

1. An interrupt of equal or higher priority is not currently being serviced.

2. The current polling cycle is the last machine cycle of the instruction currently being execute.

3. The current instruction does not involve a write to IE, EIE, IP0, IP0H, IP1 or IPH1 registers and is not a RETI.

If any of these conditions are not met, then the LCALL will not be generated. The polling cycle is repeated every machine cycle, with the interrupts sampled in the same machine cycle. If an interrupt flag is active in one cycle but not responded to, and is not active when the above conditions are met, the denied interrupt will not be serviced. This means that active interrupts are not remembered; every polling cycle is new.

The processor responds to a valid interrupt by executing an LCALL instruction to the appropriate service routine. This may or may not clear the flag which caused the interrupt. In case of Timer interrupts, the TF0 or TF1 flags are cleared by hardware whenever the processor vectors to the appropriate timer service routine. In case of external interrupt, /INT0 and /INT1, the flags are cleared only if they are edge triggered. In case of Serial interrupts, the flags are not cleared by hardware. In the case of Timer 2 interrupt, the flags are not cleared by hardware. The Watchdog timer interrupt flag WDIF has to be cleared by software. The hardware LCALL behaves exactly like the software LCALL instruction. This instruction saves the Program Counter contents onto the Stack, but does not save the Program Status Word PSW. The PC is reloaded with the vector address of that interrupt which caused the LCALL. These address of vector for the different sources are as shown on Table 18- 3: Summary of interrupt sources. The vector table is not evenly spaced; this is to accommodate future expansions to the device family.

Execution continues from the vectored address till an RETI instruction is executed. On execution of the RETI instruction the processor pops the Stack and loads the PC with the contents at the top of the stack. The user must take care that the status of the stack is restored to what it was after the hardware LCALL, if the execution is to return to the interrupted program. The processor does not notice anything if the stack contents are modified and will proceed with execution from the address put back into PC. Note that a RET instruction would perform exactly the same process as a RETI instruction, but it would not inform the Interrupt Controller that the interrupt service routine is completed, and would leave the controller still thinking that the service routine is underway.

N79E352(R) uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the interrupt sources.

PRIORITY BITS		INTERRUPT PRIORITY LEVEL
IPXH	IPX	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

Table 18- 2: Four-level interrupts priority

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in registers IE or EIE. The IE register also contains a global disable bit, EA, which disables all interrupts at once.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the IP0, IP0H, IP1, and IP1H registers. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. So, if two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve simultaneous requests of the same priority level.

Table below summarizes the interrupt sources, flag bits, vector address, enable bits, priority bits, arbitration ranking, and whether each interrupt may wake up the CPU from Power Down mode.

Source	Flag	Vector address	Enable bit	Flag cleared by	Priority bit	Arbitration ranking	Power-down wakeup
External Interrupt 0	IE0	0003H	EX0 (IE.0)	Hardware, Software	IP0H.0, IP0.0	1(highest)	Yes
Brownout Detect	BOF	002BH	EBO (EIE.6)	Hardware	IP1H.6, IP1.6	2	Yes
Watchdog Timer	WDIF	0053H	EWDI (EIE.4)	Software	IP1H.4, IP1.4	3	Yes
Timer 0 Overflow	TF0	000BH	ET0 (IE.1)	Hardware, Software	IP0H.1, IP0.1	4	No
I2C Interrupt	SI + TIF	0033h	EI2 (EIE.0)	Software	IP1H.0, IP1.0	5	No
External Interrupt 1	IE1	0013H	EX1 (IE.2)	Hardware, Software	IP0H.2, IP0.2	6	Yes
KBI	KBF	003BH	EKB (EIE.1)	Software	IP1H.1, IP1.1	7	Yes
Timer 1 Overflow	TF1	001BH	ET1 (IE.3)	Hardware, Software	IP0H.3, IP0.3	8	No
UART	RI + TI	0023H	ES (IE.4)	Software	IP0H.4, IP0.4	9	No

Timer 2 Overflow/ Match	TF2 + EXF2	0043H	ET2 (IE.5)	Software	IP0H.5, IP0.5	10	No
Input Capture	CPTF0	006BH	ECPTF (EIE.7)	Software	IP1H.7, IP1.7	11	No

Table 18- 3: Summary of interrupt sources

Note: 1. The Watchdog Timer can wake up Power Down Mode when its clock source is used internal RC.

18.3 Interrupt Response Time

The response time for each interrupt source depends on several factors, such as the nature of the interrupt and the instruction underway. In the case of external interrupts $\overline{INT0}$ to $\overline{INT1}$, they are sampled at C3 of every machine cycle and then their corresponding interrupt flags IEx will be set or reset. The Timer 0 and 1 overflow flags are set at C3 of the machine cycle in which overflow has occurred. These flag values are polled only in the next machine cycle. If a request is active and all three conditions are met, then the hardware generated LCALL is executed. This LCALL itself takes four machine cycles to be completed. Thus there is a minimum time of five machine cycles between the interrupt flag being set and the interrupt service routine being executed.

A longer response time should be anticipated if any of the three conditions are not met. If a higher or equal priority is being serviced, then the interrupt latency time obviously depends on the nature of the service routine currently being executed. If the polling cycle is not the last machine cycle of the instruction being executed, then an additional delay is introduced. The maximum response time (if no other interrupt is in service) occurs if the device is performing a write to IE, EIE, IP0, IP0H, IP1 or IP1H and then executes a MUL or DIV instruction. From the time an interrupt source is activated, the longest reaction time is 12 machine cycles. This includes 1 machine cycle to detect the interrupt, 2 machine cycles to complete the IE, EIE, IP0, IP0H, IP1 or IP1H access, 5 machine cycles to complete the MUL or DIV instruction and 4 machine cycles to complete the hardware LCALL to the interrupt vector location.

Thus in a single-interrupt system the interrupt response time will always be more than 5 machine cycles and not more than 12 machine cycles. The maximum latency of 12 machine cycle is 48 clock cycles. Note that in the standard 8051 the maximum latency is 8 machine cycles which equals 96 machine cycles. This is a 50% reduction in terms of clock periods.

18.4 Interrupt Inputs

N79E352(R) has two individual interrupt inputs as well as the Keyboard Interrupt function. The latter is described separately elsewhere in this section. Two interrupt inputs are identical to those present on the standard 80C51 microcontroller.

The external sources can be programmed to be level-activated or transition-activated by setting or clearing bit IT1 or IT0 in Register TCON. If ITn = 0, external interrupt n is triggered by a detected low at the INTn pin. If ITn = 1, external interrupt n is edge triggered. In this mode if successive samples of the /INTn pin show a high in one cycle and a low in the next cycle, interrupt request flag IEn in TCON is set, causing an interrupt request.

Since the external interrupt pins are sampled once each machine cycle, an input high or low should hold for at least 6 CPU Clocks to ensure proper sampling. If the external interrupt is high for at least one machine cycle, and then hold it low for at least one machine cycle. This is to ensure that the

transition is seen and that interrupt request flag IEn is set. IEn is automatically cleared by the CPU when the service routine is called.

If the external interrupt is level-activated, the external source must hold the request active until the requested interrupt is actually generated. If the external interrupt is still asserted when the interrupt service routine is completed another interrupt will be generated. It is not necessary to clear the interrupt flag IEn when the interrupt is level sensitive, it simply tracks the input pin level.

If an external interrupt is enabled when the device is put into Power Down or Idle mode, the interrupt will cause the processor to wake up and resume operation. Refer to the section on Power Management for details.

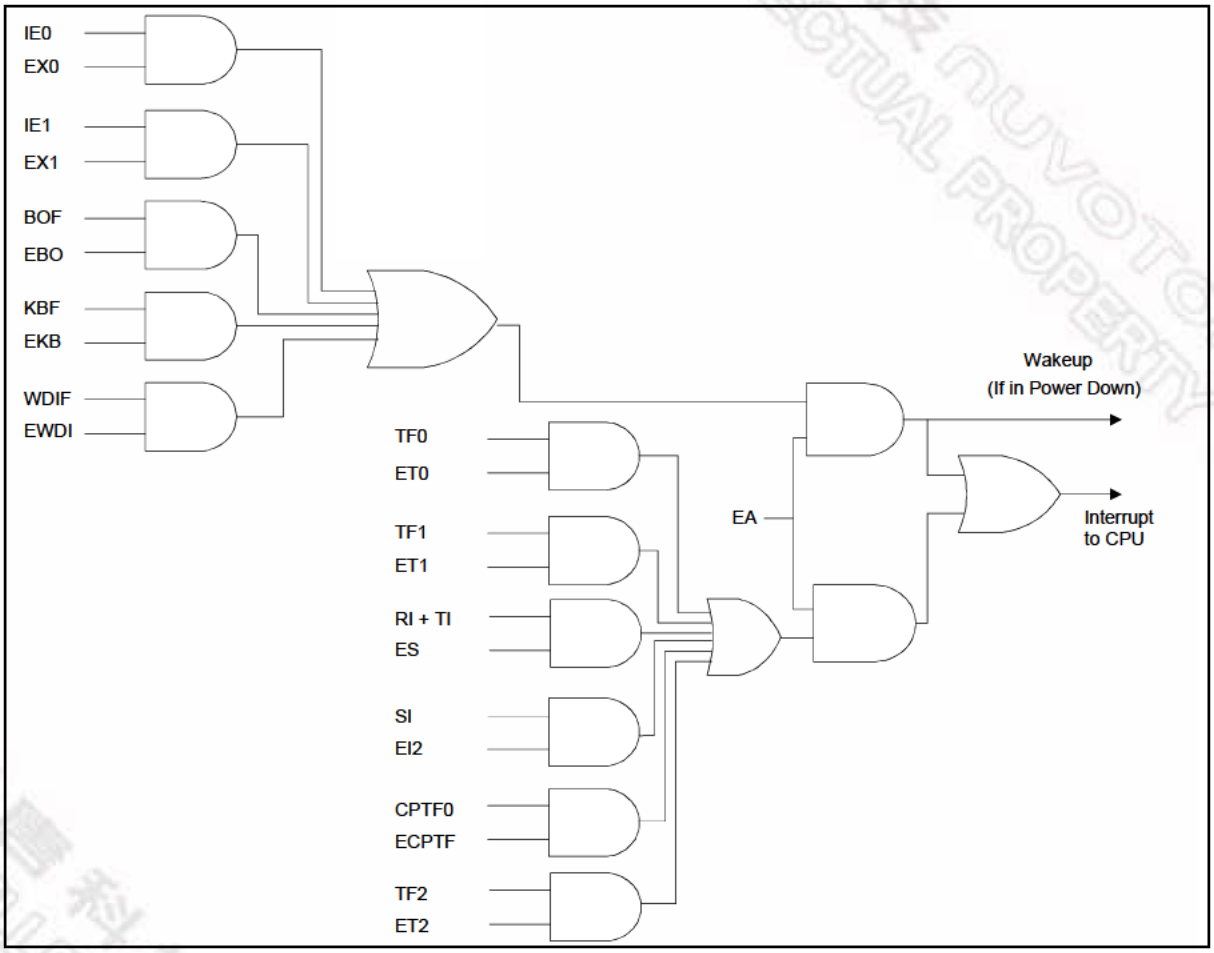


Figure 18- 1: Interrupt inputs

19. KEYBOARD FUNCTION

The N79E352(R) provideds 8 keyboard interrupt function to detect keypad status which key is acted, and allow a single interrupt to be generated when any key is pressed on a keyboard or keypad

connected to specific pins of the N79E352(R), as shown below figure. This interrupt may be used to wake up the CPU from Idle or Power Down modes, after chip is in Power Down or Idle Mode.

Keyboard function is supported through by Port 0. It can allow any or all pins of Port 0 to be enabled to cause this interrupt. Port pins are enabled by the setting of bits of KBI0 ~ KBI7 in the KBI register, as shown below figure. The Keyboard Interrupt Flag (KBF) in the AUXR1 register is set when any enabled pin is triggered while the KBI interrupt function is active, and the low pulse must be more than 1 machine cycle, an interrupt will be generated if it has been enabled. The KBF bit set by hardware and must be cleared by software. In order to determine which key was pressed, the KBI will allow the interrupt service routine to poll port 0.

The N79E352(R) has addition SFR KBL level configuration register to control either a low or high level trigger.

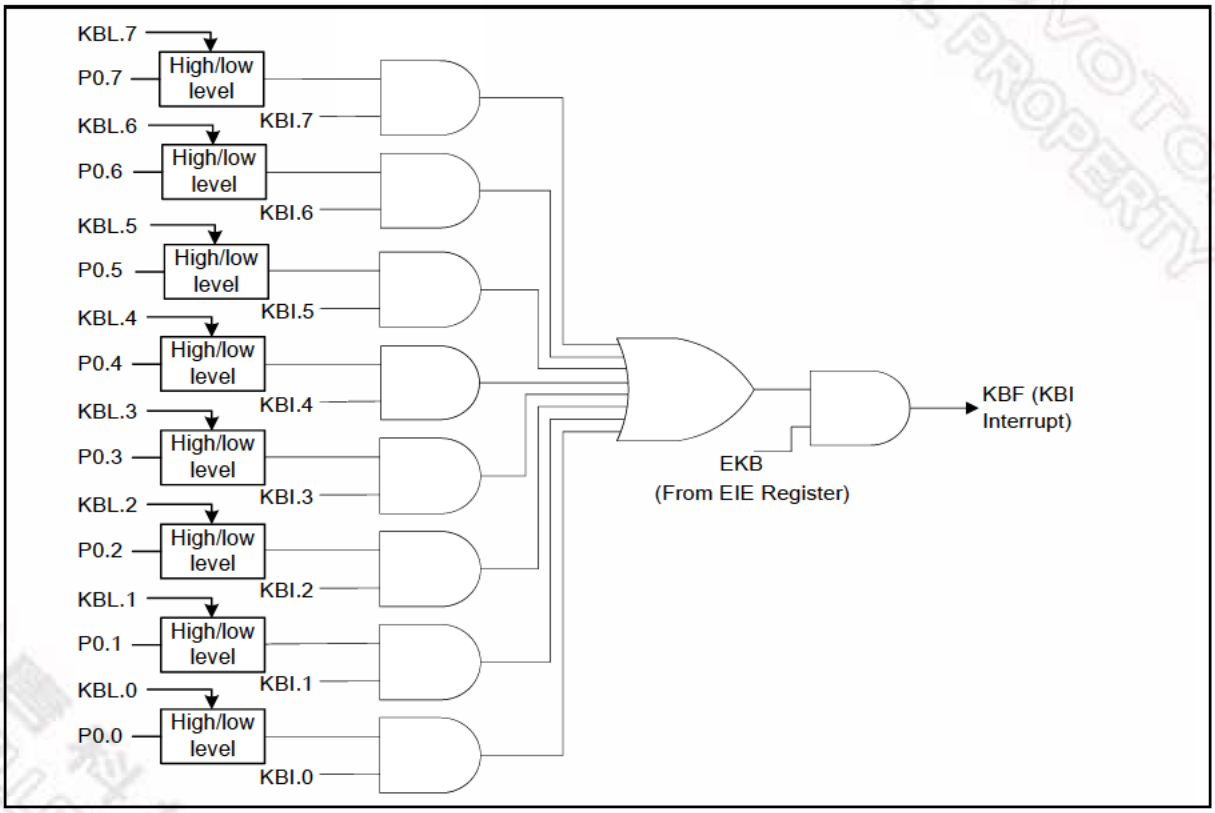


Figure 19-1: KBI inputs

20. INPUT CAPTURE

The input capture modules are function to detect/measure pulse width and period of a square wave. It supports one capture inputt with digital noise rejection filter. The modules are configured by CAPCON0, CAPCON1 and T2MOD SFR registers. Input Capture has its own edge detector but share with Timer 0. The Input Capture is a schmitt trigger pin. For this operation it basically consists of;

- Capture module function block
- Timer 0 (mode 0 and 1) block

The capture module block consists of 2 bytes capture registers, noise filter and programmable edge triggers. Noise Filter is used to filter the unwanted glitch or pulse on the trigger input pin. The noise filter can be enabled through bit ENF0 (CAPCON1). If enabled, the capture logic required to sample 4 consecutive same capture input value in order to recognize an edge as a capture event. A possible implementation of digital noise filter is as follow;

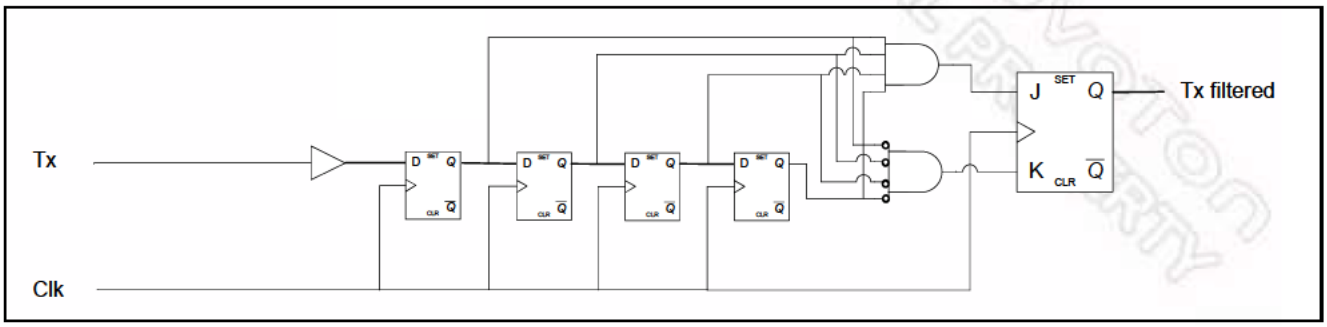


Figure 20-1: Noise filter

The interval between pulses requirement for input capture is 1 machine cycle width, which is the same as the pulse width required to guarantee a trigger for all trigger edge mode. For less than 3 system clocks, anything less than 3 clocks will not have any trigger and pulse width of 3 or more but less than 4 clocks will trigger but will not guarantee 100% because input sampling is at stage C3 of the machine cycle.

The trigger option is programmable through CCT0[1:0] (CAPCON0[3:2]). It supports positive edge, negative edge and both edge triggers. The capture module consists of an enable, ICEN0 (T2MOD.4).

Timer/Counter 0 needs to be configured as mode 0 or 1 recommanded. It's content will transfer to CCL0 and CCH0 SFR when CPTF0 is set. If ICEN0 is enabled, each time the external pin trigger, the content TL0 and TH0 (from Timer 0 block) will be captured/transferred into the capture registers, CCL0 and CCH0, depending which external pin trigger. This action also causes the CPTF0 flag bit in CAPCON1 to be set, which will also generate an interrupt (if enabled by ECPTF bit in SFR EIE.7). The flag is set by hardware and cleared by software.

Setting the T0CC bit (CAPCON1.6), will allow hardware to reset timer 0 automatically after the value of TL0 and TH0 have been captured.

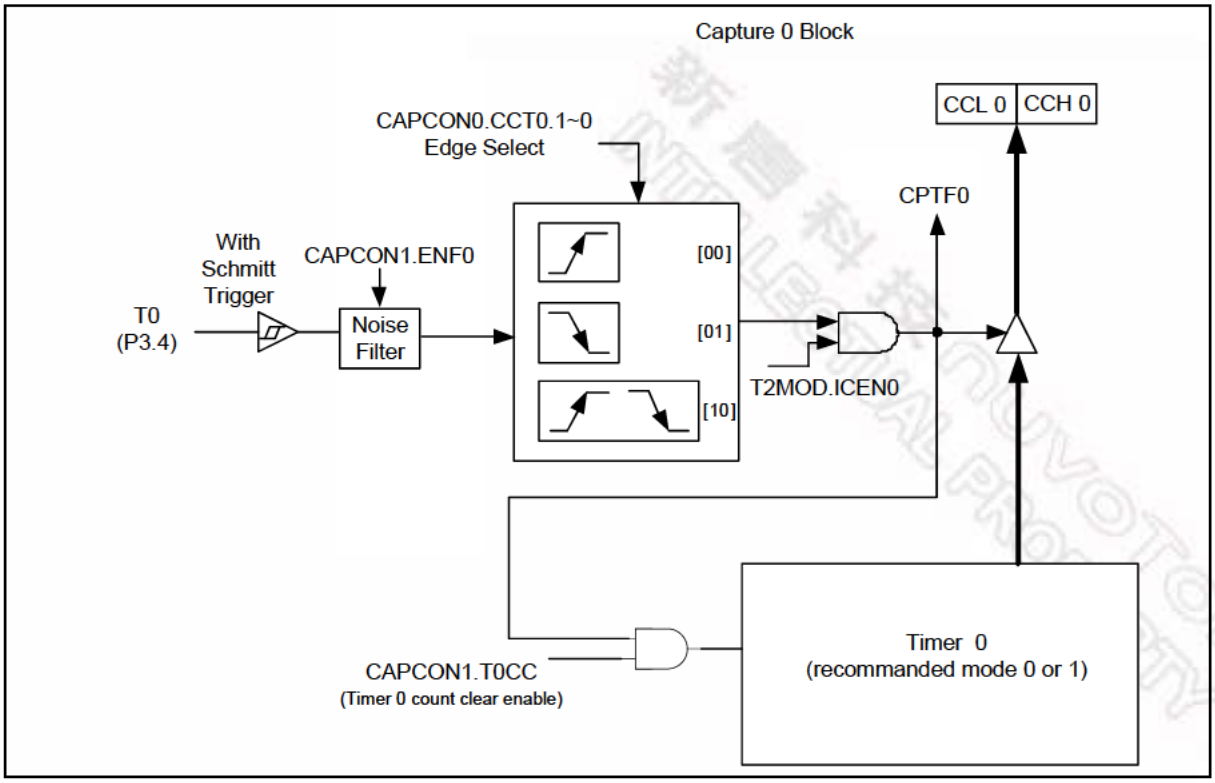


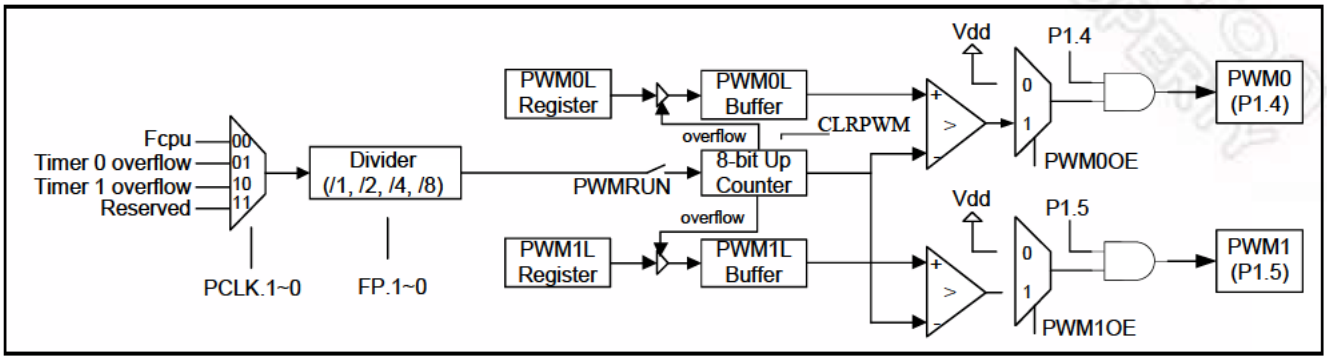
Figure 20-2: Input capture block

21. PULSE WIDTH MODULATED OUTPUTS (PWM)

The N79E352(R) contains two Pulse Width Modulated (PWM) channels which generate pulses of programmable length and interval. The output for PWM0 is on P1.4 and PWM1 on P1.5. After chip reset the internal output of the each PWM channel is a "1" (if PRHI=1). The PWM block diagram is shown as below figure. The interval between successive outputs is controlled by a 8–bit up-counter which uses the selectable clock sources. The clock sources supported are cpu clock, timer 0 overflow and timer 1 overflow, selectable by PWMCON3.PCLK.1~0 bits. The clock sources can be further divided with programmable PWMCON3.FP1~0 bits. When the counter reaches overflow, it is reloaded with zero.

The width of each PWM output pulse is determined by the value in the appropriate Compare registers, PWMnL (n=0,1). When the counter described above matches compare register value the PWM output is forced low. It remains low until the counter value overflow. The number of clock pulses that the PWMn output is low is given by:

t_{LO} = (FFh – PWMn+1)



A compare value of all zeroes, 00H, causes the output to remain permanently high. A compare value of all ones, FFH, results in the PWM output remaining permanently low.

The overall functioning of the PWM module is controlled by the contents of the PWMCON1 and PWMCON3 registers. The operation of most of the control bits are straightforward. The transfer Compare registers to the buffer registers is controlled by 8-bit counter overflow, while PWMCON1.7 (PWMRUN) allows the PWM to be either in the run or idle state. It has a CLRPWM bit to clear 8-bt up counter.

When the PWMRUN is cleared, the PWM outputs take on the state they had just prior to the bit being cleared. In general this state is not known. In order to place the outputs in a known state when PWMRUN is cleared the Compare registers can be written to either the "all 1" or "all 0" so the output will have the output desired when the counter is halted.

Note:

During PWM initial run, user is recommended to configure proper PWMn and/or PWM output pin (default high) follow by setting PWMRUN and CLRPWM bits, prior to enable PWMnOE. This is to avoid unexpected PWM output.

22. I/O PORT

N79E352(R) has four 8 bits I/O ports; port 0, port 1, port 2, port 3, one partial port 4; P4.0 to P4.3 and one partial port 5; P5.0 to P5.1. All pins of I/O ports (except port4) can be configured to one of four types by software. User may configure the mode type for the above port pin by programming PxMy SFRs.

Port 4 support only quasi mode.

PXM1.Y	PXM2.Y[Note]	PORT INPUT/OUTPUT MODE
0	0	Quasi-bidirectional.
0	1	Push-Pull
1	0	Input Only (High Impedance) PORTS.PxS=0, TTL input PORTS.PxS=1, Schmitt input
1	1	Open Drain

Table 22-1: I/O port configuration table

Note: X = 0-3 and 5. Y = 0-7.

In addition, port default mode is also configurable through CONFIG0.PMODE bit. When PMODE = 1, ports 1~3 and 5 will default to quasi mode upon all reset. If PMODE = 0, ports 1~3 and 5 will default to open drain mode upon all reset. See table below.

PORTS	CONFIG0.PMODE	UPON RESET	PXM1,2 RESET VALUE
P0	X	Open Drain	P0M1,2 = 1111 1111b
P1~3	1	Quasi	P(1~3)M1,2 = 0000 0000b
	0	Open Drain	P(1~3)M1,2 = 1111 1111b
P4	X	Quasi	Not available.
P5[1]	1	Quasi	P5M1 = xxxx x000b P5M2 = xxxx xx00b
	0	Open Drain	P5M1 = xxxx x011b P5M2 = xxxx xx11b

Table 22-2: Default port mode configuration by CONFIG0.PMODE bit.

Note: 1. Product configured to run internal rc.

All port pins can be determined to high or low after reset by configure PRHI bit in the CONFIG0 register.

Besides P4 is permenant Schmitt trigger intput, each I/O port of N79E352(R) may be selected to use TTL level inputs or Schmitt inputs by P(n)S bit on PORTS SFR register; where n is 0, 1, 2, 3 or 5. When P(n)S is set to 1, Ports are selected Schmitt trigger inputs on Port(n).

22.1 Quasi-Bidirectional Output Configuration

The default port output configuration for standard N79E352(R) I/O ports is the quasi-bidirectional output that is common on the 80C51 and most of its derivatives. This output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the pin is pulled low, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes. One of these pull-ups, called the "very weak" pull-up, is turned on whenever the port latch for the pin contains a logic 1. The very weak pull-up sources a very small current that will pull the pin high if it is left floating.

A second pull-up, called the "weak" pull-up, is turned on when the port latch for the pin contains a logic 1 and the pin itself is also at a logic 1 level. This pull-up provides the primary source current for a quasi-bidirectional pin that is outputting a 1. If a pin that has a logic 1 on it is pulled low by an external device, the weak pull-up turns off, and only the very weak pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current to overpower the weak pull-up and take the voltage on the port pin below its input threshold.

The third pull-up is referred to as the "strong" pull-up. This pull-up is used to speed up low-to-high transitions on a quasi-bidirectional port pin when the port latch changes from a logic 0 to a logic 1. When this occurs, the strong pull-up turns on for a brief time, two CPU clocks, in order to pull the port pin high quickly. Then it turns off again. The quasi-bidirectional port configuration is shown as below.

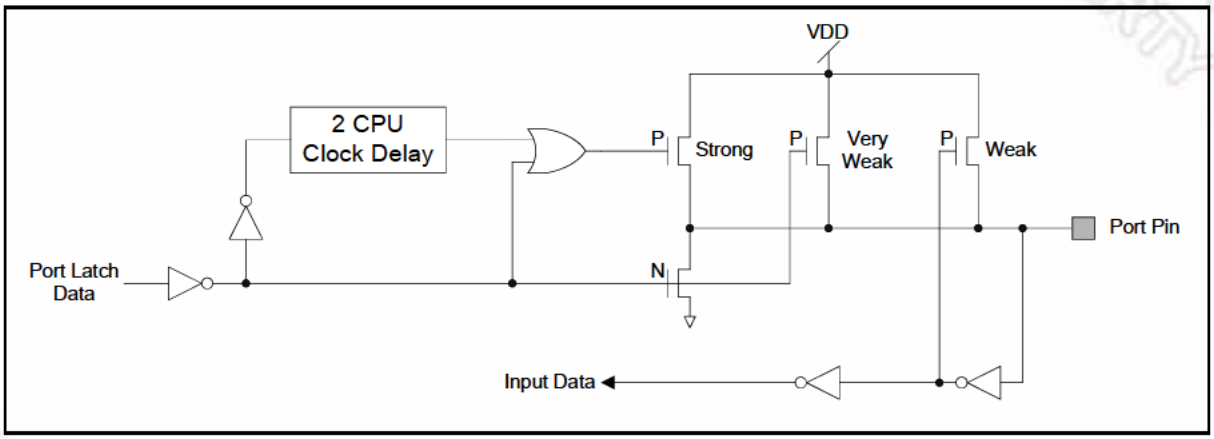


Figure 22-1: Quasi-Bidirectional Output

22.2 Open Drain Output Configuration

The open drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to VDD. The pull-down for this mode is the same as for the quasi-bidirectional mode. The open drain port configuration is shown as below.

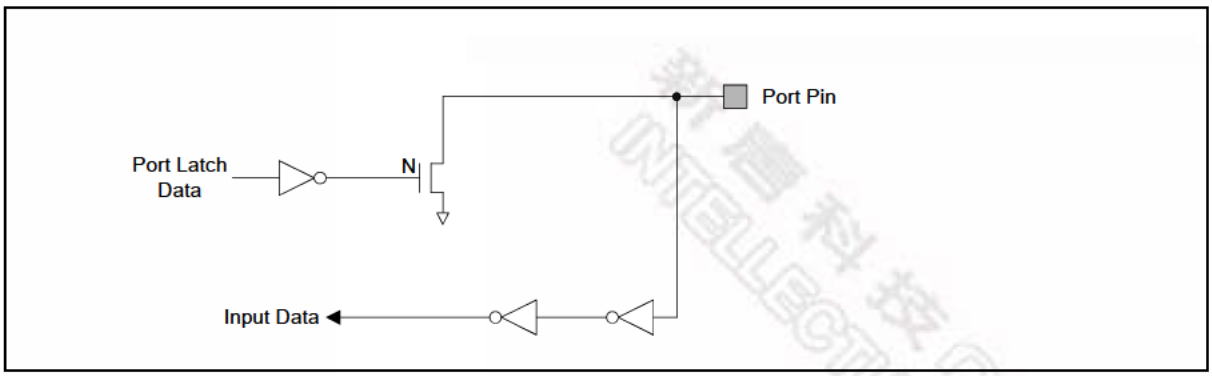


Figure 22-2: Open Drain Output

22.3 Push-Pull Output Configuration

The push-pull output configuration has the same pull-down structure as both the open drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. The push-pull port configuration is shown below.

The value of port pins at reset is determined by the PRHI bit in the CONFIG0 register. Ports may be configured to reset high or low as needed for the application. When port pins are driven high at reset, they are in quasi-bidirectional mode and therefore do not source large amounts of current. Every output on the device may potentially be used as a 20mA sink LED drive output. However, there is a maximum total output current for all ports which must not be exceeded.

All ports pins of the device have slew rate controlled outputs. This is to limit noise generated by quickly switching output signals. The slew rate is factory set to approximately 10 ns rise and fall times.

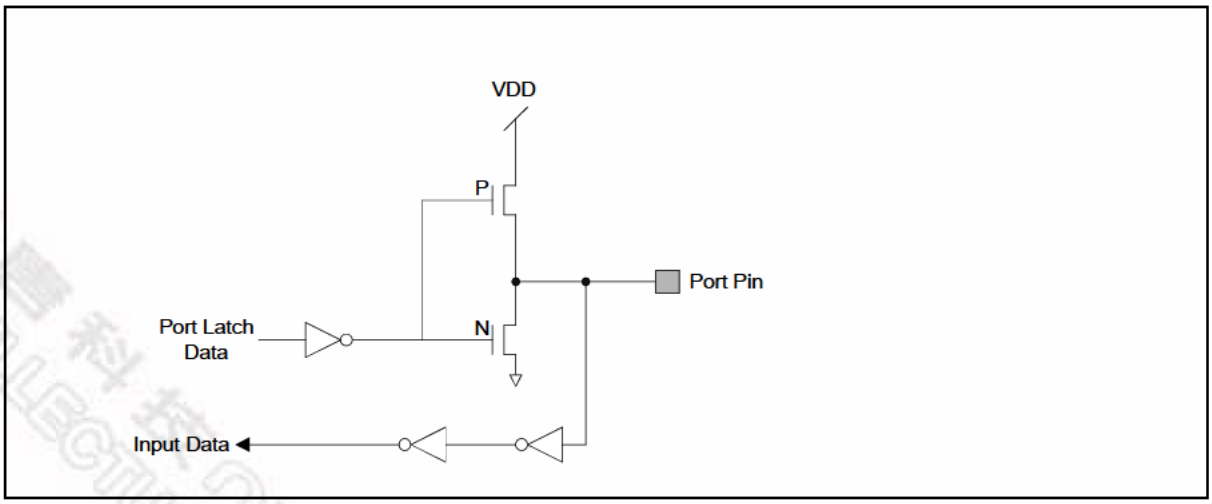


Figure 22-3: Push-Pull Output

22.4 Input Only Mode

The input only port configuation is show in figure 21-4, it is a schmitt-triggered input or TTL input.

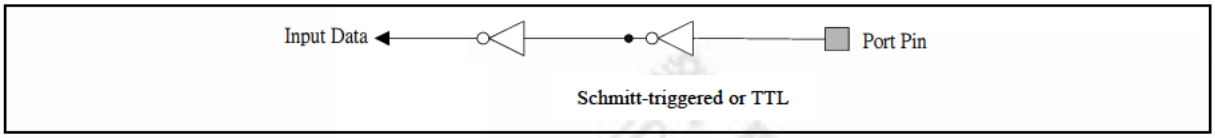


Figure 22-4: Push-Pull Output

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23. OSCILLATOR

N79E352(R) provides three oscillator input option. These are configured at CONFIG register (CONFIG0) that include On-Chip RC Oscillator Option, External Clock Input Option and Crystal Oscillator Input Option. The Crystal Oscillator Input frequency may be supported from 4MHz to 24MHz, and without capacitor or resister.

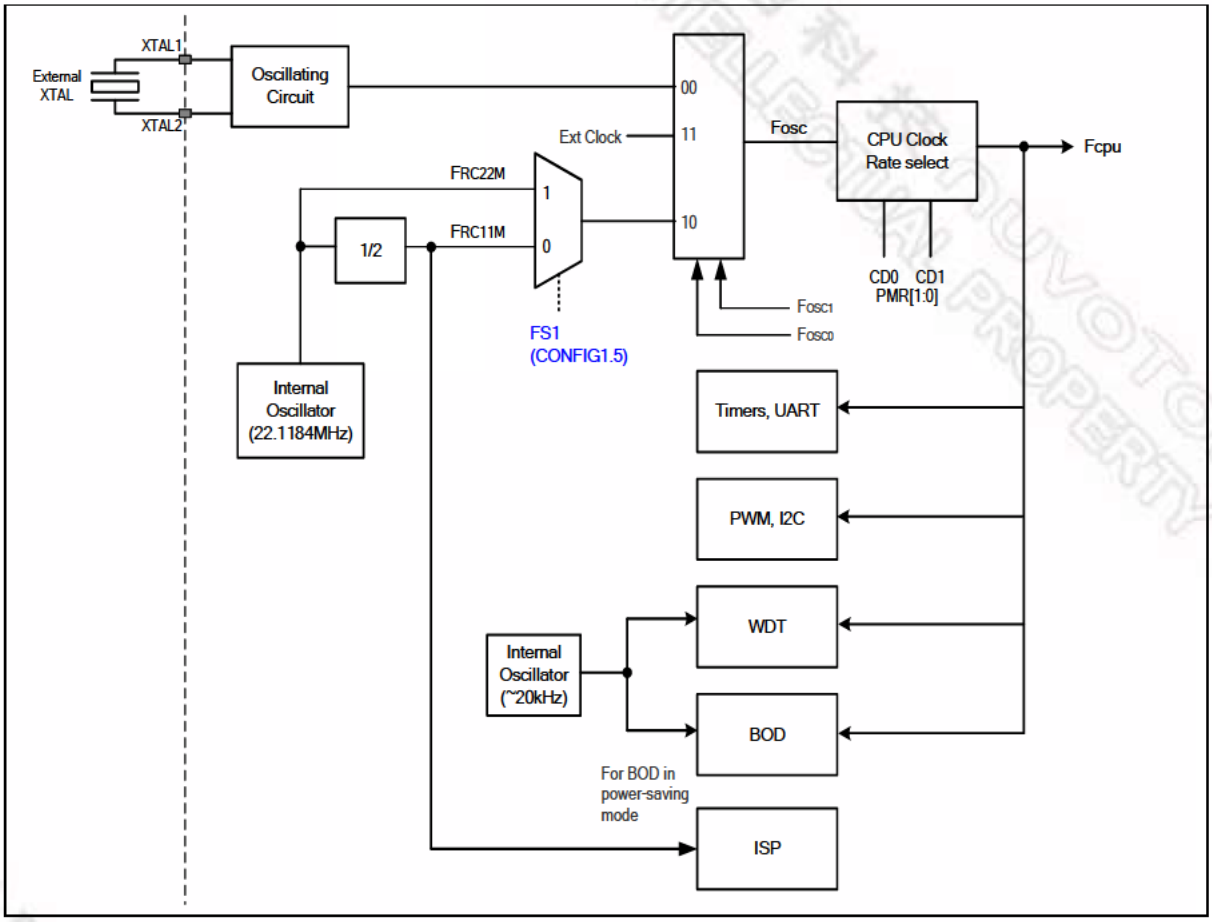


Figure 23-1: Oscillator

23.1 On-Chip RC Oscillator Option

The On-Chip RC Oscillator is fixed at 11.0592MHz or 22.1184MHz (selectable by FS1 config bit) ±2% for N79E352R, ±25% for N79E352 frequency to support clock source. When FOSC1, FOSC0 = 01b, the On-Chip RC Oscillator is enabled.

23.2 External Clock Input Option

The clock source pin (XTAL1) is from External Clock Input by FOSC1, FOSC0 = 11b, and frequency range is ffrom 0Hz up to 24MHz.

The device supports a clock output function when either the on-chip RC oscillator or external clock input options are selected. This allows external devices to synchronize to the device. When enabled, via the ENCLK bit in the P5M1 register, the clock output appears on the XTAL2/CLKOUT pin whenever the on-chip oscillator is running, including in Idle Mode. The frequency of the clock output is 1/4 of the CPU clock rate. If the clock output is not needed in Idle Mode, it may be turned off prior to entering

Idle, saving additional power. The clock output may also be enabled when the external clock input option is selected.

23.3 CPU Clock Rate select

The CPU clock of N79E352(R) may be selected by the PMR.CD0/1 bits. If (CD1,CD0) = 01b, the CPU clock is running at 4 CPU clock per machine cycle, and without any division from source clock (Fosc). This frequency division function affect all peripheral timings as they are all sourcing from the CPU clock(Fcpu). The following table shows the PMR.CD1/0 bits definition.

CD1,	CD0	Clocks/machine Cycle
0	x	4
1	0	64
1	1	1024

CD0/1 definitions

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24. POWER MONITORING

In order to prevent incorrect operation during power up and power drop, the N79E352(R) provides two power monitor function that are Power-On Detect and Brownout Detect.

24.1 Power On Detect

The Power–On Detect function is a design to detect power up after power voltage reaches to a level where Brownout Detect can work. After power on detect, the POR (WDCON.6) will be set to "1" to indicate an initial power up condition. The POR flag will be cleared by software.

24.2 Brownout Detect and Reset

The N79E352(R) has an on-chip Brown-out Detection circuit for monitoring the V_{DD} level during operation by comparing it to a programmable brownout trigger level. There are 4 brownout trigger levels available for wider voltage applications. The 3 nominal levels are 2.6V, 3.8V and 4.5V (programmable through BOV.1-0 bits). When V_{DD} drops to the selected brownout trigger level (V_{BOR}), the brownout detection logics will either reset the CPU until the V_{DD} voltage raises above V_{BOR} or requests a brownout interrupt at the moment that V_{DD} falls and raises through V_{BOR}. The brownout detection circuits also provides a low power brownout detection mode for power saving. When LPBOV=1, the brownout detection repeatly senses the voltage for $64/f_{BRC}$ then turn off detector for $960/f_{BRC}$ (f_{BRC} = internal rc frequency), if V_{DD} voltage still below brownout trigger level. f_{BRC}, the frequency of built-in RC oscillator is approximately 20KHz+/-100%.

The Brownout Detect block is shown in Figure 24-1.

BOV1	BOV0	Brownout Voltage
0	x	Brownout voltage is 2.6V
1	0	Brownout voltage is 3.8V
1	1	Brownout voltage is 4.5V

Brownout Voltage Selection

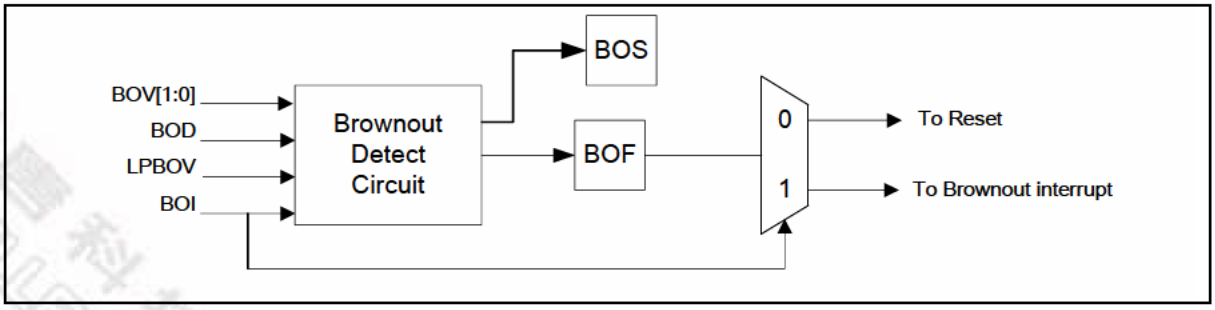


Figure 24-1: Brown-out Detect Block

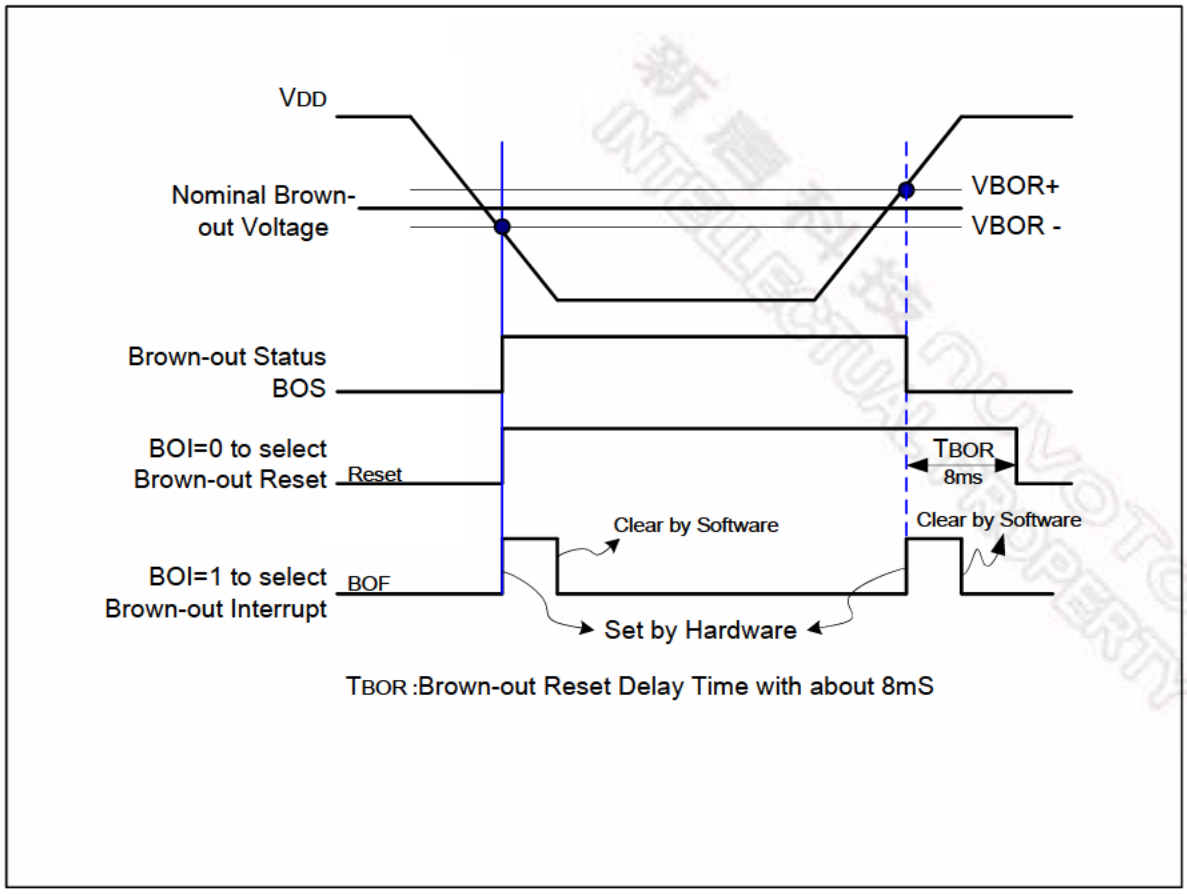


Figure 24-2: Brown-out Voltage Detection

25. ICP(IN-CIRCUIT PROGRAM) FLASH PROGRAM

The ICP(In-Circuit-Program) mode is another approach to access the Flash EPROM. There are only 3 pins needed to perform the ICP function. One is mode input, shared with RST pin, which must be kept in Vdd voltage in the entire ICP working period. One is clock input, shared with P1.7, which accepts serial clock from external device. Another is data I/O pin, shared with P1.6, that an external ICP program tool shifts in/out data via P1.6 synchronized with clock(P1.7) to access the Flash EPROM of N79E352(R).

(Note, While PRHI=0, P1.6, P1.7 are still quasi high during reset period. During reset period , P1.6, P1.7 cann't switch to open-drain by setting config).

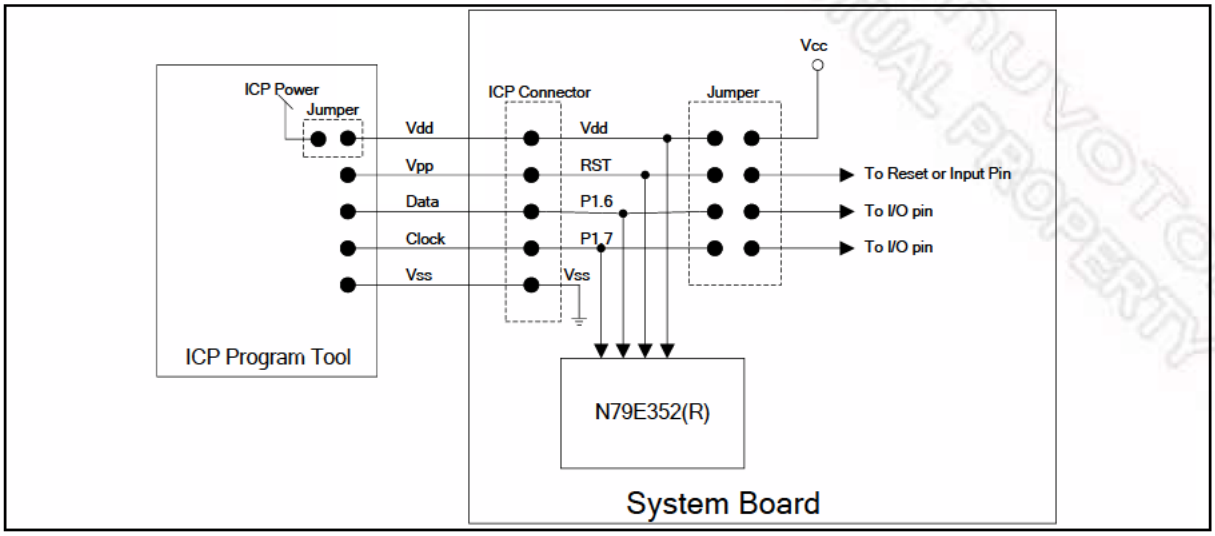


Figure 26-1: ICP Writer Tool connector pin assign

Note:

1. When using ICP to upgrade code, the RST, P1.6 and P1.7 must be taken within design system board.
2. After program finished by ICP, to suggest system power must power off and remove ICP connector then power on.
3. It is recommended that user performs erase function and programming configure bits continuously without any interruption.
4. During ICP mode, all PWM pins will be tri-stated.

26. CONFIG BITS

The N79E352(R) has two CONFIG bits (CONFIG0 located at FB00h, CONFIG1 located at FB01h) that must be defined at power up and can not be set the program after start of execution. Those features are configured through the use of two flash EPROM bytes, and the flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of flash EPROM (CONFIG1) and those operations on it are described below.

26.1 CONFIG0

7	6	5	4	3	2	1	0
WDTCK	PMODE	PRHI	-	CBOD	BPFR	Fosc 1	Fosc 0

WDTCK : Watchdog Timer Clock Selection Bit.
PMODE : Port MODE Bit.
PRHI : Port Reset High Bit.
CBOD : Config Brownout Detect Enable Bit.
BPFR : Bypass Clock Filter Bit.
Fosc1 : CPU Oscillator Type Select Bit 1.
Fosc0 : CPU Oscillator Type Select Bit 0.

Figure 25-1: Config0 register bits

BIT	NAME	FUNCTION
7	WDTCK	Clock source of Watchdog Timer select bit: 0: The internal 20KHz RC oscillator clock is for Watchdog Timer clock used. 1: The uC clock is for Watchdog Timer clock used.
6	PMODE	Port Mode Type select bit: 0: Port 1~3 and 5 reset to open drain mode. 1: Port 1~3 and 5 reset to quasi mode.
5	PRHI	Port Reset High or Low select bit: 0: Port reset to low state. 1: Port reset to high state. Note: For product to run external program (/EA=0), user need to ensure PRHI is set to 1.
4	-	Reserved.
3	CBOD	Config Brownout Detect Enable bit 0: Disable Brownout Detect. 1: Enable Brownout Detect.
2	BPFR	Bypass Clock Filter. 0: Disable Clock Filter. 1: Enable Clock Filter.
1	Fosc1	CPU Oscillator Type select bit 1.

0	Fosc0	CPU Oscillator Type select bit 0.

Oscillator Configuration bits:

Fosc1	Fosc0	OSC source
0	0	4MHz ~ 24MHz crystal
0	1	Internal RC Oscillator (FS1 bit in CONFIG1.5 will determine either 11.0592MHz or 22.1184MHZ)
1	0	Reserved
1	1	External Oscillator in XTAL1; XALT2 is in Tri-state

26.2 CONFIG1

7	6	5	4	3	2	1	0
C7	C6	FS1	-	CBOV.1-0		C1	-

C7 : 8/4K Flash EPROM Code Lock Bit
C6 : 512/256/128/64 byte Data Lock Bit
FS1 : Internal RC 11.0592MHz/22.1184MHz Selection Bit
CBOV.1-0 : Brownout Level Selection Bits
C1 : Movc Inhibit Enable Bit

Figure 25-2: Config1 register bits

C7: 8K Flash EPROM Lock bit

This bit is used to protect the customer's program code. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the Flash EPROM data and CONFIG Registers can not be accessed again.

C6: 128 byte Data Flash EPROM Lock bit

This bit is used to protect the customer's 128 bytes of data code. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the 128 bytes of Flash EPROM data and CONFIG Registers can not be accessed again.

Bit 7	Bit 6	Function Description
1	1	Both security of 8KB program code and 128 Bytes data area are not locked. They can be erased, programmed or read by Writer or JTAG mode.
0	1	The 8KB program code area is locked. It can not be read and written by Writer or JTAG mode. The 128 Bytes data area can be program or read. The bank erase is invalid.
1	0	Not supported.
0	0	Both security of 8KB program code and 128 Bytes data area are locked. They can not be read and written by Writer or JTAG mode.

FS1: Internal Oscillator selection bit

This bit is used to select internal oscillator.

FS1	Internal Oscillator Output
0	11.0592MHz
1	22.1184MHz (default)

Internal Oscillator Selection Table

CBOV.1-0: Brownout level selection bits

These bits are used to select brownout voltage level.

CBOV.1	CBOV.0	Brownout Voltage
1	x	Brownout voltage is 2.6V
0	1	Brownout voltage is 3.8V
0	0	Brownout voltage is 4.5V

C1: MOVC inhibit enable bit

MOVC inhibit enable bit	MOVC access
0	The MOVC instruction in external memory cannot access the code in internal memory.
1	No restriction.

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

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27. ELECTRICAL CHARACTERISTICS

27.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITION	RATING	UNIT
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Operating Temperature	TA	-40	+85	°C
Storage Temperature	Tst	-55	+150	°C
Sink current	ISK		90	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

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27.2 D.C. Characteristics

(TA = -40~85°C, unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Voltage	V_{DD}	2.4		5.5	V	V_{DD}=4.5V ~ 5.5V @ 24MHz V_{DD}=2.7V ~ 5.5V @ 12MHz V_{DD}=2.4V ~ 5.5V @ 4MHz
Operating Current	I_{DD1}			5	mA	No load, RST = V_{DD}, V_{DD}= 3.0V @ 11.0592MHz
	I_{DD2}			15	mA	No load, RST = V_{DD}, V_{DD}= 5.0V @ 22.1184MHz
Idle Current	I_{IDLE}			4	mA	No load, V_{DD} = 3.0V @ 11.0592MHz
Power Down Current	I_{PWDN}		1	5	μA	No load, V_{DD} = 5.5V @ Disable BOV function
			1	5	uA	No load, V_{DD} = 3.0V @ Disable BOV function
Input / Output						
Input Current P0, P1, P2, P3, P4, P5	I_{IN1}	-50	-	+10	μA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}
Input Current P1.5(RST pin)[1]	I_{IN2}	-48	-32	-24	μA	V_{DD} = 5.5V, V_{IN} = 0.45V
Input Leakage Current P0, P1, P2, P3, P5 (Open Drain)	I_{LK}	-10	-	+10	μA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current P0, P1, P2, P3, P4, P5	I_{TL} [*3]	-450	-	-246	μA	V_{DD} = 5.5V, V_{IN}<2.0V
		-93	-	-56		V_{DD}=2.4 Vin = 1.3v
Input Low Voltage P0, P1, P2, P3, P4, P5 (TTL input)	V_{IL1}	0	-	1.0	V	V_{DD} = 4.5V
		0	-	0.6 1.0		V_{DD} = 2.4V
Input High Voltage P0, P1, P2, P3, P4, P5 (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} = 2.4V
Input Low Voltage XTAL1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V
Input High Voltage XTAL1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V
Negative going threshold (Schmitt input)	V_{ILS}	-0.5	-	0.3V_{DD}	V	
Positive going threshold (Schmitt input)	V_{IHS}	0.7V_{DD}	-	V_{DD}+0.5	V	
Hysteresis voltage	V_{HY}		0.2V_{DD}		V	
Input Low Voltage RST [*1]	V_{IL21}	-	1.0	1.6	V	V_{DD}=4.5V

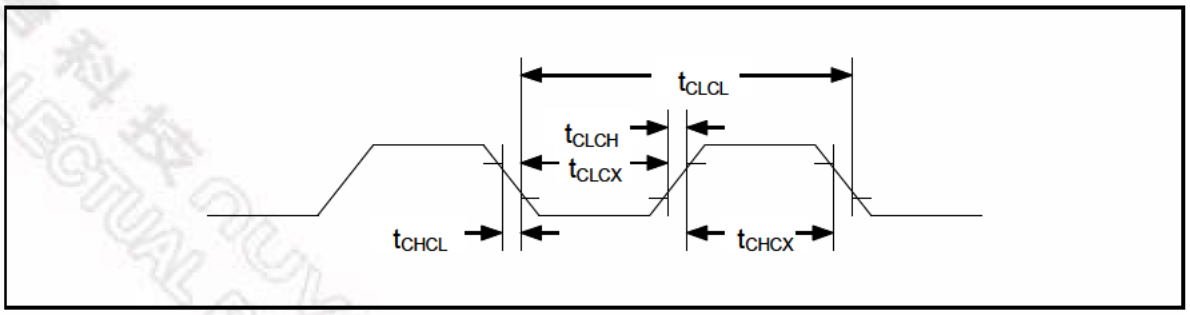
	V_{IL22}	-	0.7	0.8	V	V_{DD}=2.7V
Input High Voltage RST [*1]	V_{IH21}	3.5	2.3	VDD+0.2	V	V_{DD}=5.5V
	V_{IH22}	2	1.5	VDD+0.2	V	V_{DD}=2.7V
Source Current P0, P1, P2, P3, P5 (PUSH-PULL Mode)	I_{SR1}	-16	-26	-36	mA	V_{DD} = 4.5V, V_S = 2.4V
		-5	-7.9	-11	mA	V_{DD} = 2.4V, V_S = 2.0V
Source Current P0, P1, P2, P3, P4, P5 (Quasi-bidirectional Mode)	I_{SR2}	-150	-210	-360	µA	V_{DD} = 4.5V, V_S = 2.4V
		-39	-53	-69	µA	V_{DD} = 2.4V, V_S = 2.0V
Sink Current P0, P1, P2, P3, P4, P5 (Quasi-bidirectional and PUSH-PULL Mode)	I_{SK2}	13	18.5	24	mA	V_{DD} = 4.5V, V_S = 0.45V
		9	15	21		V_{DD} = 2.4V, V_S = 0.45V
Brownout voltage with BOV[1:0] =0xb	$V_{BO2.4}$	2.55	2.6	2.85	V	
Brownout voltage with BOV[1:0] =10b	$V_{BO3.8}$	3.65	3.8	3.95	V	
Brownout voltage with BOV[1:0] =11b	$V_{BO4.5}$	4.35	4.5	4.65	V	
Hysterisis range of BOD voltage	V_{Bh}	35	-	150	mV	V_{DD} = 2.4V~5.5V, (LPBOD,BOI) = (0,x) or (1,0)
		10	-	60	mV	V_{DD} = 2.4V~5.5V, (LPBOD,BOI)=(1,1)
Sink current [*2] P0, P2, ALE, /PSEN	Isk31	-16	-26	-36	mA	V_{DD}=4.5V, Vs = 0.45V
	Isk32	-5	-7.9	-11	mA	V_{DD}=2.7V, Vs = 0.45V
Source current [*2] P0, P2, ALE, /PSEN	Isr31	13	18.5	24	mA	V_{DD}=4.5V, Vs = 2.4V
	Isr32	9	15	21	mA	V_{DD}=2.7V, Vs = 2.0V

Notes: *1. RST pin is a Schmitt trigger input. RST has internal pull-low resistor.

*2. XTAL1 is a CMOS input.

*3. Pins of P0, P1, P2, P3 and P5 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when Vin approximates to 2V.

27.3 A.C. Characteristics



Note: Duty cycle is 50%.

27.3.1 External Clock Characteristics

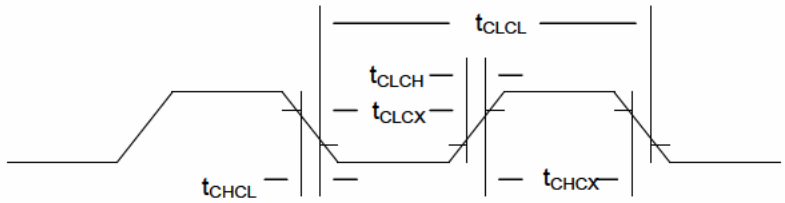
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Clock High Time	t_{CHCX}	22.6	-	-	nS	
Clock Low Time	t_{CLCX}	22.6	-	-	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	

27.3.2 AC Specification

PARAMETER	SYMBOL	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS
Oscillator Frequency	$1/t_{CLCL}$	0	24	MHz

27.3.3 External clock Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock High Time	t_{CHCX}	12.5			ns	
Clock Low Time	t_{CLCX}	12.5			ns	
Clock Rise Time	t_{CLCH}			10	ns	
Clock Fall Time	t_{CLCL}			10	ns	



Note: Duty cycle is 50%

Figure 26-1 External clock characteristics

27.3.4 Serial Port Mode 0 Timing Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Serial Port Clock Cycle Time SM2=0 12 clocks per cycle SM2=1 4 clocks per cycle	t_{XLXL}		 12 t_{CLCL} 4 t_{CLCL}		ns	
Output Data Setup to Clock Rising Edge SM2=0 12 clocks per cycle SM2=1 4 clocks per cycle	t_{QVXH}		 10 t_{CLCL} 3 t_{CLCL}		ns	

Output Data Hold to Clock Rising Edge SM2=0 12 clocks per cycle SM2=1 4 clocks per cycle	t_{XHQX}		 2 t_{CLCL} t_{CLCL}		ns	
Input Data Hold after Clock Rising SM2=0 12 clocks per cycle SM2=1 4 clocks per cycle	t_{XHDX}		 t_{CLCL} t_{CLCL}		ns	
Clock Rising Edge to Input Data Valid SM2=0 12 clocks per cycle SM2=1 4 clocks per cycle	t_{XHDV}		 11 t_{CLCL} 3 t_{CLCL}		ns	

27.3.5 Program Memory Read Cycle

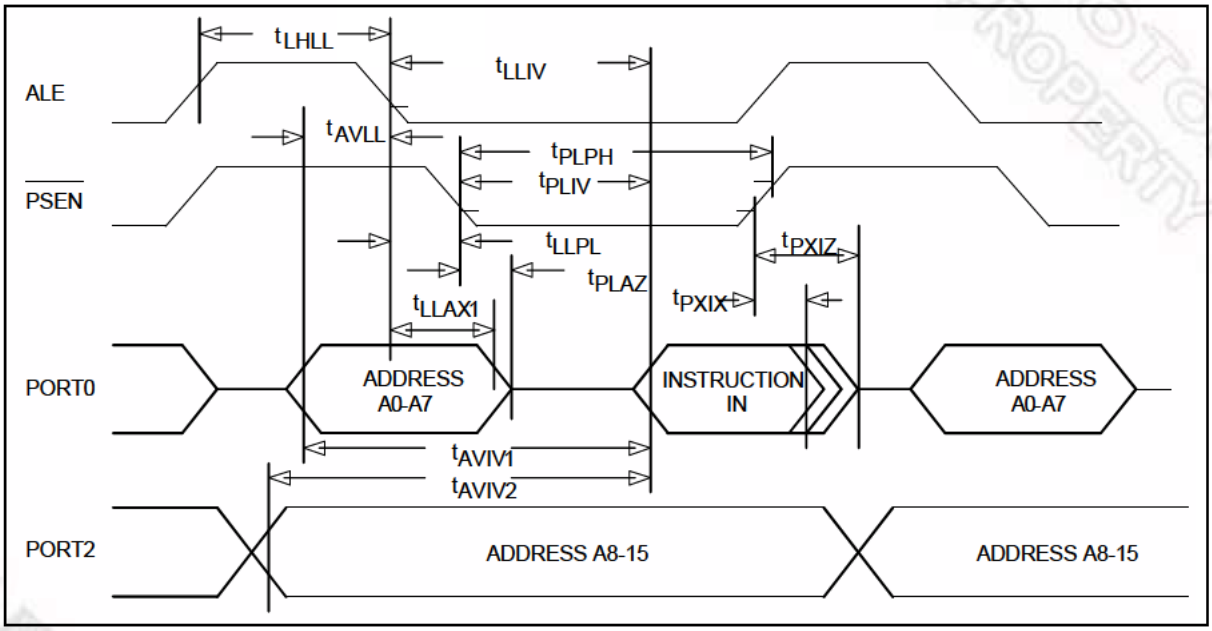


Figure 26-2 Program Memory Read Cycle

27.3.6 Data Memory Read Cycle

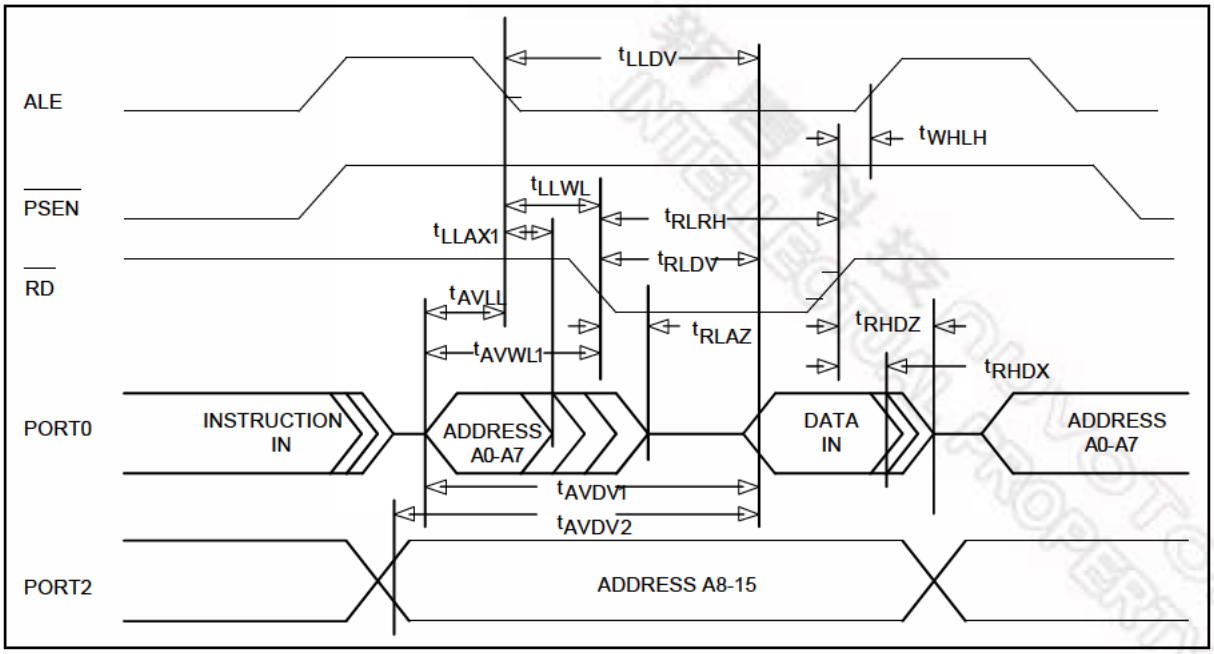


Figure 26-3 Data Memory Read Cycle

27.3.7 Data Memory Write Cycle

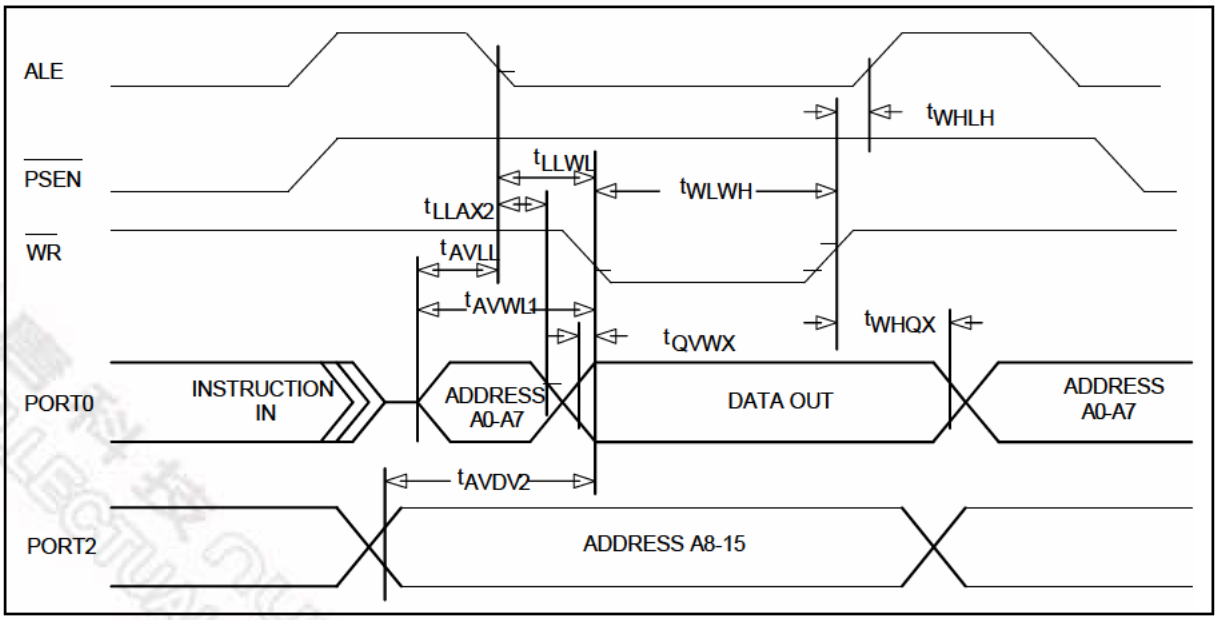


Figure 26-4 Data Memory Write Cycle

27.3.8 I2C Bus Timing Characteristics

PARAMETER	SYMBOL	Standard Mode I2C Bus		UNIT
		Min.	Max.	
SCL clock frequency	f_{SCL}	0	100	kHz
bus free time between a STOP and START condition	t_{BUF}	4.7	-	uS
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{Hd;STA}$	4.0	-	uS
Low period of the SCL clock	t_{LOW}	4.7	-	uS
HIGH period of the SCL clock	t_{HIGH}	4.0	-	uS
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	uS
Data hold time	$t_{HD;DAT}$	5.0	-	uS
Data set-up time	$t_{SU;DAT}$	250	-	nS
Rise time of both SDA and SCL signals	t_r	-	1000	nS
Fall time of both SDA and SCL signals	t_f	-	300	nS
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	uS
Capacitive load for each bus line	C_b	-	400	pF

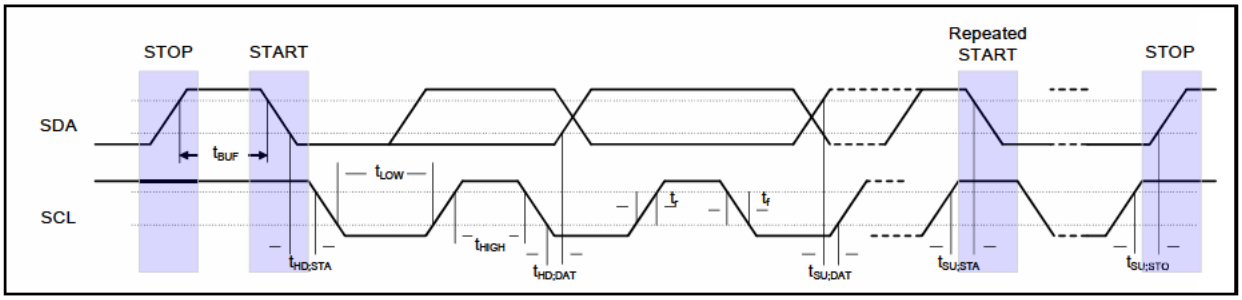


Figure 26-5: I2C Bus Timing

EXPLANATION OF LOGIC SYMBOLS

In order to maintain compatibility with the original 8051 family, this device specifies the same parameter as such device, using the same symbols. The explanation of the symbols is as follows.

t	Time	A	Address
C	Clock	D	Input Data
H	Logic level high	L	Logic level low
I	Instruction	P	$\overline{PSEN}$
Q	Output Data	R	$\overline{RD}$ signal
V	Valid	W	$\overline{WR}$ signal
X	No longer a valid state	Z	Tri-state

27.4 RC OSC AND AC CHARACTERISTICS

(VDD–VSS = 2.4~5V, TA = -40~85°C.)

Parameter	Specification (reference)				Test Conditions
	Min.	Typ.	Max.	Unit	
Frequency accuracy of On-chip RC oscillator (for N79E352)	-25		25	%	V_{DD}=2.4V~5.5V, TA = -40°C ~85°C
Frequency accuracy of On-chip RC oscillator with calibration[1] (for N79E352R)	-2		2	%	V_{DD}=4.5V~5.5V, TA = 25°C
	-5		5	%	V_{DD}=2.7V~5.5V, TA = 0~85°C
	-7		7	%	V_{DD}=2.7V~5.5V, TA = -20~85°C
	-9		9	%	V_{DD}=2.7V~5.5V, TA = -40~85°C
Wakeup time		256		clk	

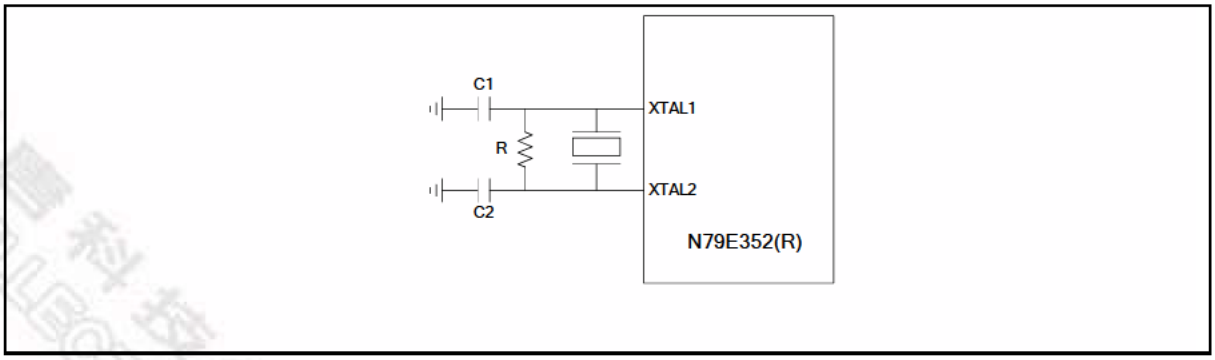
Note:

1. These values are for design guidance only and are not tested.

27.5 Typical Application Circuit

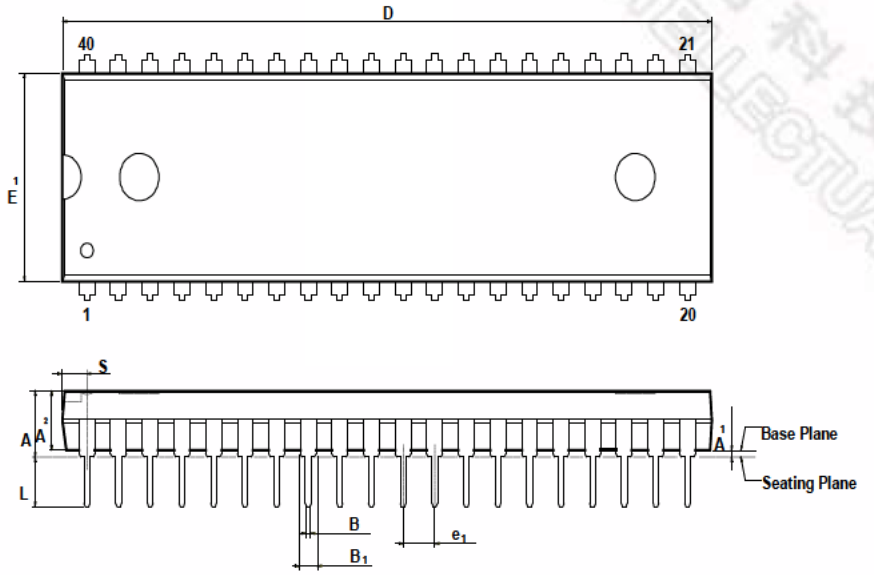
CRYSTAL	C1	C2	R
4MHz ~ 24MHz	without	without	without

The above table shows the reference values for crystal applications.



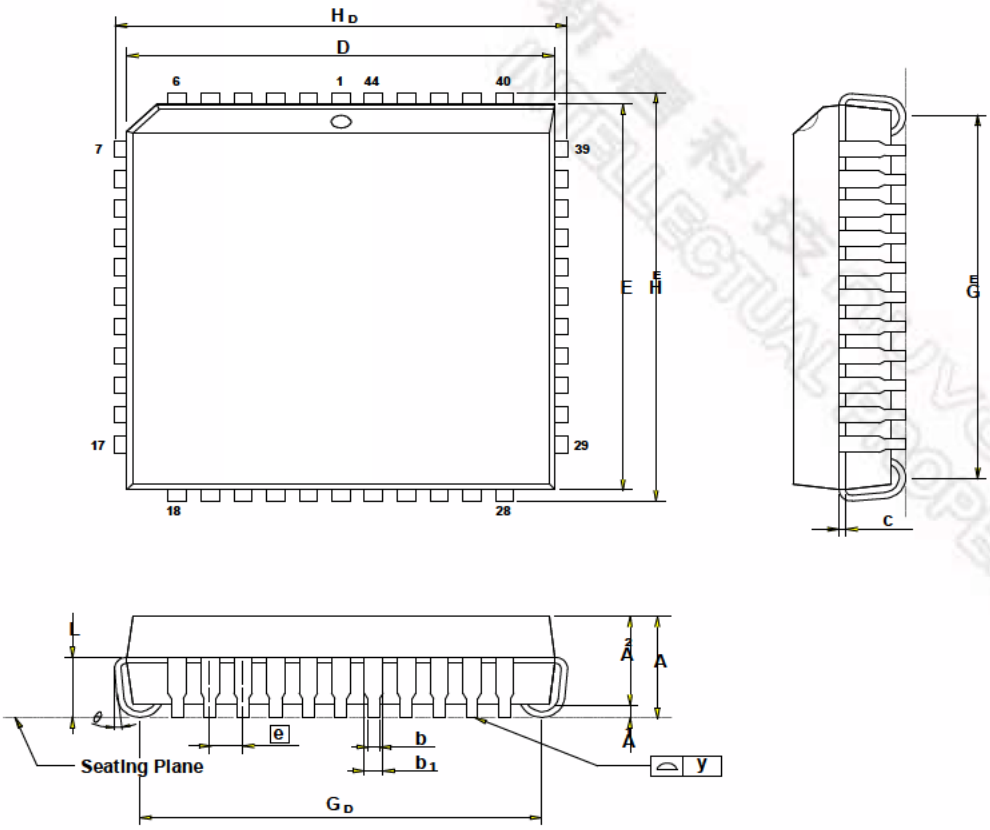
28. PACKAGE DIMENSIONS

28.1 40-pin DIP



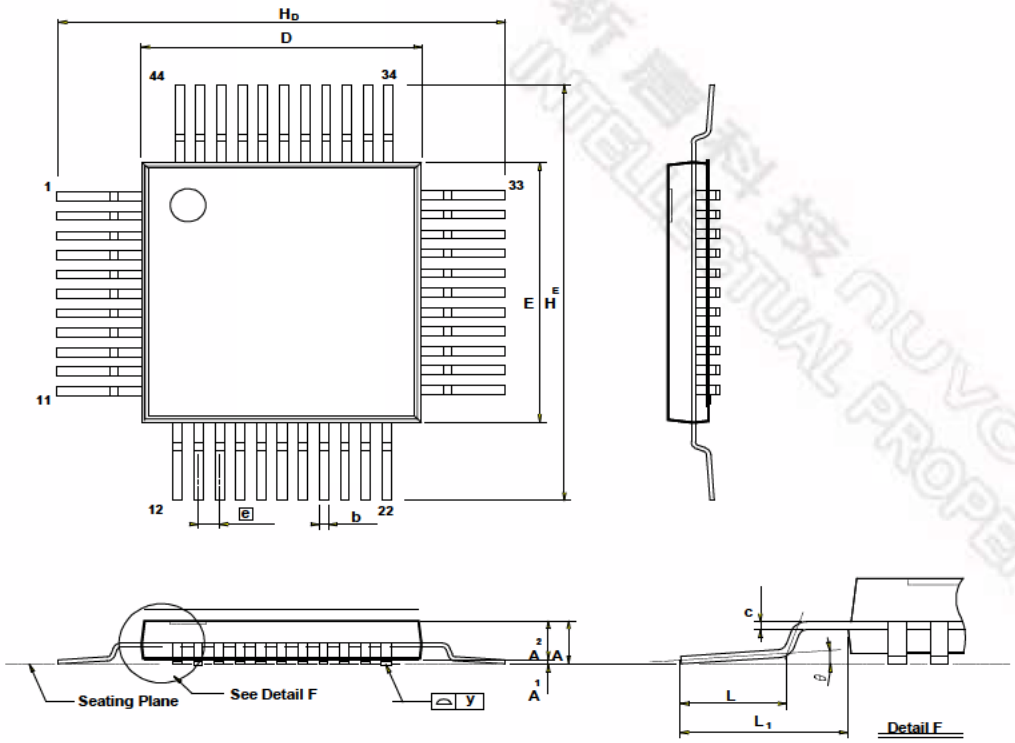
Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
α	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.090	—	—	2.29

28.2 44-pin PLCC



Symbol	Dimension in Inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.185	—	—	4.70
A_1	0.020	—	—	0.51	—	—
A_2	0.145	0.150	0.155	3.68	3.81	3.94
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.36
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.29	2.54	2.79
y	—	—	0.004	—	—	0.10

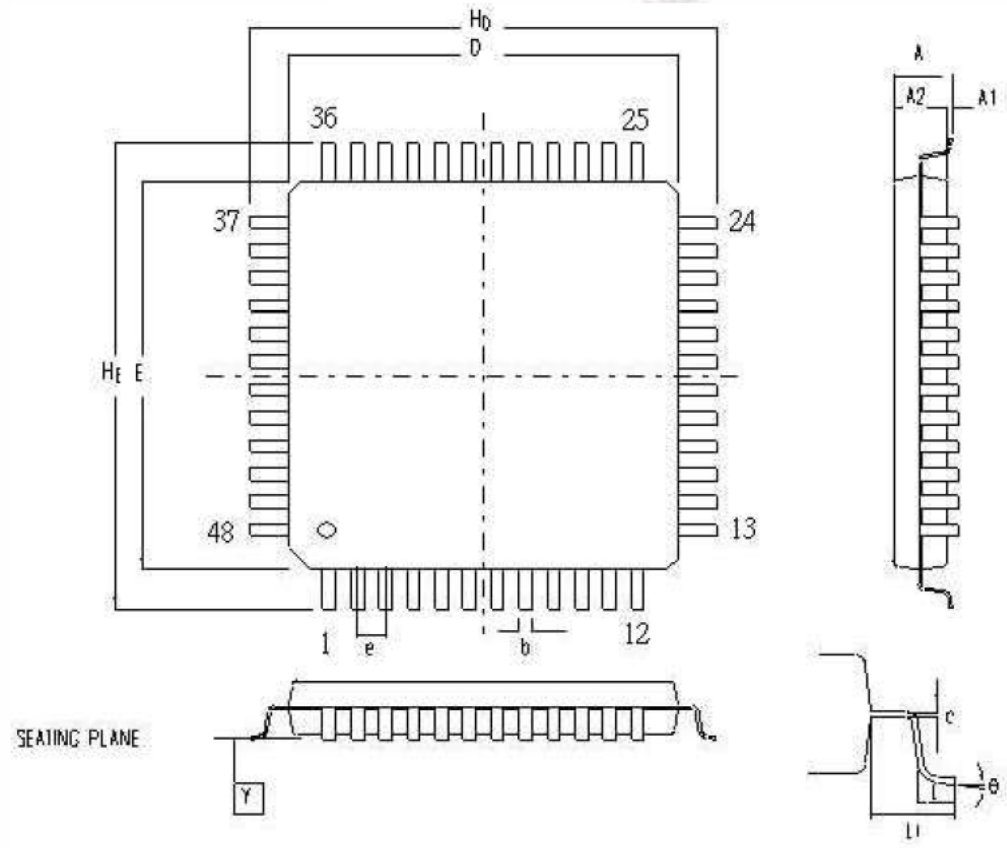
28.3 44-pin PQFP



Symbol	Dimension in Inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	-	—	—	-
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.10	0.15	0.25
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	—	.0315	—	—	0.80	—
H_D	0.510	0.520	0.530	12.95	13.20	13.45
H_E	0.510	0.520	0.530	12.95	13.20	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	—	0.063	—	—	1.60	—
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

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28.4 48-pin LQFP



Controlling dimension : Millimeters

Symbol	Dimension in Inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	0.004	0.006	0.05	0.10	0.15
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
HD	0.350	0.354	0.358	8.90	9.00	9.10
HE	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

29. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A01	Aug, 14, 2008	-	Initial Issued
A02	Aug, 21, 2008	7,8	Update pin configurations.
A03	Feb, 2, 2009	-	Add access external memory diagram
A04	Feb, 9, 2009	-	Modify the part no. with each package 1. 40DIP: N79E352ADG, N79E352RADG 2. 44PLCC: N79E352APG, N79E352RAPG 3. 44PQFP: N79E352AFG, N79E352RAFG 4. 48LQFP: N79E352ALG, N79E352RALG
A05	Apr, 22, 2009	- 108~109 124~125 115	1. Correct typo errors. 2. Release input capture 0 function in Section 20. 3. Re-arrange section sequency after Section 20. 2. Update D.C specification. 3. Renew Figure 0-1: Oscillator
A06	Jul, 29, 2009	119	1. Add ICP description.

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