A1130, A1131, and A1132

Two-Wire Unipolar Vertical Hall-Effect Switches with Advanced Diagnostics

Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: January 31, 2025

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

A1130, A1131, and A1132

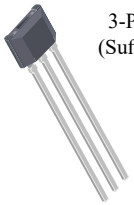
Two-Wire Unipolar Vertical Hall-Effect Switches with Advanced Diagnostics

FEATURES AND BENEFITS

- ISO 26262:2011 compliant
  - Achieves ASIL B as a stand-alone component
  - A²-SIL™ documentation available including FMEDA and Safety Manual
  - Continuously operating background diagnostics
  - Integrated regulator undervoltage monitor
- Magnetic sensing parallel to surface of package
- Internal current regulator for two-wire operation
- Highly sensitive unipolar switch thresholds
- Operation down to 3 V
- Selection of temperature coefficients (TC) to match magnet properties
- Small package sizes, 3-pin SOT23W and SIP
- Automotive-grade ruggedness
  - Qualified per AEC-Q100
  - Internal protection circuits enable 40 V load dump compliance
  - Operation up to 165°C junction temperature
  - Low temperature drift and high physical stress resistance
  - Solid-state reliability
  - Reverse-battery and overvoltage protection

PACKAGES

3-Pin SOT23W
(Suffix LH)



3-Pin SIP
(Suffix UA)

Not to scale

DESCRIPTION

The A1130, A1131, and A1132 are vertical Hall-effect sensor ICs developed in accordance with ISO 26262:2011. The A113x devices feature integrated continuous diagnostic features and a safe output state that supports a functional safety level of ASIL B. The diagnostic features cover critical subsystems of the IC including the signal path, voltage regulator, sensing element, and digital subsystem.

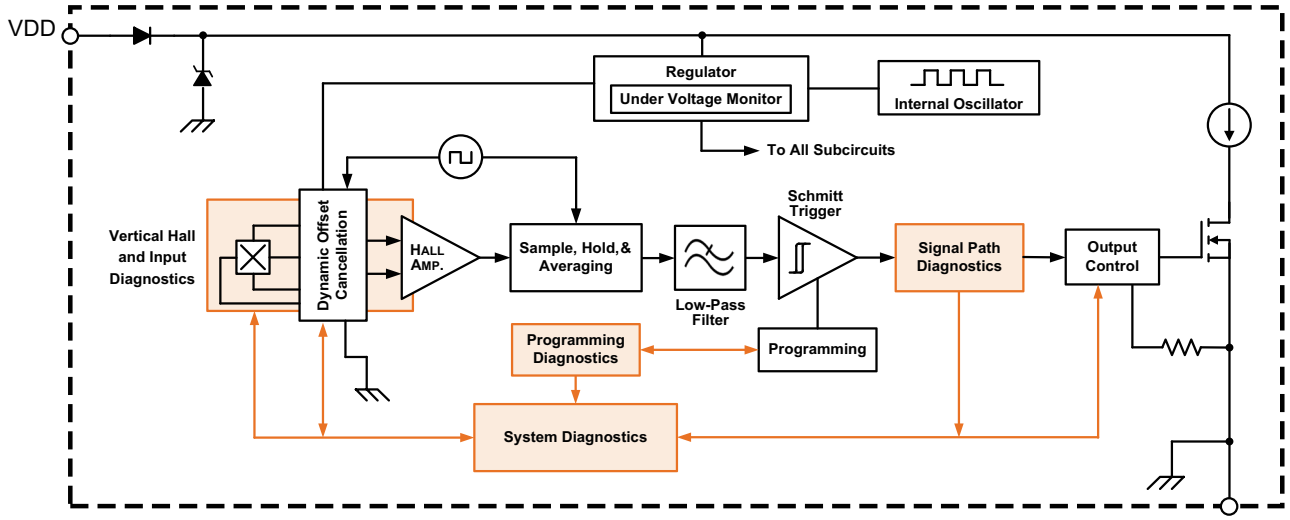
These devices feature an output current interface that is compatible with existing two-wire systems, providing interconnect open and short diagnosis. These devices also feature a safe output state to communicate IC diagnostic information while maintaining compatibility with existing two-wire systems. Should the diagnostics sense an internal failure, the output current will be driven to a level that is below the standard low current level.

This family of unipolar Hall-effect switch ICs feature vertical Hall sensing elements that are sensitive to magnetic fields that are parallel to the surface of the IC package. This can provide additional flexibility in magnetic configuration, as well as the potential to migrate from SIP-based traditional planar Hall-effect sensor ICs to surface-mount vertical Hall-effect sensor

Continued on next page...

APPLICATIONS

- Brake and clutch pedal switches
- Fluid float sensor
- Seat belt buckles and position
- Electronic power steering (EPS) index sensing
- Hood/trunk latches
- Electronic parking brakes



Functional Block Diagram

DESCRIPTION (continued)

ICs while maintaining the same magnetic orientation.

In addition to providing integrated diagnostics and standard two-wire current interface, these sensor ICs are temperature-compensated for use with ferrite and neodymium iron boron magnets and include automotive-grade ruggedness features such as reverse-battery protection, overvoltage protection, and load dump capability of up to 40 V.

This family of devices is available in two package styles and in choices of sensor sensitivity orientations as shown in Figure 2. Package type LH is a modified SOT23W surface-mount package, while package type UA is a three-lead ultramini SIP for through-hole mounting. Both packages are RoHS-compliant and lead (Pb) free (suffix, -T), with 100% matte-tin-plated leadframes.

SPECIFICATIONS

SELECTION GUIDE

Part Number	Packing	Mounting	Sensing Orientation	Output State for B > B_{OP}	Typical Switchpoints (G)		Typical Supply Current (mA)		Operating Ambient Temperature, T_A (°C)
					B_{OP}	B_{RP}	$I_{DD(HIGH)}$	$I_{DD(LOW)}$	
A1130LLHLT-T	7" reel, 3000 pieces	3-pin SOT23W surface mount	X	$I_{DD(HIGH)}$	55	35	14.3	5.9	–40 to 150
A1130LLHLX-T	13" reel, 10000 pieces	3-pin SOT23W surface mount	X						
A1130LUATN-X-T	13" reel, 4000 pieces	3-pin SIP through hole	X						
A1130LUATN-Y-T	13” reel, 4000 pieces	3-pin SIP through hole	Y						
A1131ELHLT-T	7" reel, 3000 pieces	3-pin SOT23W surface mount	X	$I_{DD(LOW)}$	95	70	28.1	10.7	–40 to 85
A1131ELHLX-T	13” reel, 10000 pieces	3-pin SOT23W surface mount	X						
A1132KLHLT-T	7" reel, 3000 pieces	3-pin SOT23W surface mount	X	$I_{DD(LOW)}$	60	35	14.5	3.7	–40 to 125
A1132KLHLX-T	13” reel, 10000 pieces	3-pin SOT23W surface mount	X						

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes		Rating	Unit
Forward Supply Voltage	V_{DD}			26.5	V
Reverse Supply Voltage	V_{RDD}			–18	V
Magnetic Density Flux	B			Unlimited	G
Operating Ambient Temperature	T_A	A1130	Range L	–40 to 150	°C
		A1131	Range E	–40 to 85	°C
		A1132	Range K	–40 to 125	°C
Maximum Junction Temperature	T_J(MAX)			165	°C
Storage Temperature	T_{stg}			–65 to 170	°C

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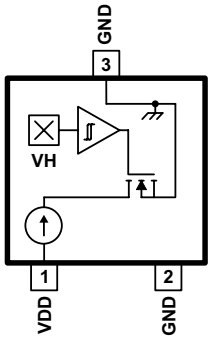
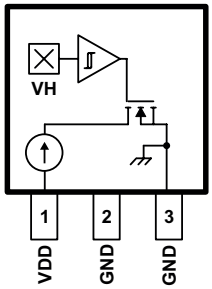
PINOUT DIAGRAMS AND TERMINAL LIST TABLE



Package LH Pinout



Package UA Pinout

Terminal List Table

Symbol	Pin Number		Description
	LH Package	UA Package	
VDD	1	1	Power supply to chip
GND	2	2	Ground
GND	3	3	Ground

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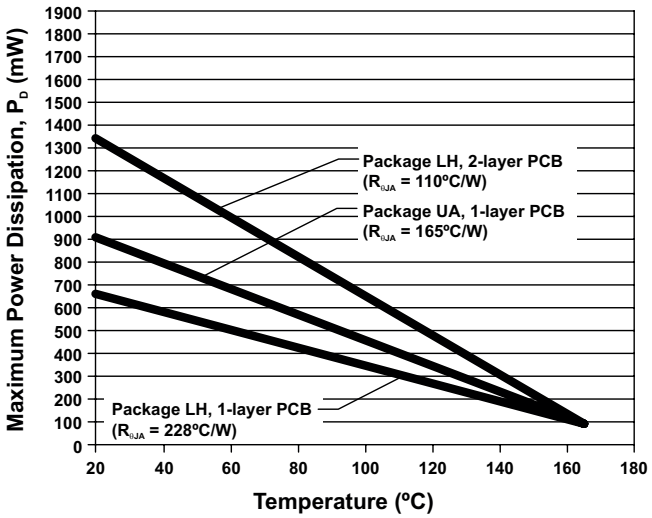
THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Notes	Rating	Unit
Package Thermal Resistance	$R_{\theta JA}$	Package LH, 1-layer PCB with copper limited to solder pads	228	°C/W
		Package LH, 2-layer PCB with 0.463 in.^{2} of copper area, each side connected by thermal vias	110	°C/W
		Package UA, 1-layer PCB with copper limited to solder pads	165	°C/W



Power Dissipation versus Ambient Temperature

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OPERATING CHARACTERISTICS: Valid over full operating voltage and ambient temperature ranges for $T_J < T_J$ (max), unless otherwise specified

Characteristics	Symbol	Test Conditions		Min.	Typ. [1]	Max.	Unit
Supply Voltage [2]	V_{DD}	A1130		3	–	24	V
		A1131		3	–	6	V
		A1132		3	–	12	V
Supply Current	$I_{DD(LOW)}$	A1130	$B < B_{RP}$	5	5.9	6.9	mA
		A1131	$B > B_{OP}$	9.5	10.7	13.6	mA
		A1132	$B > B_{OP}$	2	3.7	4.5	mA
	$I_{DD(HIGH)}$	A1130	$B > B_{OP}$	12	14.3	17	mA
		A1131	$B < B_{RP}$	25.2	28.1	30.9	mA
		A1132	$B < B_{RP}$	13	14.5	16	mA
Reverse Supply Current	I_{RDD}	A1130, A1131, A1132	$V_{RDD} = –18$ V	–	–	–1.6	mA
			$V_{RDD} = –9$ V	–	–	–50	µA
Power-On Time [3]	t_{ON}	$V_{DD} \geq V_{DD}$ (min), $B < B_{RP}$ (min) – 10 G, $B > B_{OP}$ (max) + 10 G		–	50	70	µs
Power-On State [4]	POS	$t < t_{ON}$ (max) ; V_{DD} slew rate > 25 mV/µs		$I_{DD(HIGH)}$			–
Output Slew Rate [5]	di/dt	R_{SENSE} = 100 Ω, C_{BYP} = 0.01 µF, $I_{DD(HIGH)} \rightarrow I_{DD(LOW)}$, $I_{DD(LOW)} \rightarrow I_{DD(HIGH)}$, 10% to 90% points		–	7.25	–	mA/µs
Chopping Frequency	f_C			–	800	–	kHz
Supply Zener Clamp Voltage	V_Z	$I_{DD(LOW)}$ (max) + 3 mA, $T_A = 25°C$		28	–	–	V
Sensitivity Temperature Coefficient [6]	TC_{SENS}	A1130		–	–0.11	–	%/°C
		A1131		–	–0.20	–	%/°C
		A1132		–	–0.19	–	%/°C
Diagnostic Characteristics							
Diagnostics Time Slot	t_{DIAG}			–	50	70	µs
Diagnostics Fault Retry Time [7]	t_{DIAGF}			–	2.2	2.75	ms
Fault Mode Supply Current, Base	$I_{DD(BASE)FAULT}$			–	0.97	–	mA
Fault Mode Supply Current, Peak	$I_{DD(PEAK)FAULT}$			–	2.5	4	mA
Fault Mode Supply Current, Average [8]	$I_{DD(AVG)FAULT}$	See Equations 1 and 2		0.5	1	1.5	mA

[1] Typical data are at $T_A = 25°C$ and V_{DD} = 12 V (A1130), V_{DD} = 5 V (A1131), V_{DD} = 8 V (A1132).
[2] V_{DD} represents the voltage between the VDD pin and the GND pin.
[3] Power-On Time is the duration from when V_{DD} rises above V_{DD}(min) until the output has attained a valid state.
[4] POS is undefined for $V_{DD} < V_{DD}$(min). Use of a V_{DD} slew rate greater than 25 mV/µs is recommended.
[5] Use of a larger bypass capacitor results in slower current change.
[6] Relative to sensitivity at $T_A = 25°C$.
[7] The diagnostics fault retry repeats continuously until a fault condition is no longer observed. See Diagnostics Mode Fault section for details.
[8] Average current measured for one fault mode period; $t_{DIAG} + t_{DIAGF}$.

Equation 1:

$$Fault\ Mode\ Duty\ Cycle\ (DC) = t_{DIAG} / (t_{DIAG} + t_{DIAGF})$$

Equation 2:

$$I_{DD(AVG)FAULT} = [I_{DD(BASE)FAULT} \times (1 - DC)] + [I_{DD(PEAK)FAULT} \times DC]$$

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OPERATING CHARACTERISTICS (continued): Valid over full operating voltage and ambient temperature ranges for $T_J < T_J$ (max), unless otherwise specified

Characteristics	Symbol	Test Conditions		Min.	Typ. [8]	Max.	Unit [9]
Magnetic Characteristics							
Magnetic Sampling Time Slot	t_{SAMPLE}			–	50	70	µs
Operate Point	B_{OP}	A1130	T_A = 25°C	40	55	70	G
			T_A = –40 to 150°C	25	–	80	G
		A1131	T_A = 25°C	75	95	115	G
			T_A = –40 to 85°C	50	–	135	G
		A1132	T_A = –40 to 125°C	30	60	85	G
Release Point	B_{RP}	A1130	T_A = 25°C	20	35	50	G
			T_A = –40 to 150°C	5	–	60	G
		A1131	T_A = 25°C	55	70	85	G
			T_A = –40 to 85°C	30	–	110	G
		A1132	T_A = –40 to 125°C	5	35	65	G
Hysteresis	B_{HYS}	A1130	T_A = 25°C	5	20	35	G
			T_A = –40 to 150°C	5	–	35	G
		A1131	T_A = 25°C	15	25	35	G
			T_A = –40 to 85°C	10	–	42	G
		A1132	T_A = –40 to 125°C	10	25	42	G

[8] Typical data are at T_A = 25°C and V_{DD} = 12 V (A1130), V_{DD} = 5 V (A1131), V_{DD} = 8 V (A1132).
[9] 1 G (gauss) = 0.1 mT (millitesla).

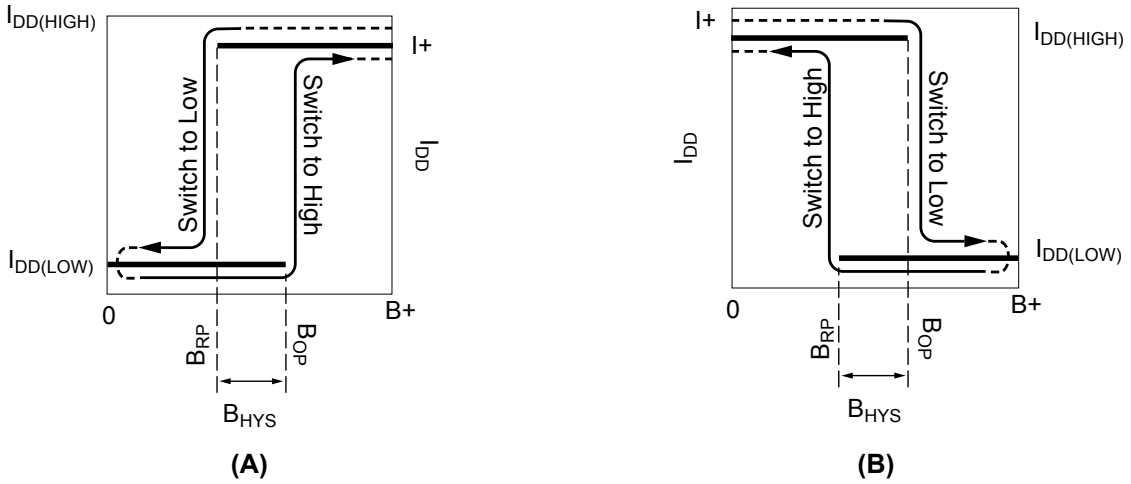

Figure 1: Device switching behavior for A1130 (panel A), A1131 and A1132 (panel B). On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength.

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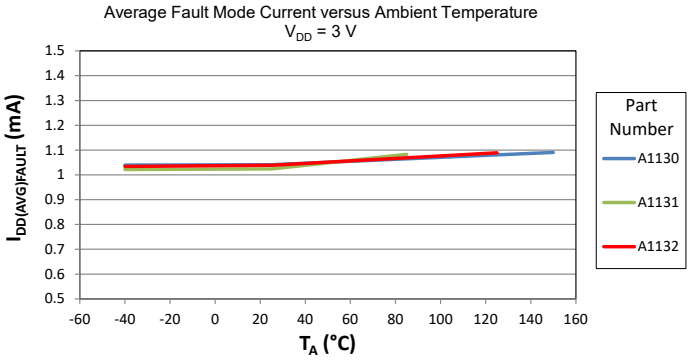
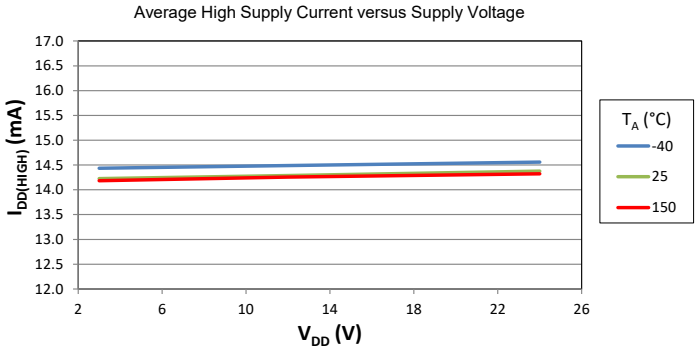
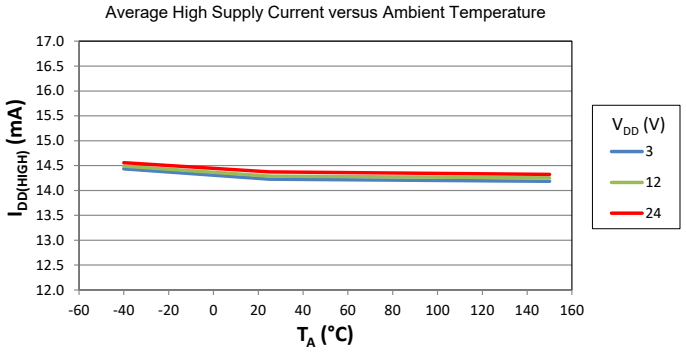
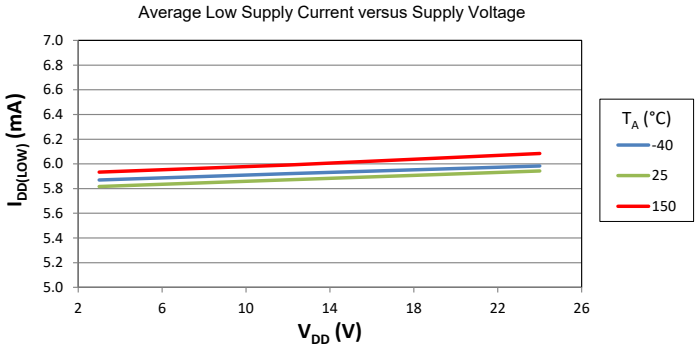
CHARACTERISTIC PERFORMANCE DATA
SAFE STATE

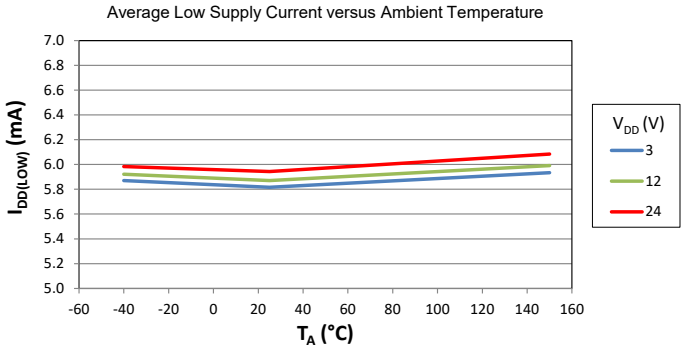


CHARACTERISTIC PERFORMANCE DATA
A1130









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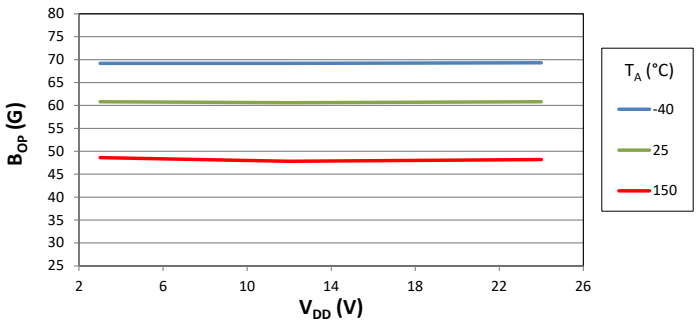
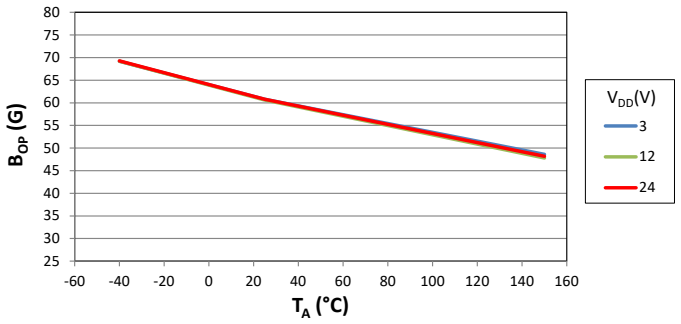
CHARACTERISTIC PERFORMANCE DATA
A1130 (continued)

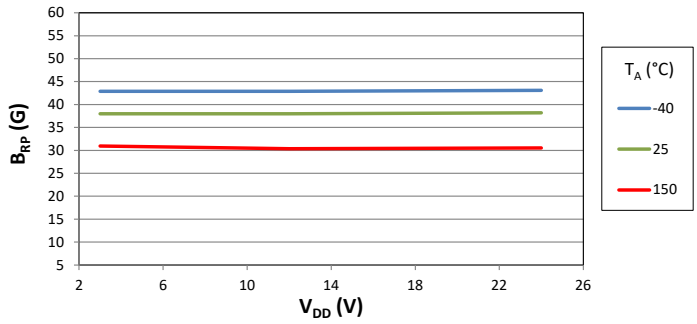
Average Operate Point versus Supply Voltage



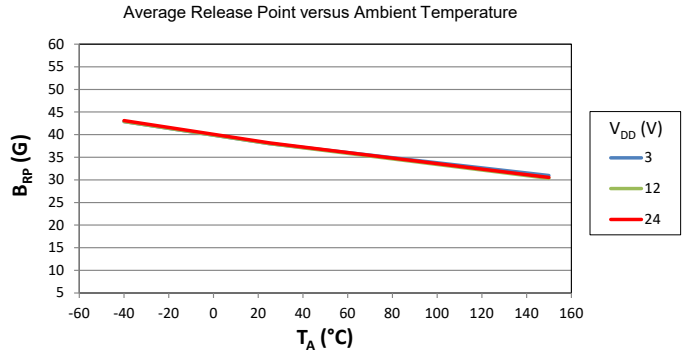
Average Operate Point versus Ambient Temperature



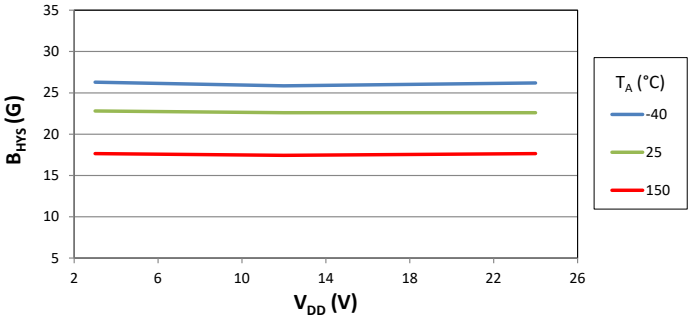
Average Release Point versus Supply Voltage



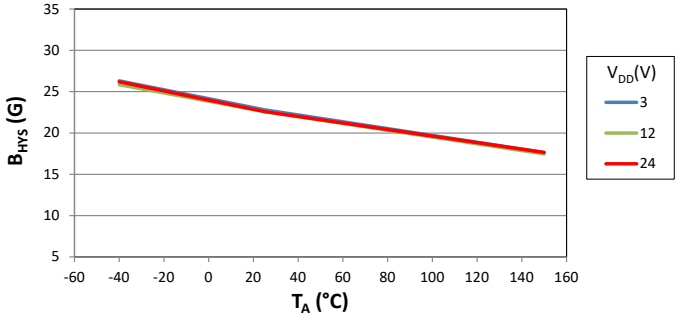
Average Release Point versus Ambient Temperature



Average Switchpoint Hysteresis versus Supply Voltage



Average Switchpoint Hysteresis versus Ambient Temperature



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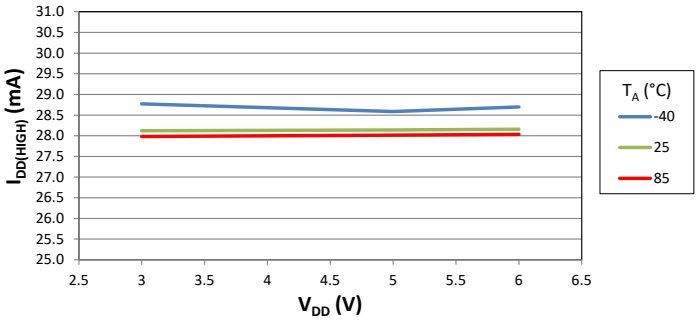
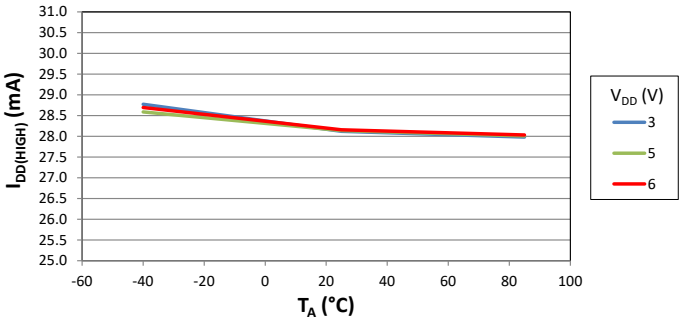
CHARACTERISTIC PERFORMANCE DATA
A1131

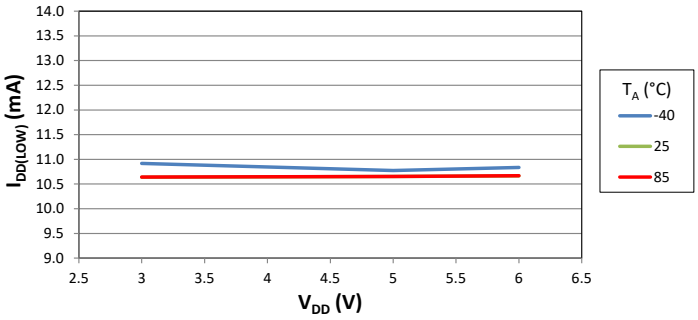
Average High Supply Current versus Supply Voltage



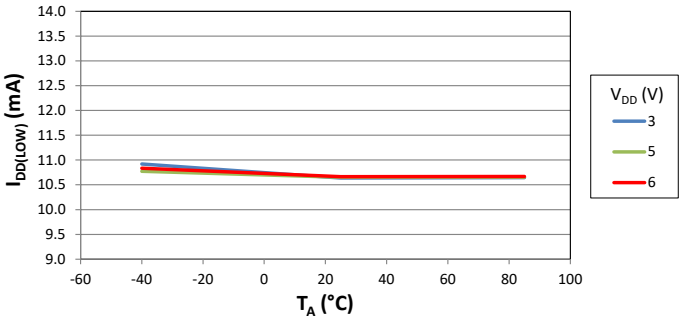
Average High Supply Current versus Ambient Temperature



Average Low Supply Current versus Supply Voltage



Average Low Supply Current versus Ambient Temperature



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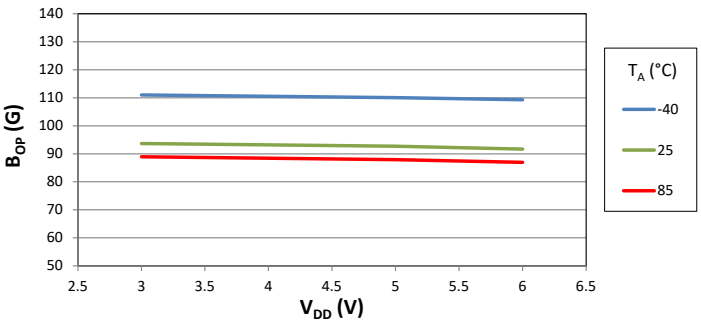
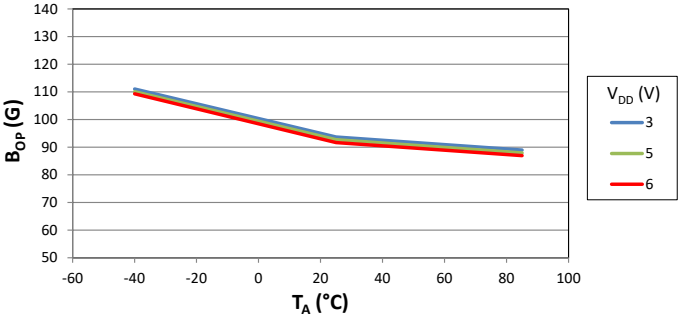
CHARACTERISTIC PERFORMANCE DATA
A1131 (continued)

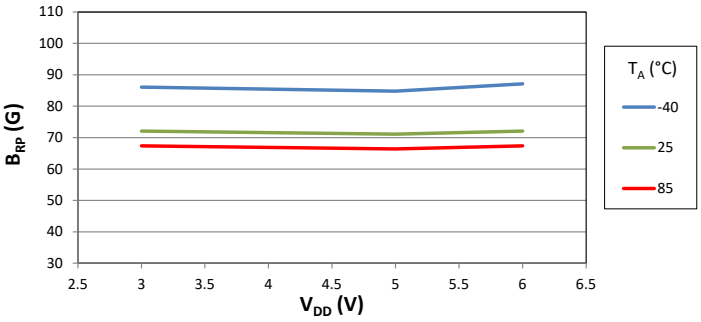
Average Operate Point versus Supply Voltage



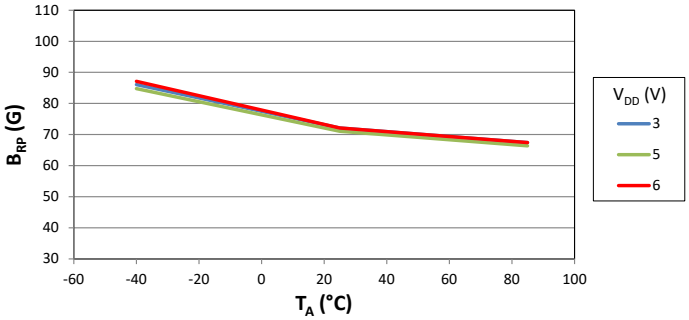
Average Operate Point versus Ambient Temperature



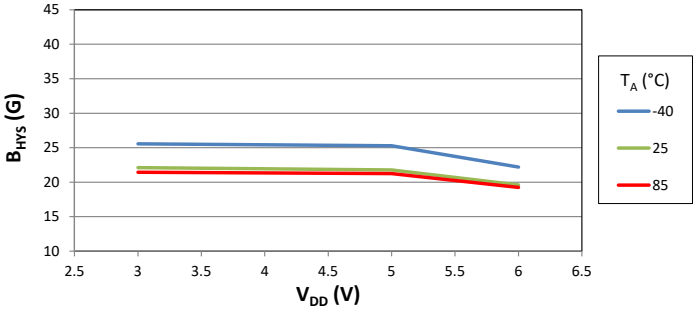
Average Release Point versus Supply Voltage



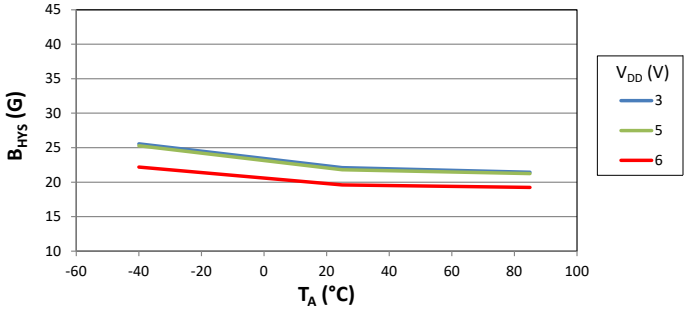
Average Release Point versus Ambient Temperature



Average Switchpoint Hysteresis versus Supply Voltage



Average Switchpoint Hysteresis versus Ambient Temperature



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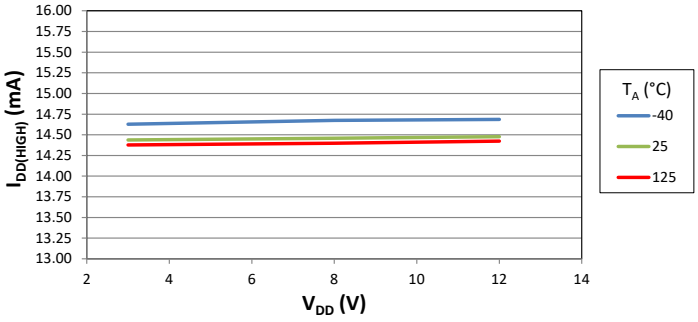
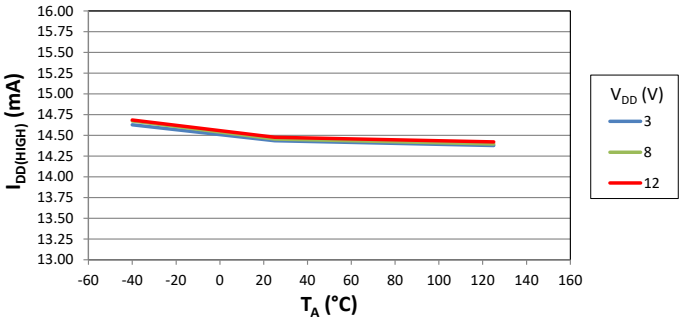
CHARACTERISTIC PERFORMANCE DATA
A1132

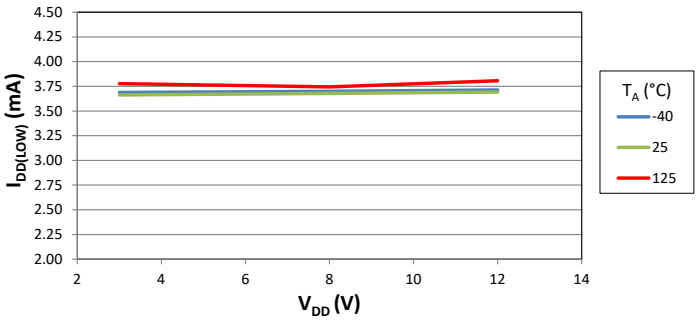
Average High Supply Current versus Supply Voltage



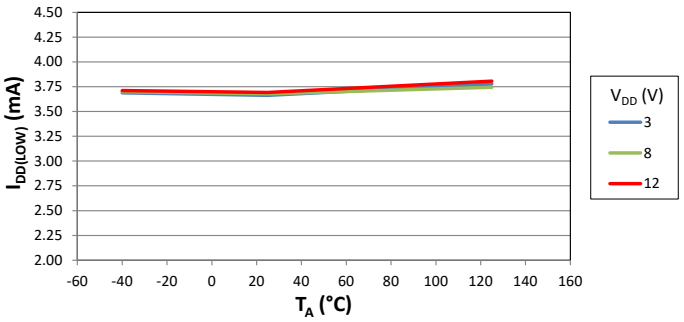
Average High Supply Current versus Ambient Temperature



Average Low Supply Current versus Supply Voltage



Average Low Supply Current versus Ambient Temperature



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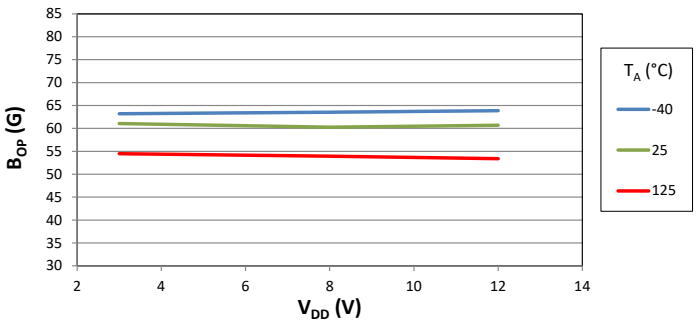
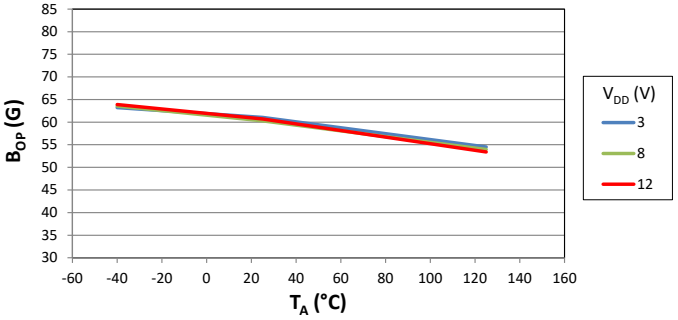
CHARACTERISTIC PERFORMANCE DATA
A1132 (continued)

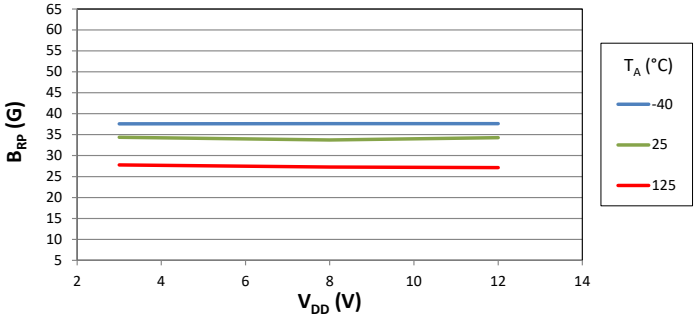
Average Operate Point versus Supply Voltage



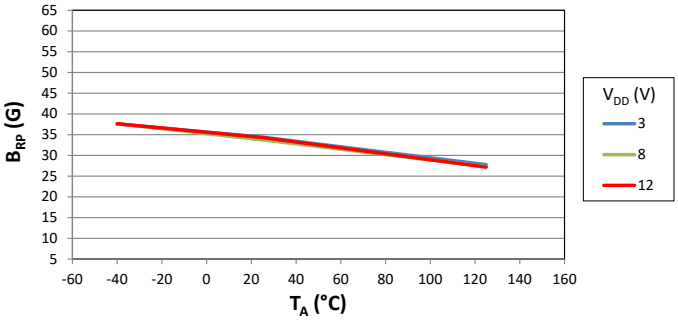
Average Operate Point versus Ambient Temperature



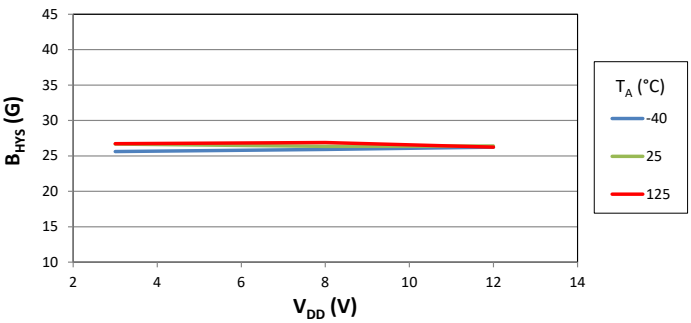
Average Release Point versus Supply Voltage



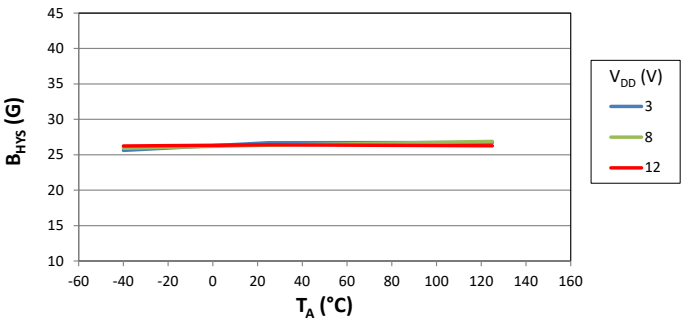
Average Release Point versus Ambient Temperature



Average Switchpoint Hysteresis versus Supply Voltage



Average Switchpoint Hysteresis versus Ambient Temperature



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FUNCTIONAL DESCRIPTION

Functional Safety

The A1130, A1131, and A1132 were designed in accordance with the international standard for automotive functional safety, ISO 26262:2011. This product achieves an ASIL (Automotive Safety Integrity Level) rating of ASIL-B according to the standard. The A1130, A1131, and A1132 are all classified as a SEOoC (Safety Element Out of Context) and can be easily integrated into safety-critical systems requiring higher ASIL ratings that incorporate external diagnostics or use measures such as redundancy. Safety documentation will be provided to support and guide the integration process. For further information, contact your local Allegro field applications engineer or sales representative.

Operation

A1130 – The A1130 output, I_{DD}, switches high ($I_{DD(HIGH)}$) when a south polarity magnetic field perpendicular to the Hall-effect sensor exceeds the operate point threshold, B_{OP} (see panel A of Figure 1). When the magnetic field is reduced below the release point, B_{RP}, the device output switches low ($I_{DD(LOW)}$).

The A1130 is offered in both the LH (3-pin SOT23W) and UA (3-pin SIP) packages. In the LH package, the vertical Hall element is located near the side of the package closest to pin 1 and senses magnetic fields parallel with the X-axis (see panel A in Figure 2). In the UA package, the sensor is located in one of two positions depending on the configuration selection.

The A1130LUA-X has a vertical Hall-effect sensor located on the right side of the UA package and detects magnetic fields parallel with the X-axis (see panel C in Figure 2). The alternative configuration in the UA package is the A1130LUA-Y, which has a sensitive element located near the top of the package and senses fields parallel with the Y-axis (see panel B in Figure 2).

A1131 and A1132 – The output of the A1131 and A1132 devices switches low ($I_{DD(LOW)}$) when a south polarity magnetic field perpendicular to the Hall element exceeds the operate point threshold, B_{OP} (see panel B of Figure 1). When the magnetic field is reduced below the release point, B_{RP}, the device output switches high ($I_{DD(HIGH)}$).

The A1131 and A1132 are offered exclusively in the LH package. The vertical Hall element is located near the side of the package closest to pin 1 and senses magnetic fields parallel with the X-axis (see panel A in Figure 2).

A1130, A1131, and A1132 – The difference in the magnetic operate and release points is the hysteresis (B_{HYS}) of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

Powering-on the device in the hysteresis range (less than B_{OP} and higher than B_{RP}) will result in an $I_{DD(HIGH)}$ output state. The correct state is attained after the first excursion beyond B_{OP} or B_{RP}. Refer to Figure 3 for an example of the power-on behavior.

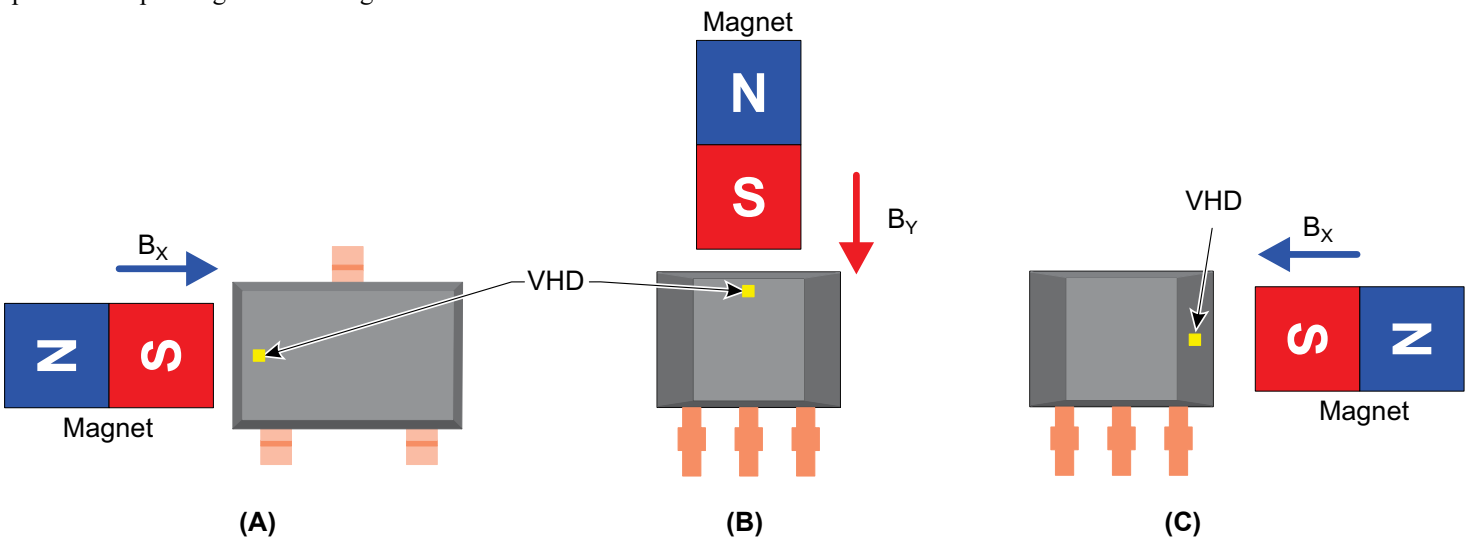

Figure 2: Vertical Hall Device (VHD) Sensing Direction for A1130LLH, A1131ELH, and A1132KLH (panel A), A1130LUA-Y (panel B), and A1130LUA-X (panel C).

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Power-On Sequence and Timing

The state of the output is only valid when the supply voltage is within the specified operating range (V_{DD} (min) ≤ V_{DD} ≤ V_{DD} (max)) and the power-on time has elapsed ($t > t_{ON}$). Refer to Figure 3: Power-On Example for an illustration of the power-on sequence.

During the power-on time, $t < t_{ON}$, the device output state is latched in the $I_{DD(HIGH)}$ state. After the first magnetic signal time slot sample has been processed (t_1 in Figure 3), the output will correspond with the externally applied magnetic field.

During the first diagnostics time slot, the output is latched according to the magnetic field input from the power-on signal sampling time slot. A normally operating device will continue this sampling and diagnostics routine. A device that has a fault will revert control of the output to the system diagnostics controller and enter the safe state, $I_{DD(AVG)FAULT}$.

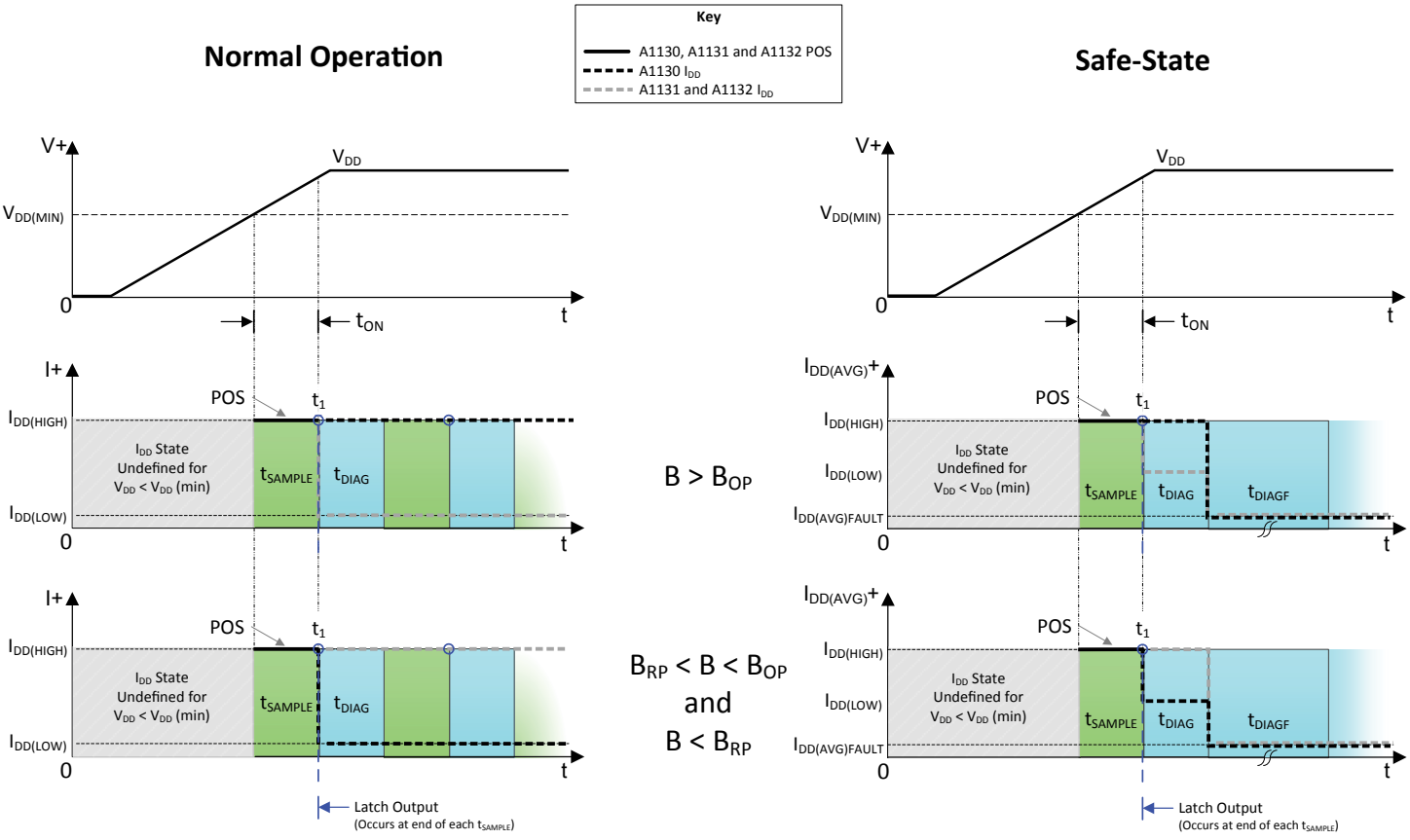

Figure 3: Power-On Example – Normally Operating Device (Left) and Safe-State Device (Right)

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Two-Wire Interface

The regulated current output is configured for two-wire applications, requiring one less wire for operation than switches with the traditional open-collector output. Additionally, the system designer inherently gains basic diagnostics because there is always output current flowing, which should be in either of two narrow ranges under normal operation, shown in Figure 4 as $I_{DD(HIGH)}$ and $I_{DD(LOW)}$. Any current level not within these ranges indicates a fault condition.

If $I_{DD} > I_{DD(HIGH)}$ (max), then a short condition exists, and if $I_{DD} < I_{DD(LOW)}$ (min), then an open condition exists (except in the case of an error found during internal diagnostics, in which case the average supply current is $I_{DD(AVG)FAULT}$). Any value of I_{DD} between the allowed ranges for $I_{DD(HIGH)}$ and $I_{DD(LOW)}$ indicates a general fault condition.

This unique two-wire interface protocol is backward compatible with legacy systems using two-wire switches. Additionally, the low fault mode supply current resulting from an internal fault will fall outside of the low and high supply current ranges, and can be similarly identified as a sensor fault.

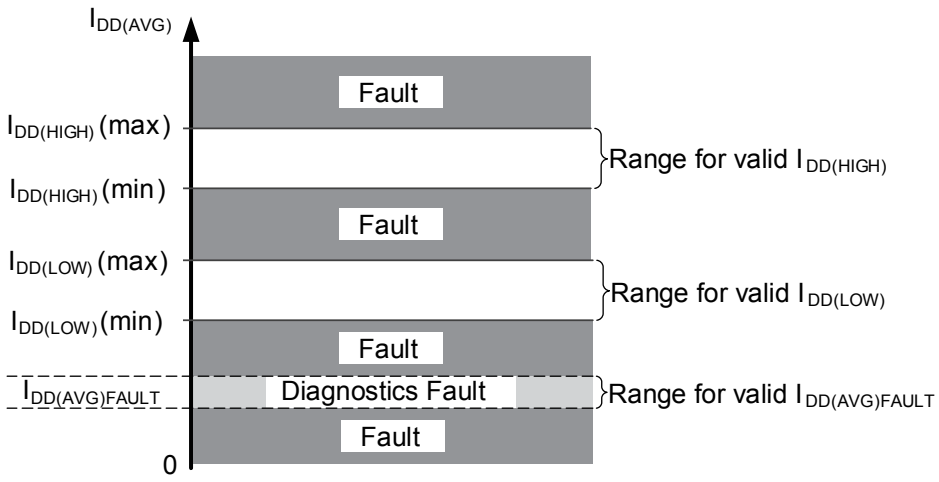

Figure 4: Diagnostic Characteristics of Supply Current Values

Output Polarity

The output signal may be read as a voltage, V_{SENSE}, by using a sense resistor, R_{SENSE}, placed either in series with VDD or with GND (refer to Figure 5). When R_{SENSE} is placed in series with GND, the output signal voltage is in phase with I_{DD}. When R_{SENSE} is placed in series with VDD, the output signal voltage is inverted relative to I_{DD}. Note also that the output of the A1130 is inverted relative to the outputs of the A1131 and A1132 (refer to the Selection Guide).

Table 1: Output Signal Polarity

R_{SENSE} Location (Refer to Figure 5)	I_{DD} State	V_{SENSE} Logic State
High Side (VDD Pin Side)	High	Low
	Low	High
Low Side (GND Pin Side)	High	High
	Low	Low

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TYPICAL APPLICATIONS

It is strongly recommended that an external bypass capacitor, C_{BYP}, be connected (in close proximity to the Hall sensor) between the supply and ground of the device to guarantee correct performance under harsh environmental conditions and to reduce noise from internal circuitry. As is shown in Figure 5, a 0.01 µF capacitor is typical. Use of a larger bypass capacitor may result in a slower output slew rate, and should be evaluated according to the requirements set forth by the application. Additionally, an optional output load capacitor may be added in parallel with the sense resistor for increased signal filtering and EMC immunity.

The A1130, A1131, and A1132 are designed for functional safety and comply with ISO 26262:2011 ASIL B. When used in conjunction with appropriate system-level control, the internal diagnostic features can assist in meeting the most stringent ASIL safety requirements. For further information, contact your local Allegro field applications engineer or sales representative.

Extensive applications information on magnets and Hall-effect sensors is available in:

- *Hall-Effect IC Applications Guide, AN27701,*
- *Hall-Effect Devices: Guidelines For Designing Subassemblies Using Hall-Effect Devices AN27703.1*
- *Soldering Methods for Allegro's Products – SMT and Through-Hole, AN26009*

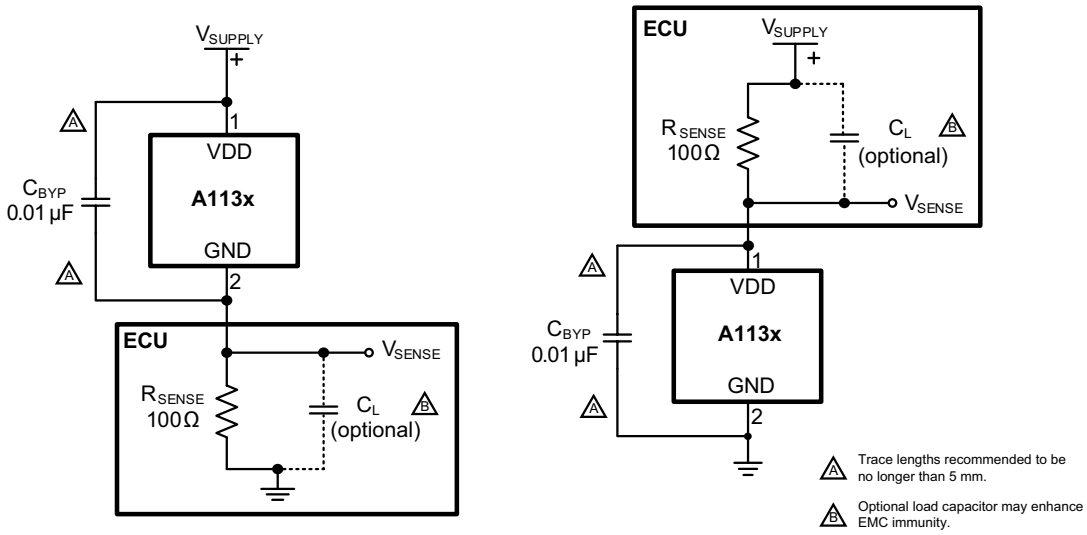
All are provided on the Allegro website:

www.allegromicro.com

Temperature Coefficient and Magnet Selection

The A1130, A1131, and A1132 are designed with a sensitivity temperature coefficient to compensate for drifts of NdFeB and ferrite magnets over temperature—as indicated in the specifications table on page 5. This compensation improves the magnetic system performance over the entire temperature range.

For example, the magnetic field strength from NdFeB decreases as the temperature increases from 25°C to 150°C. This lower magnetic field strength means that a lower switching threshold is required to maintain switching at the same distance from the magnet to the sensor. Correspondingly, higher switching thresholds are required at cold temperatures, as low as –40°C, due to the higher magnetic field strength from the NdFeB magnet. The A1130, A1131, and A1132 compensate the switching thresholds over temperature as described above. It is recommended that system designers evaluate their magnetic circuit over the expected operating temperature range to ensure the magnetic switching requirements are met.



(A) Low-Side Sensing **(B) High-Side Sensing**

Figure 5: Typical Application Circuits

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Diagnostics

The A1130, A1131, and A1132 were developed in accordance with ISO 26262:2011 and feature a proprietary diagnostics routine that enables the achievement of ASIL B safety requirements. This internal diagnostics routine continuously runs between magnetic signal sampling time slots during normal operation. Maximum time slot duration is 70 µs for each of the magnetic signal sampling and the diagnostics mode.

During the diagnostics time slot, external magnetic signals are not sampled and the device output will retain the state from the prior magnetic signal sampling time slot (unless a diagnostics fault causes the device to enter a safe state). The system provides continuous fault detection for the internal power supply regulator and entire signal chain, regardless of the external magnetic field.

The successive operation of the magnetic signal sampling and diagnostics modes results in a Hall signal refresh every 140 µs. This time slotting technique allows for the proper settling of the signal during magnetic and diagnostics routines. A channel reset occurs between slots to force transitions and prevent inter-slot coupling.

During the diagnostics mode time slot, a signal is injected at the vertical Hall element and checked at the exit of the Schmitt trigger. During this time, the critical signal path subsystems are monitored for proper operation. The Hall element biasing circuit and voltage regulator are additionally checked for valid operation. and the programming block is checked for correct parity. The injected signal forces two internal state transitions ($B > B_{OP}$ and $B < B_{RP}$) under normal operation. In cases when these output transitions do not occur, or if another internal fault is detected, the average device supply current will be reduced to $I_{DD(AVG)FAULT}$ (See Diagnostics Mode Fault Operation section).

When a higher system ASIL rating is required, additional external safety measures may be employed (e.g. sensor redundancy and rationality checks, etc.). Refer to the device safety manual for additional details about the diagnostics.

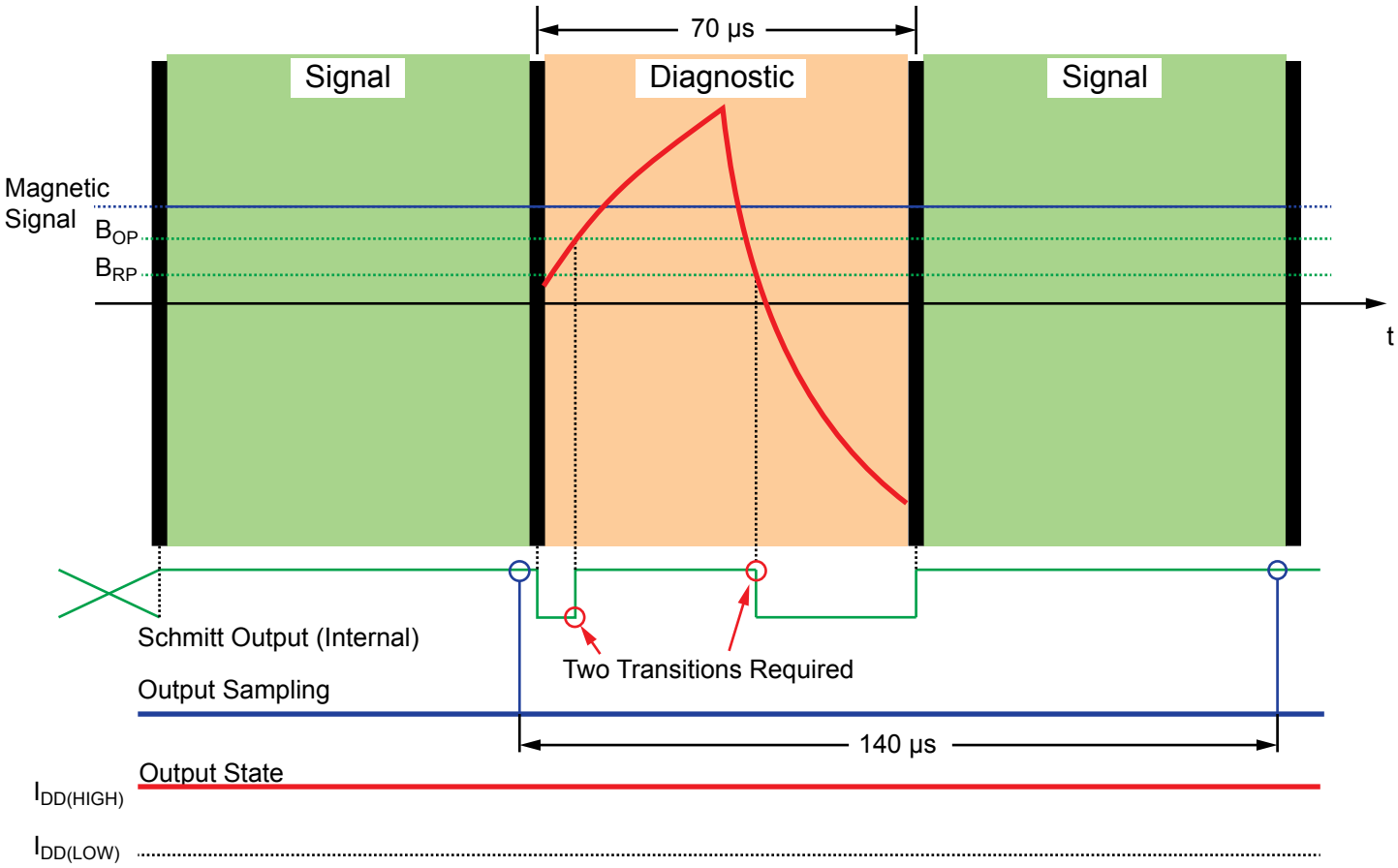

Figure 6: Time Slot Multiplexing Diagram (A1130 Polarity Shown)

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Diagnostics Mode Fault Operation

In the event of a fault, the device will continuously run the diagnostics routine every 2.75 ms (t_{DIAGF}). The periodic recovery attempt sequence allows the device to continuously check for fault integrity while maintaining an optimized low supply current. The recovery period, composed of t_{DIAG} + t_{DIAGF}, is low duty cycle. In this mode, the current varies from $I_{DD(PEAK)FAULT}$ while performing the diagnostics test to $I_{DD(BASE)FAULT}$ standby current.

In the case where the fault is no longer present, normal time-slotting operation will resume, beginning with an internal reset and a transition to the power-on state. However, if the fault is persistent, the device will remain in fault mode and the supply current will continue to have an average of $I_{DD(AVG)FAULT}$. See Equations 1 and 2 (page 5) for determining the fault mode average current.

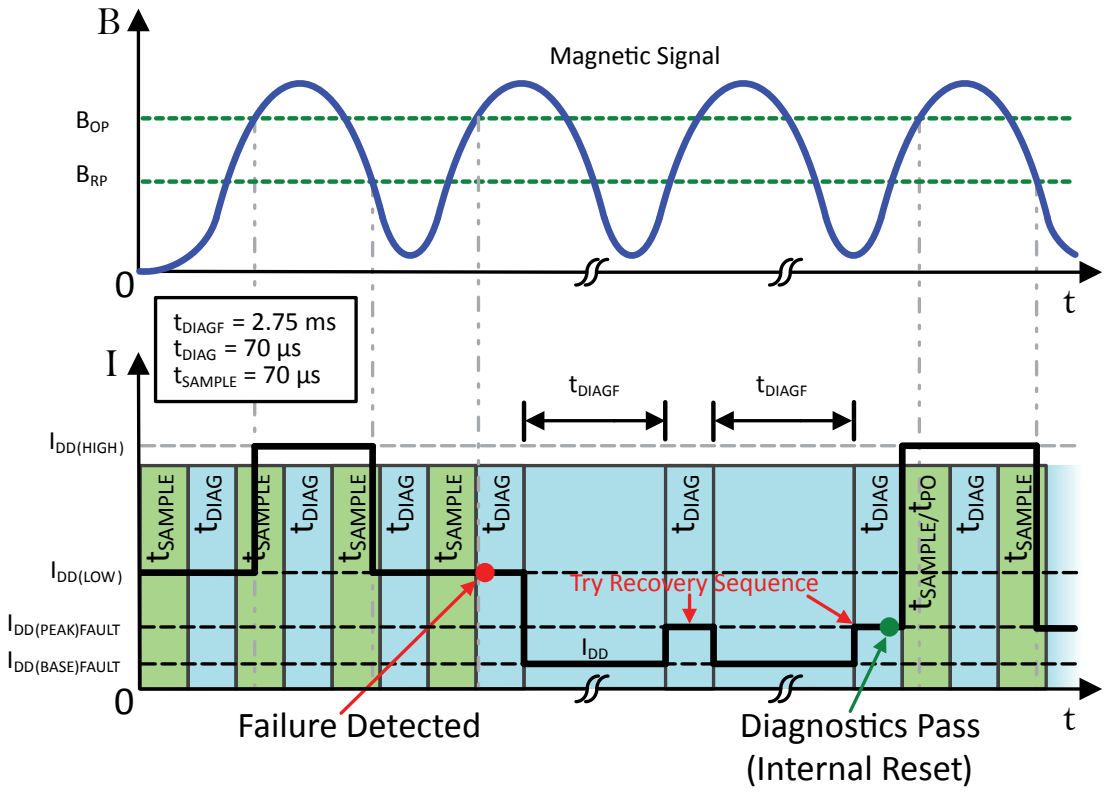

Figure 7: Diagnostics Recovery Sequence (A1130 Polarity Shown)

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CHOPPER STABILIZATION

A limiting factor for switchpoint accuracy when using Hall-effect technology is the small-signal voltage developed across the Hall plate. This voltage is proportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal and maintain an accurate, reliable output over the specified temperature and voltage range. Chopper stabilization is a proven approach used to minimize Hall offset.

The technique, dynamic quadrature offset cancellation, removes key sources of the output drift induced by temperature and package stress. This offset reduction technique is based on a signal modulation-demodulation process. Figure 8: Model of Chopper Stabilization Circuit (Dynamic Offset Cancellation) illustrates how it is implemented.

The undesired offset signal is separated from the magnetically induced signal in the frequency domain through modulation.

The subsequent demodulation acts as a modulation process for the offset, causing the magnetically induced signal to recover its original spectrum at baseband while the DC offset becomes a high-frequency signal. Then, using a low-pass filter, the signal passes while the modulated DC offset is suppressed.

Allegro's innovative chopper stabilization technique uses a high-frequency clock. The high-frequency operation allows a greater sampling rate that produces higher accuracy, reduced jitter, and faster signal processing. Additionally, filtering is more effective and results in a lower noise analog signal at the sensor output. Devices such as the A1130, A1131, and A1132 that use this approach have a stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process which allows the use of low-offset and low-noise amplifiers in combination with high-density logic and sample-and-hold circuits.

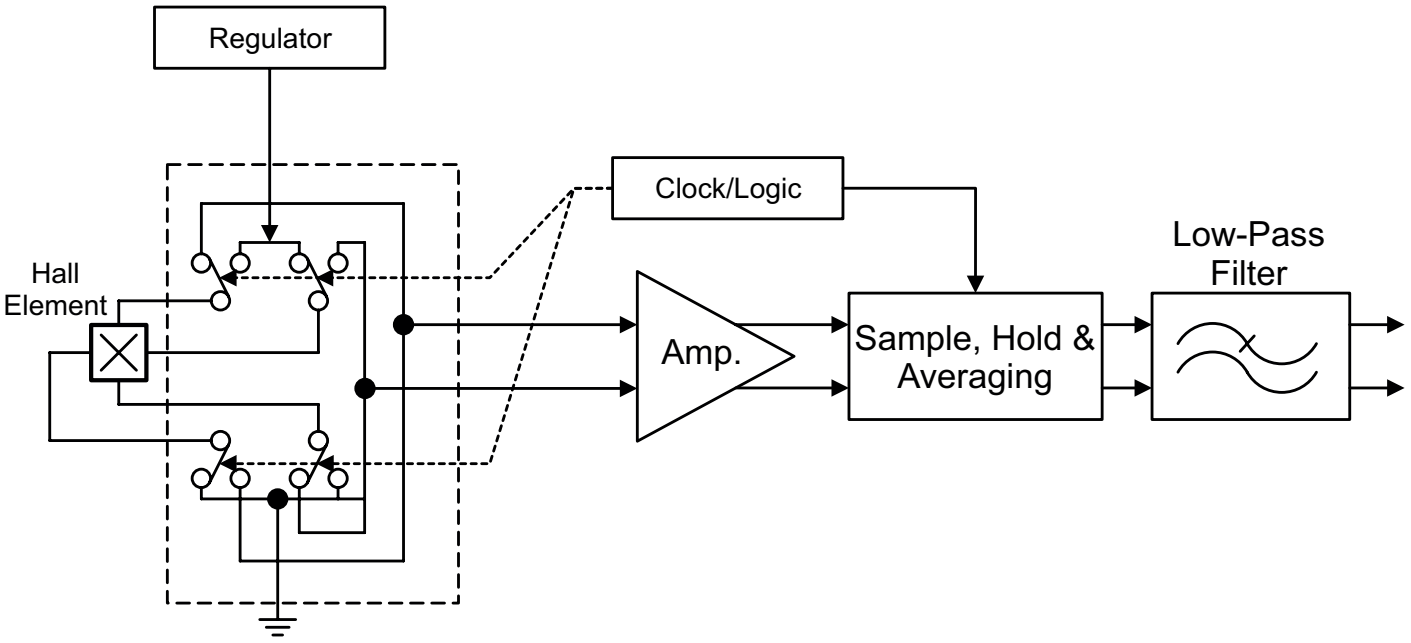

Figure 8: Model of Chopper Stabilization Circuit (Dynamic Offset Cancellation)

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POWER DERATING

The device must be operated below the maximum junction temperature of the device, T_J (max). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data for each package is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Thermal radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A = 25°C, V_{DD} = 8 V, I_{DD} = 3.7 mA, and $R_{\theta JA}$ = 110°C/W for the LH package, then:

$$P_D = V_{DD} \times I_{DD} = 8\ V \times 3.7\ mA = 29.6\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 29.6\ mW \times 110°C/W = 3.3°C$$

$$T_J = T_A + \Delta_T = 25°C + 3.3°C = 28.3°C$$

A worst-case estimate, P_D (max), represents the maximum allowable power level (V_{DD} (max), I_{DD} (max)), without exceeding T_J (max), at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{DD} at T_A = 150°C, package UA, using low-K PCB. Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$ = 165°C/W, T_J (max) = 165°C, V_{DD} (max) = 24 V, and I_{DD} (max) = 17 mA.

Calculate the maximum allowable power level, P_D (max). First, invert equation 3:

$$\Delta T_{max} = T_J(max) - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation.

Then, invert equation 2:

$$P_D(max) = \Delta T_{max} \div R_{\theta JA} = 15°C \div 165°C/W = 91\ mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{DD}(est) = P_D(max) \div I_{DD}(max) = 91\ mW \div 17\ mA = 5.4\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages ≤ V_{DD} (est).

Compare V_{DD} (est) to V_{DD} (max). If V_{DD} (est) ≤ V_{DD} (max), then reliable operation between V_{DD} (est) and V_{DD} (max) requires enhanced $R_{\theta JA}$. If V_{DD} (est) ≥ V_{DD} (max), then operation between V_{DD} (est) and V_{DD} (max) is reliable under these conditions.

In cases where the V_{DD} (max) level is known, and the system designer would like to determine the maximum allowable ambient temperature (T_A (max)), the calculations can be reversed.

For example, in a worst-case scenario with conditions V_{DD} (max) = 24 V, I_{DD} (max) = 17 mA, and $R_{\theta JA}$ = 228°C/W for the LH package using equation 1, the largest possible amount of dissipated power is:

$$P_D = V_{IN} \times I_{IN}$$

$$P_D = 24\ V \times 17\ mA = 408\ mW$$

Then, by rearranging equation 3:

$$T_A(max) = T_J(max) - \Delta T$$

$$T_A(max) = 165°C - (408\ mW \times 228°C/W)$$

$$T_A(max) = 165°C - 93°C = 72°C$$

In another A1130 example, the maximum supply voltage is equal to V_{DD} (min). Therefore, V_{DD} (max) = 3 V and I_{DD} (max) = 17 mA. By using equation 1, the largest possible amount of dissipated power is:

$$P_D = V_{IN} \times I_{IN}$$

$$P_D = 3\ V \times 17\ mA = 51\ mW$$

Then, by rearranging equation 3:

$$T_A(max) = T_J(max) - \Delta T$$

$$T_A(max) = 165°C - (51\ mW \times 228°C/W)$$

$$T_A(max) = 165°C - 11.6°C = 153.4°C$$

The example above indicates that at V_{DD} = 3 V and I_{DD} = 17 mA, the T_A (max) can be as high as 153.4°C without exceeding T_J (max). However the T_A (max) rating of the device is 150°C; the A1130 performance is not guaranteed above T_A = 150°C.

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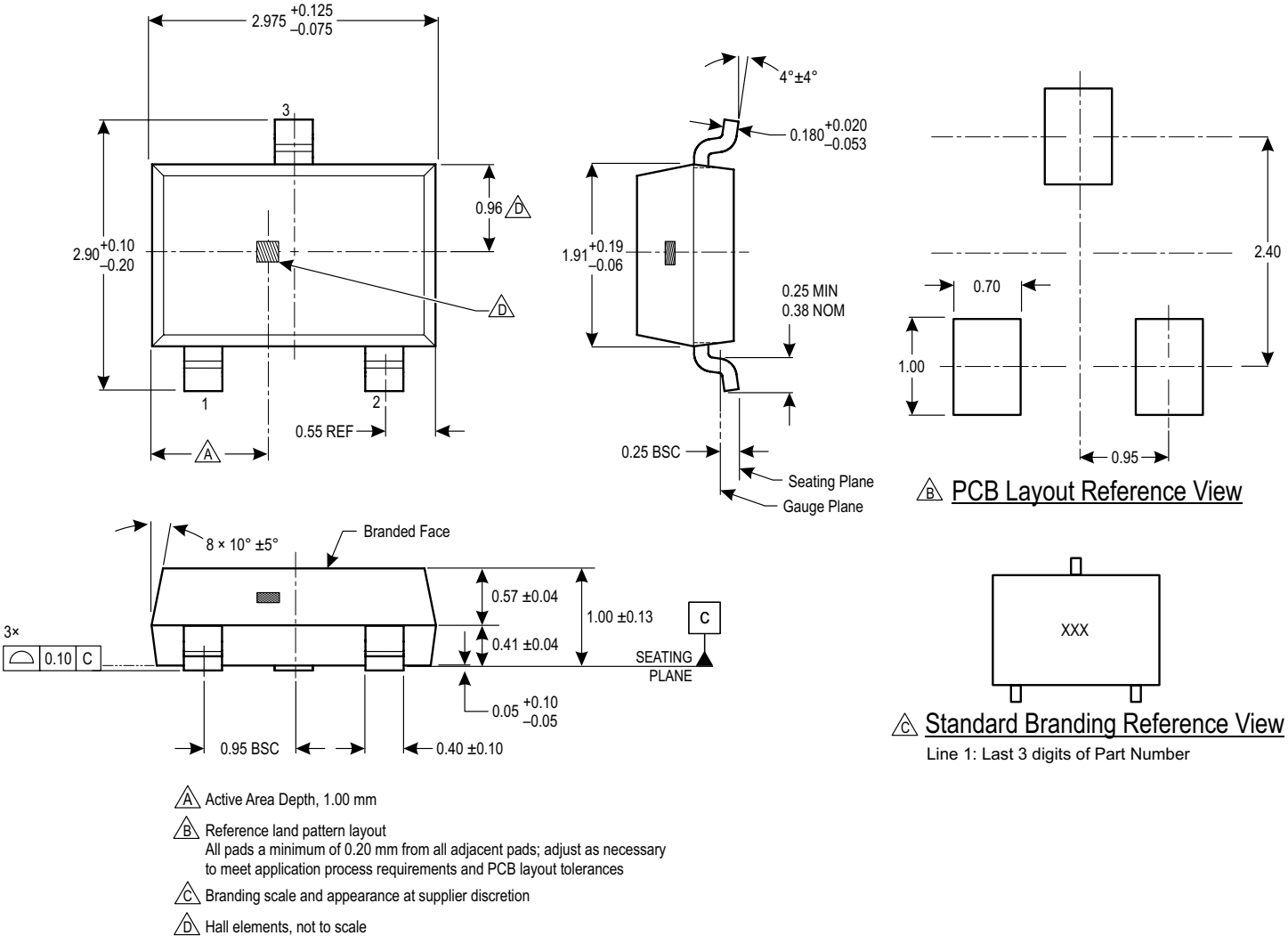
PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000628, Rev. 1)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Active Area Depth, 1.00 mm

B Reference land pattern layout
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

D Hall elements, not to scale

Figure 9: Package LH, 3-Pin SOT23W (A1130LLH, A1131ELH, A1132KLH)

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(Reference DWG-0000404, Rev. 1)
NOT TO SCALE
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

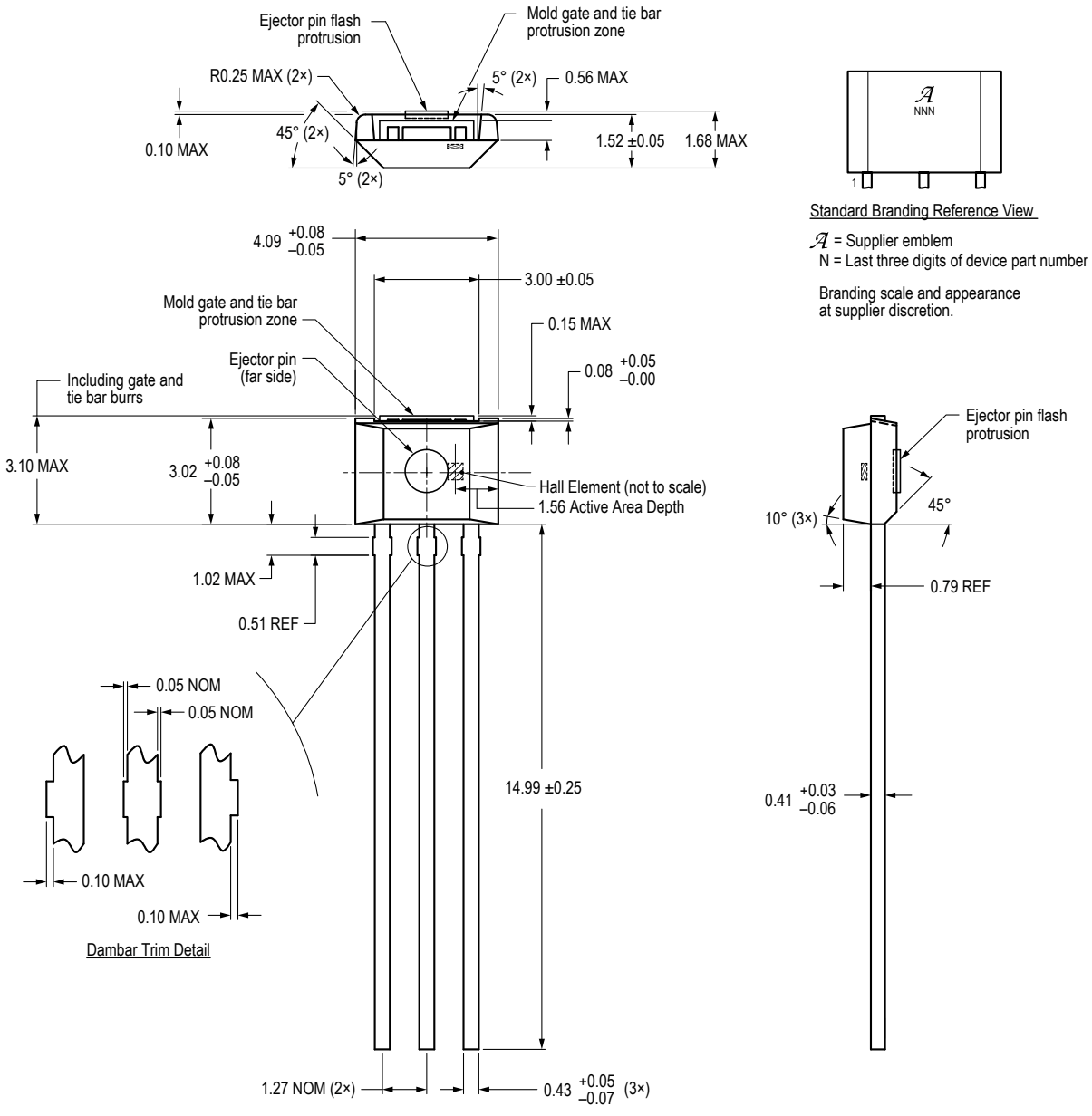

Figure 10: Package UA, 3-Pin SIP (A1130LUA-X)

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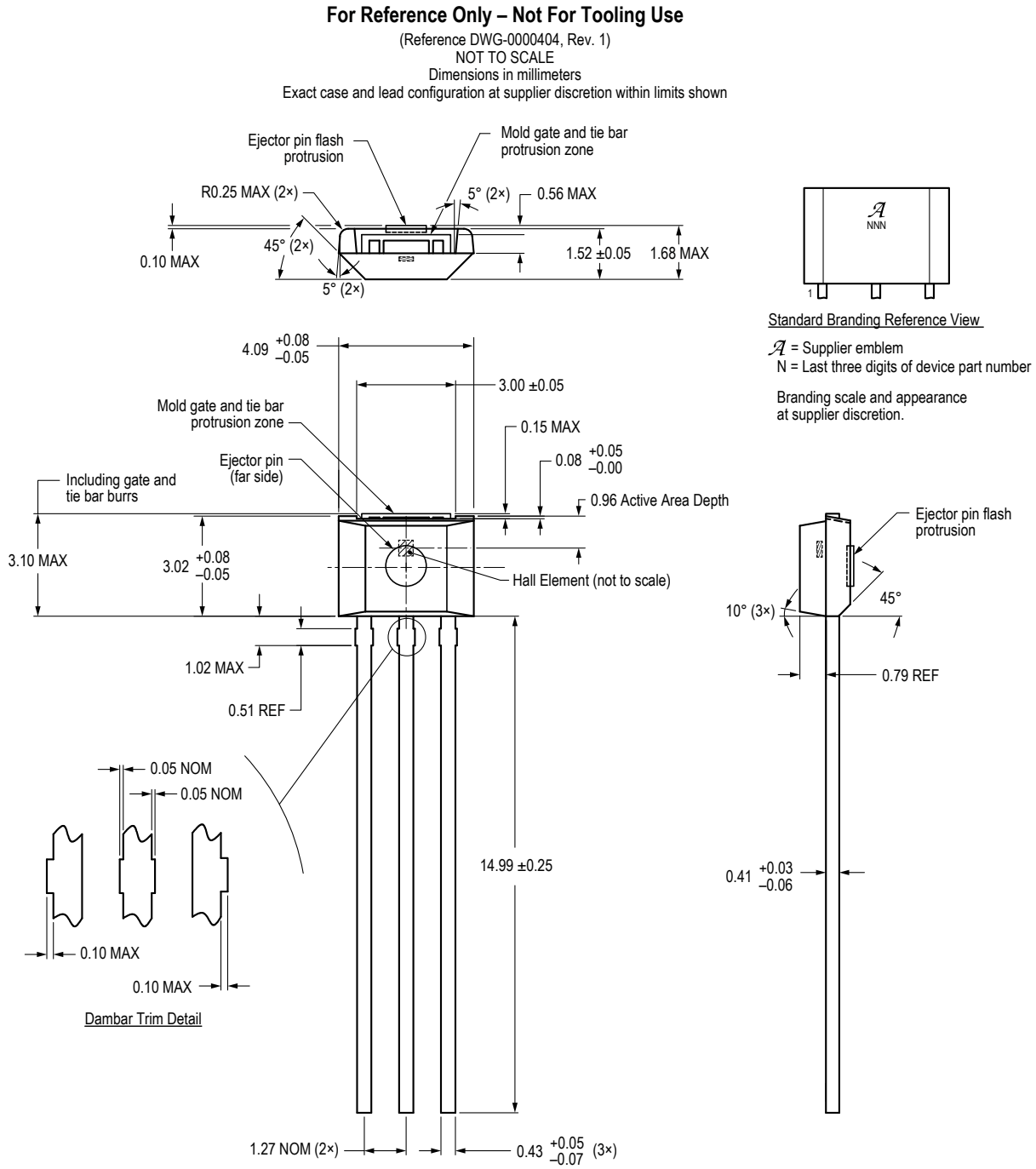

Figure 11: Package UA, 3-Pin SIP (A1130LUA-Y)

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Revision History

Number	Date	Description
–	March 16, 2017	Initial release
1	March 22, 2017	Corrected Typical Supply Currents in Selection Guide (page 2)
2	May 25, 2017	Updated Selection Guide packing information (page 2)
3	June 19, 2018	Minor editorial updates
4	July 11, 2019	Minor editorial updates
5	July 18, 2022	Updated package drawings (pages 21-23)
6	September 30, 2024	Updated product status to last-time buy
7	April 6, 2026	Updated product status to obsolete

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