

ISP3080

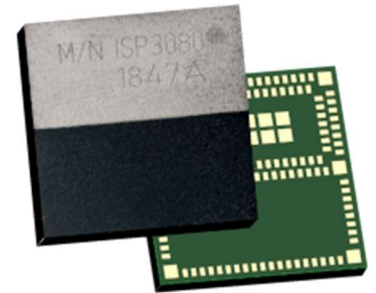
Data Sheet



Ultra-Wide Band and Bluetooth Low Energy

Built-in Antennas Smart Module

This highly miniaturized LGA module, 12 x 12 x 1.5 mm, is based on the QM33110 UWB transceiver and nRF52833 BLE chip. Using a simple user interface via the SPI connection and integrating a Cortex™ M4 CPU, flash and RAM memory combined with optimized antennas, ISP3080 offers the perfect stand-alone ranging module solution for RTLS, access control and indoor positioning applications. The module also includes a 3D accelerometer to allow for low power modes with wake up dictated by movement.



Key Features

- UWB IEEE 802.15.4z
- Bluetooth Low Energy 5.1
Direction Finding and Long Range
- BT Mesh, Thread, Zigbee, ANT+ NFC
- Fira Compatible – Near Field Interaction
- Fully integrated RF Matching and Antenna
UWB 6.5 GHz band 5 and 8.0 GHz band 9
BLE 2.4 GHz
- Integrated 32 MHz & 32 kHz Clocks
- Integrated ultra-low-power high-performance
accelerometer MEMS LIS2DE12
- DC/DC converter with loading circuit
- UWB section based on Qorvo QM33110
- BLE section based on Nordic Semi nRF52833
- Configurable 23 GPIOs including 5 ADCs
- 8 QM33110 GPIOs for UWB functions
- Digital interfaces
USB, QSPI, SPI, UART, I²S, PDM, PWM
- Power supply 2.4 to 3.6V
- Very small size 12 x 12 x 1.5 mm
- Temperature -40 to +85 °C



Applications

- Find Me applications with accurate distance
- Precision Real Time Location Systems (RTLS) for
Healthcare, Sport and Wellness
- Consumer, Industrial...
- Security bubble
- Access control
- Indoor positioning

Certifications

- Bluetooth SIG
- CE
- FCC, IC pending
- TELEC
- RoHS and Reach compliant.
- Conflict Mineral Declaration



Document Revision History

Revision	Date	Ref	Change Description
R0	17/08/2022	cb pg	Initial preliminary release
R1	22/02/2023	cb pg	Updated for ISP3080B version, pad numbering and sizes changed
R2	13/09/2023	er cb	Updated for ISP3080C version, pad numbering and sizes changed
R3	25/09/23	cb pg	ISP3080C changes to pinout and addition of detail for Accelerometer
R4	05/08/24	cb pg	Corrections to schematic and pin list
R5	25/02/25	cb pg	Certification update
R6	13/03/25	cb pg	Packaging information update chapter 5
R7	15/07/2025	bh pg	Moisture sensitivity recommendation update, Tape and Reel update to indicate feed direction of the reel, Add section layout recommendation for connection of crystal

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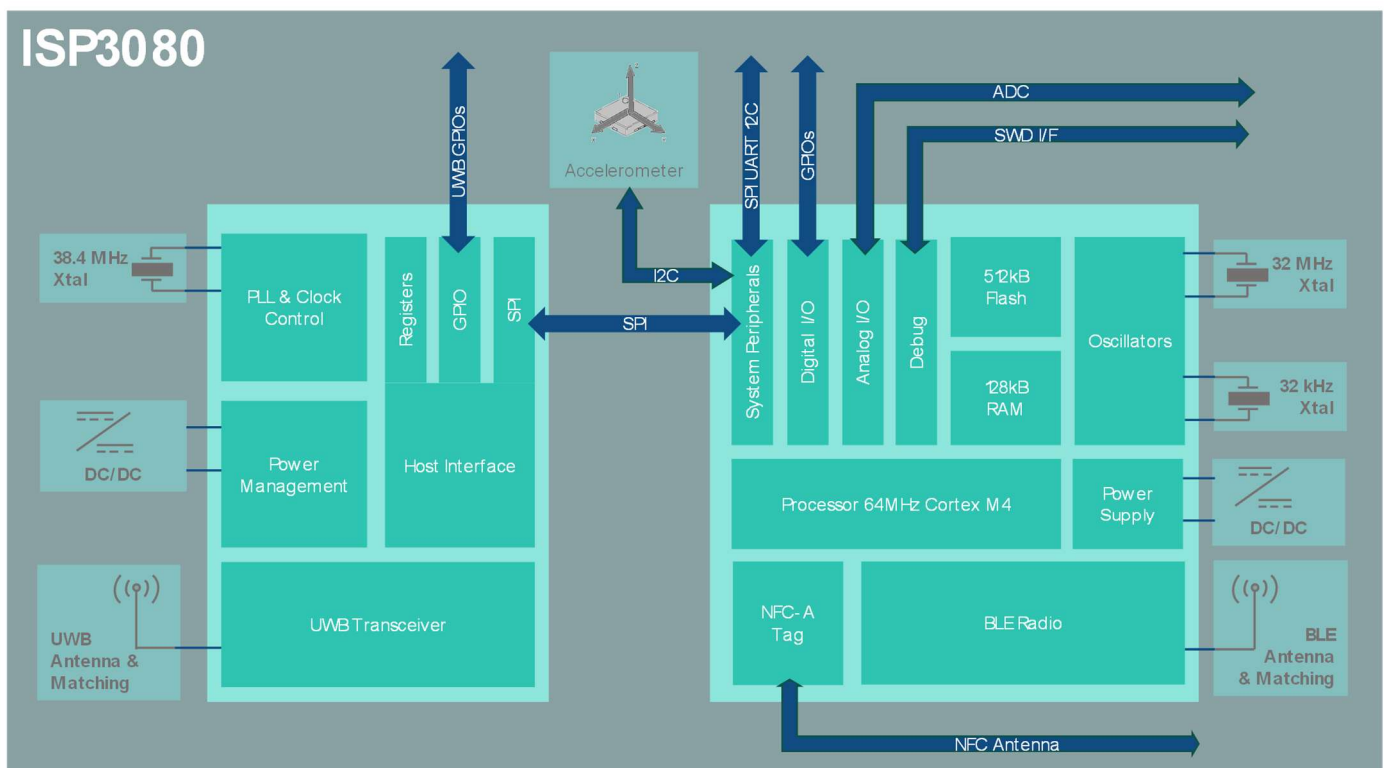
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1. Block Diagram & Features

This module is based on Qorvo / DecaWave QM33110 single-chip UWB transceiver and nRF52833 Nordic Semiconductor 2.4GHz wireless System on Chip (SoC). It integrates a 32-bit ARM Cortex™ M4 CPU, 512 kB flash memory, 128 kB RAM as well as analog and digital peripherals. Despite the small size of 12 x 12 x 1.5 mm, the module integrates decoupling capacitors, 38.4 MHz crystal for UWB, 32 MHz and 32.768 kHz crystals for BLE, DC-DC converters, RF matching circuits and two antennas in addition to the wireless SoCs. Low power consumption and advanced power management enables battery lifetimes up to several months on a coin cell battery.

UWB communication is compliant to IEEE 802.15.4. Using a simple user interface controlled over the air by Bluetooth, ISP3080 offers the perfect stand-alone ranging module solution for RTLS (Precision Real Time Location Systems), indoor positioning, access control and security bubble applications. For long range applications with typically few hundred meters distance, ISP3080 can be used in conjunction with an external UWB antenna.

BLE connectivity is compliant with Bluetooth 5.1 standards, enabling Direction finding and Long Range features over Bluetooth. ISP3080 BLE section can be used either in Peripheral or Central roles for BLE.



2. Specifications

2.1. General Notice

The electrical specifications of the module are directly related to the Nordic Semiconductor specifications for nRF52833 chipset series and the Qorvo specifications for QM33110 chipset. Bellow information is only a summary of the main parameters. For more detailed information, especially about current consumption, please refer to the up-to-date specification of the chipset available on Nordic Semi and Qorvo websites.

2.2. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage VDD	-0.3	3.9	V
USB Supply Voltage respect to ground – VBUS	-0.3	5.8	V
IO Pin Voltage	-0.3	VDD + 0.3	V
UWB RF Input Level to receiver		14	dBm
BLE RF Input Level		10	dBm
NFC Antenna pin current		80	mA
Storage Temperature	-40	+85	°C
Moisture Sensitivity Level		3	-
ESD (Human Body Model)		2000	V
Flash Endurance		10000	cycles



ATTENTION

CONSERVE PRECAUTIONFOR HANDLING
ELECTROSTATIC SENSITIVE DEVICES
Human Body Model Class 3A

2.3. Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Supply Voltage VCC	2.4	3.3	3.6	V
Operating Input Voltage IO Pins P0.xx,P1.yy	0		VCC	V
VBUS Supply Voltage	4.35	5.0	5.5	V
Operating Temperature Range	-40	+25	+85	°C

2.4. Power Consumption

The figures below are given as an indication of overall current consumption. These figures will be updated after measurements during the qualification phase of development.

Parameter	Min	Typ	Max	Unit
UWB receiver CH5		72		mA
UWB receiver CH9		88		mA
UWB transmitter CH5		48		mA
UWB transmitter CH9		59		mA
UWB idle mode		8		mA
UWB sleep mode		260		nA
UWB deep sleep mode		100		nA
BLE Peak current, Receiver active ⁽¹⁾		4.6		mA
BLE Peak current, Transmitter active +8 dBm Output Power ⁽¹⁾		14.2		mA
BLE Peak current, Transmitter active 0 dBm Output Power ⁽¹⁾		4.9		mA
CPU System OFF current, no RAM retention		0.6		μA
CPU System ON base current, full RAM retention		1.8		μA

(1) DCDC enable, Power supply 3V, 1 Mbps

2.5. Clock Sources

Parameter	Min	Typ	Max	Unit
Internal High Frequency Clock for RF Stability: 38.4 MHz Crystal Frequency Tolerance ⁽¹⁾			± 30	ppm
Internal High Frequency Clock for RF Stability: 32 MHz Crystal Frequency Tolerance ⁽¹⁾			± 40	ppm
Internal Low Frequency Clock for BLE Synchronization: 32.768 kHz Crystal Frequency Tolerance ⁽²⁾			± 40	ppm
Internal Low Frequency Clock for BLE Synchronization: RC Oscillator ⁽³⁾			± 250	ppm
RF Frequency tolerance: For UWB operation Channel 5			± 30	ppm
RF Frequency tolerance: For BLE operation Channels0 to 39			± 40	ppm

(1) Including initial tolerance, drift, aging, temperature, and frequency pulling

(2) Including initial tolerance, drift, aging, and frequency pulling

(3) Frequency tolerance after calibration

2.6. Radio Specifications

Parameter	Min	Typ	Max	Unit
UWB channel 5 center frequency		6489.6		MHz
UWB channel 9 center frequency		7987.2		MHz
UWB channel bandwidth		499.2		MHz
UWB Rx sensitivity Level for BER <1%		-93		dBm
UWB Output Power spectral density EIRP			-41.3	dBm/MHz
UWB Antenna Gain channel 5		2		dBi
UWB Antenna Gain channel 9		2		dBi
UWB Load impedance		50		Ω
UWB Range Open field @ 1 m height (1)		50		m
BLE Frequency Range	2402		2480	MHz
BLE Channel 0 to 39 Spacing		2		MHz
BLE Output Power Channels 0 to 39	-20		+8	dBm
BLE Rx sensitivity Level for BER <0,1% ideal Tx	-96			dBm
BLE Max Antenna Gain on small ground plane		-3.1		dBi
BLE EIRP	-43		5	dBm
BLE Range Open field @1m height		70		m

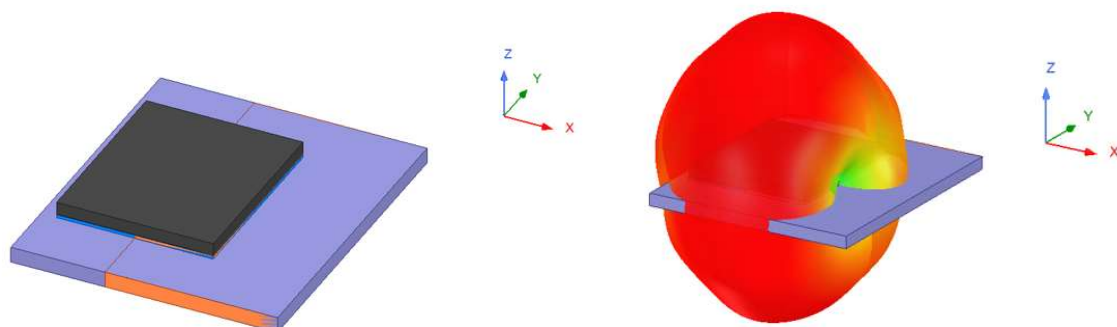
(1) 6.8Mbps / Preamble 128

2.7. UWB Antenna Performance

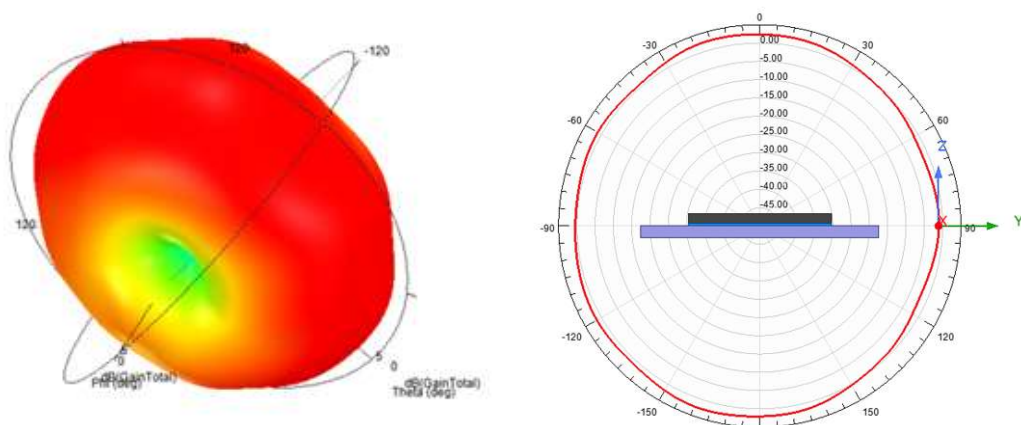
The internal antenna has a maximum absolute gain of 2 dBi. The RF output power of the module is set at 2 dB below the nominal value of -41.3 dBm/MHz to compensate for this antenna gain. The maximum output power rating is -43.3 dBm/MHz at the antenna input.

Note that the patterns shown below are for a small ground plane as shown. Larger ground planes will tend to create a less omnidirectional pattern.

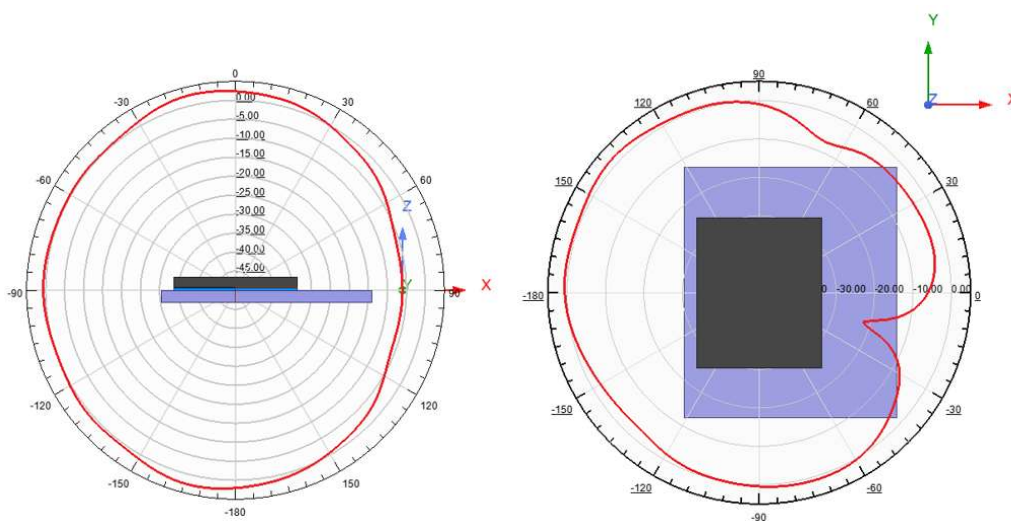
3D Radiation Patterns at 8 GHz



2D Radiation Patterns at 8 GHz



UWB Radiation pattern 2D plot (Theta,Phi=90°)

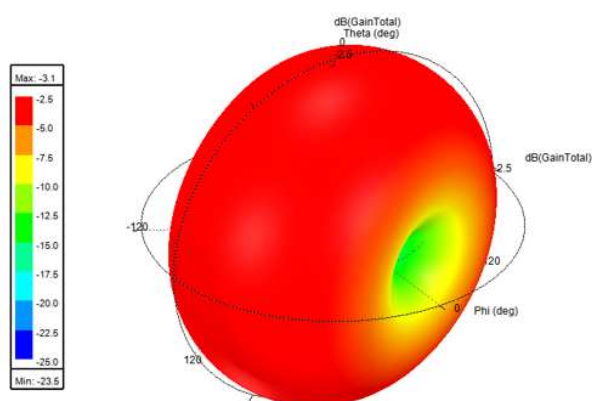


UWB Radiation pattern 2D plot (Theta,Phi=0°)

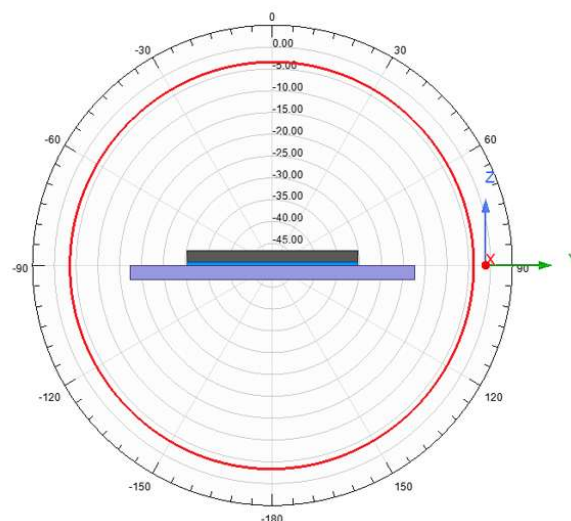
UWB Radiation pattern 2D plot (Phi, Theta=90°)

2.8. BLE Antenna Performance

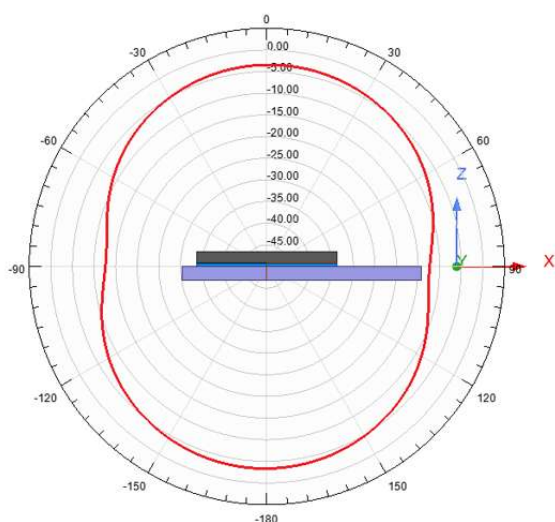
Radiation Patterns at 2.4 GHz



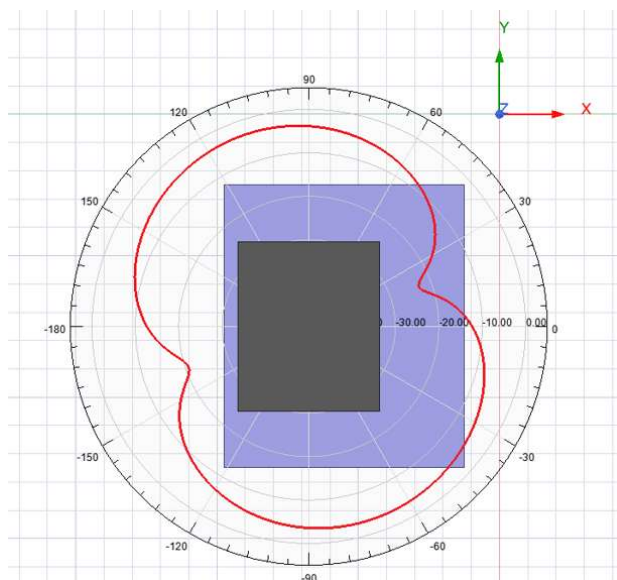
BLE Radiation pattern 3D plot



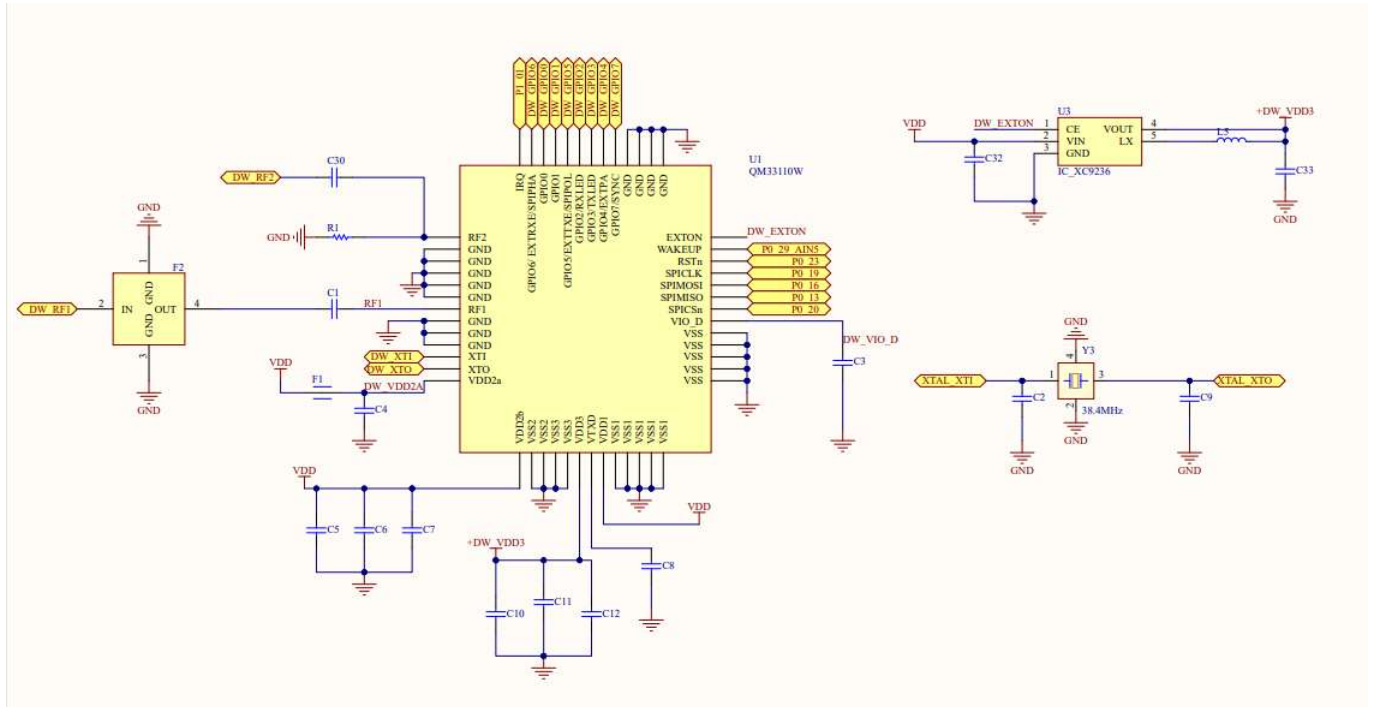
BLE Radiation pattern 2D plot (Theta,Phi=90°)



BLE Radiation pattern 2D plot (Theta,Phi=0°)



BLE Radiation pattern 2D plot (Phi, Theta=90°)



Schematic of the UWB part of the module

2.10. Internal connections

The following nRF52 pins are used to communicate with the QM33110 and therefore must be configured as shown.

nRF Pin Name	DW3000 Pin Name	Description
P0_29	WAKEUP	Wake up
P0_23	RSTn	Reset active low
P0_19	SPICLK	SPI Clock
P0_16	SPIMOSI	SPI Master Output
P0_13	SPIMISO	SPI Master Input
P0_20	SPICSn	SPI Chip Select active low
P1_01	IRQ	Interrupt line

The following nRF52 pins are used to communicate with the accelerometer LIS2DE12 and therefore must be configured as shown or left floating if the accelerometer is not used.

nRF Pin Name	Accelerometer Pin	Description
P1_07	SCL	I2C Clock Pin must be configured with Internal Pull Up
P1_02	SDA	I2C Data Pin must be configured with Internal Pull Up
P0_24	INT1	Interrupt 1 – can be configured as an interrupt
P1_04	INT2	Interrupt 2 – can be configured as an interrupt
P1_06	ACCEL_EN	Accelerometer Enable Pin should be configured as Output High to enable accelerometer.

3. Pin Description

The module uses an LGA format on a 0.50 mm pitch. The pad layout follows the QFN Jedec standard for LGA parts. The NC pads are to be connected to isolated metal pads on the application PCB for mechanical stability and reliability (drop test).

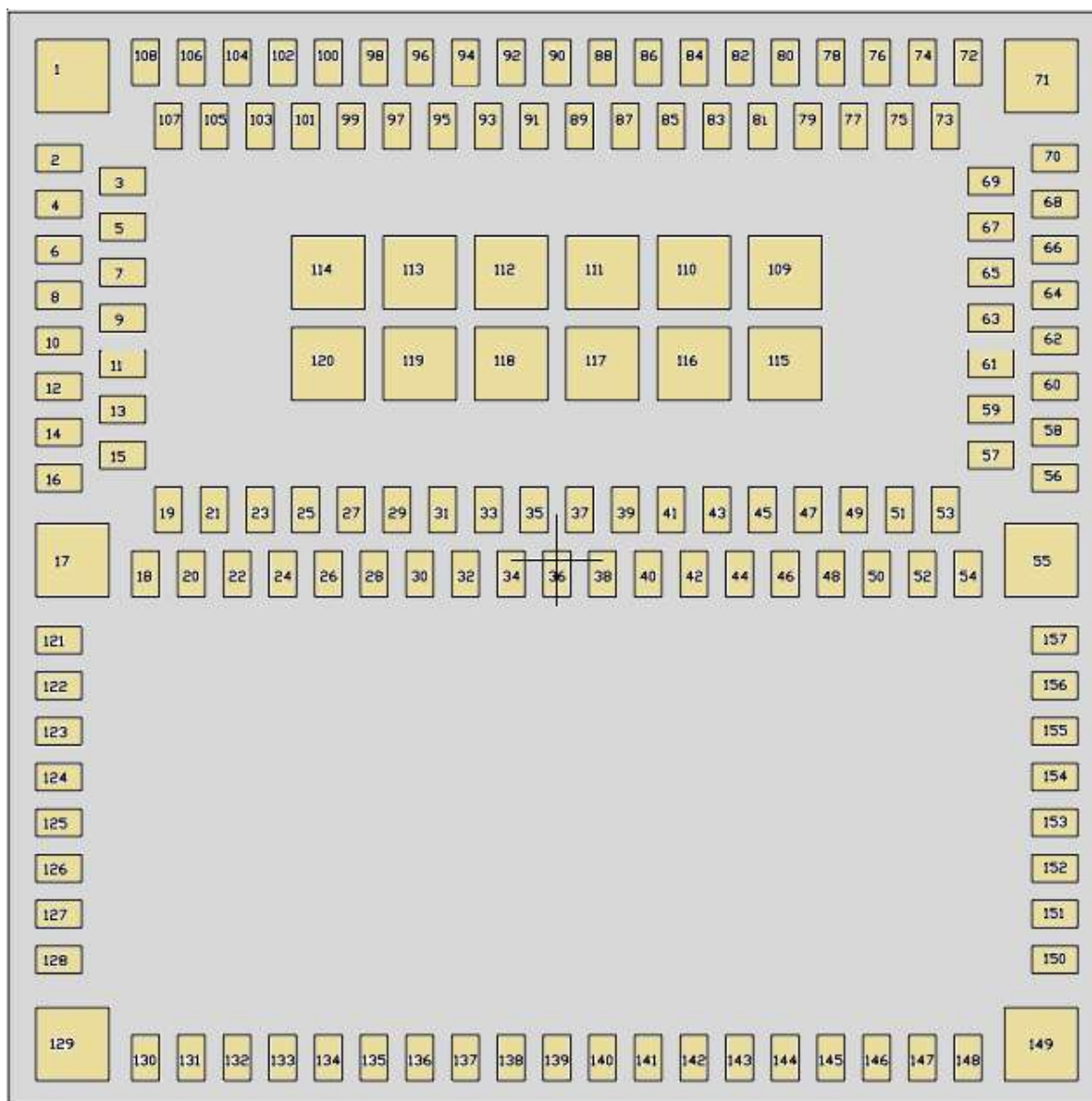
Pin	Name	Pin Function	Description
1	GND	Ground	Ground – Must be connected to ground on application PCB
2	DW_GPIO0	Digital I/O	DW3000 general purpose I/O pin RXOKLED – Pin may be configured to go high on reception of good frame to control Rx LED
3	GND	Ground	Ground – Must be connected to ground on application PCB
4	DW_GPIO1	Digital I/O	DW3000 general purpose I/O pin SFDLED – Pin may be configured to go high on reception of Start Frame Delimiter (SFD) to control SFD LED
5	GND	Ground	Ground – Must be connected to ground on application PCB
6	DW_GPIO5	Digital I/O	DW3000 general purpose I/O pin EXTTXE/SPIPOL At power on selects SPI polarity. The pin may be configured as External Transmitter Enable (EXTTXE). State High during Tx
7	GND	Ground	Ground – Must be connected to ground on application PCB
8	DW_GPIO3	Digital I/O	DW3000 general purpose I/O pin TXLED Pin may be configured to go high after a transmission to control a LED
9	GND	Ground	Ground – Must be connected to ground on application PCB
10	DW_GPIO2	Digital I/O	DW3000 general purpose I/O pin RXLED Pin may be configured to go high during receive mode to control RX LED
11	GND	Ground	Ground – Must be connected to ground on application PCB
12	DW_GPIO4	Digital I/O	DW3000 general purpose I/O pin EXTPA Pin may be configured to control an External Power Amplifier
13	GND	Ground	Ground – Must be connected to ground on application PCB
14	DW_GPIO7	Digital I/O	DW3000 general purpose I/O pin SYNC This pin is used for external synchronization. It has internal pull down and can be reconfigures as a GPIO
15	GND	Ground	Ground – Must be connected to ground on application PCB
16	GND	Ground	Ground – Must be connected to ground on application PCB
17	GND	Ground	Ground – Must be connected to ground on application PCB
18	DW_RF2	N/C	N/C Reserved for future use
19	GND	Ground	Ground – Must be connected to ground on application PCB
20	GND	Ground	Ground – Must be connected to ground on application PCB
21	GND	Ground	Ground – Must be connected to ground on application PCB

Pin	Name	Pin Function	Description
22	GND	Ground	Ground – Must be connected to ground on application PCB
23	GND	Ground	Ground – Must be connected to ground on application PCB
24	UWB_ANT	RF I/O	Internal UWB antenna RF I/O pin Should be connected to DW_RF1 for normal operation
25	GND	Ground	Ground – Must be connected to ground on application PCB
26	DW_RF1	RF I/O	UWB RF I/O pin of the module. Should be connected to UWB_ANT for normal operation.
27	GND	Ground	Ground – Must be connected to ground on application PCB
28	GND	Ground	Ground – Must be connected to ground on application PCB
29	GND	Ground	Ground – Must be connected to ground on application PCB
30	DW_XTI	Clock	DW3000 clock input. Should be connected to XTAL_XTI for normal operation with int XTAL. Input pin for use of external TCXO
31	GND	Ground	Ground – Must be connected to ground on application PCB
32	XTAL_XTI	Clock	38MHz XTAL input. Should be connected to DW_XTI for normal operation with int XTAL. Leave NC when using external TCXO
33	GND	Ground	Ground – Must be connected to ground on application PCB
34	DW_XTO	Clock	DW3000 clock output. Should be connected to XTAL_XTO for normal operation with int XTAL. Leave NC when using external TCXO
35	GND	Ground	Ground – Must be connected to ground on application PCB
36	XTAL_XTO	Clock	38MHz XTAL output. Should be connected to DW_XTO for normal operation with int XTAL. Leave NC when using external TCXO
37	GND	Ground	Ground – Must be connected to ground on application PCB
38	GND	Ground	Ground – Must be connected to ground on application PCB
39	GND	Ground	Ground – Must be connected to ground on application PCB
40	GND	Ground	Ground – Must be connected to ground on application PCB
41	GND	Ground	Ground – Must be connected to ground on application PCB
42	GND	Ground	Ground – Must be connected to ground on application PCB
43	GND	Ground	Ground – Must be connected to ground on application PCB
44	BLE_ANT	RF I/O	Internal BLE antenna RF I/O pin. Should be connected to BLE_OUT for normal operation
45	GND	Ground	Ground – Must be connected to ground on application PCB
46	BLE_OUT	RF I/O	BLE RF I/O pin of the module. Should be connected to BLE_ANT for normal operation
47 -55	GND	Ground	Ground – Must be connected to ground on application PCB
56	PO_09 NFC1	Digital I/O	nRF52 general purpose I/O pin

Pin	Name	Pin Function	Description
57	P0_10 NFC2	Digital I/O	nRF52 general purpose I/O pin
58	GND	Ground	Ground – Must be connected to ground on application PCB
59	GND	Ground	Ground – Must be connected to ground on application PCB
60	VDD	Power	External supply for ISP3080
61	P0_22	Digital I/O	nRF52 general purpose I/O pin
62	SWDIO	Digital I/O	nRF52 Serial Wire Debug I/O for debug and programming
63	GND	Ground	Ground – Must be connected to ground on application PCB
64	SWDCLK	Digital Input	nRF52 Serial Wire Debug clock input for debug and programming
65	P0_17	Digital I/O	nRF52 general purpose I/O pin
66	P0_18 nRESET	Digital I/O	nRF52 general purpose I/O pin
67	P0_14	Digital I/O	nRF52 general purpose I/O pin
68	D+	USB Data	USB D+
69	P0_28 AIN4	Digital I/O	nRF52 general purpose I/O pin
70	D-	USB Data	USB D-
71	GND	Ground	Ground – Must be connected to ground on application PCB
72	VBUS	Power	USB power supply
73	P0_21	Digital I/O	nRF52 general purpose I/O pin
74	P0_06	Digital I/O	nRF52 general purpose I/O pin
75	P0_25	Digital I/O	nRF52 general purpose I/O pin
76	P0_05 AIN3	Digital I/O	nRF52 general purpose I/O pin
77	P0_27	Digital I/O	nRF52 general purpose I/O pin
78	P0_04 AIN2	Digital I/O	nRF52 general purpose I/O pin
79	P0_26	Digital I/O	nRF52 general purpose I/O pin
80	P0_02 AIN0	Digital I/O	nRF52 general purpose I/O pin
81	GND	Ground	Ground – Must be connected to ground on application PCB
82	P0_03 AIN1	Digital I/O	nRF52 general purpose I/O pin
83	GND	Ground	Ground – Must be connected to ground on application PCB
84	P0_11 TRACEDATA2	Digital I/O	nRF52 general purpose I/O pin
85	GND	Ground	Ground – Must be connected to ground on application PCB
86	P0_07 TRACECLK	Digital I/O	nRF52 general purpose I/O pin

Pin	Name	Pin Function	Description
87	GND	Ground	Ground – Must be connected to ground on application PCB
88	P1_09 TRACEDATA3	Digital I/O	nRF52 general purpose I/O pin
89	GND	Ground	Ground – Must be connected to ground on application PCB
90	P0_08	Digital I/O	nRF52 general purpose I/O pin
91	GND	Ground	Ground – Must be connected to ground on application PCB
92	P0_12 TRACEDATA1	Digital I/O	nRF52 general purpose I/O pin
93	GND	Ground	Ground – Must be connected to ground on application PCB
94	P1_00 TRACEDATA0	Digital I/O	nRF52 general purpose I/O pin
95-107	GND	Ground	Ground – Must be connected to ground on application PCB
108	DW_GPIO6	Digital I/O	DW3000 general purpose I/O pin EXTRE/SPIPHA power up SPI Phase selection, may also be configured as External Receiver Enable
109-120	GND	Ground	Ground – Must be connected to ground on application PCB
121-157	NC	Mechanical	These pins must be left NC on the application PCB

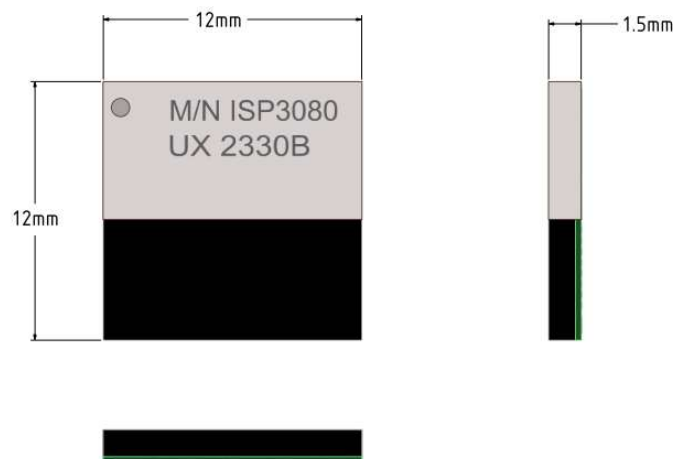
ISP3080 Pinout Top View



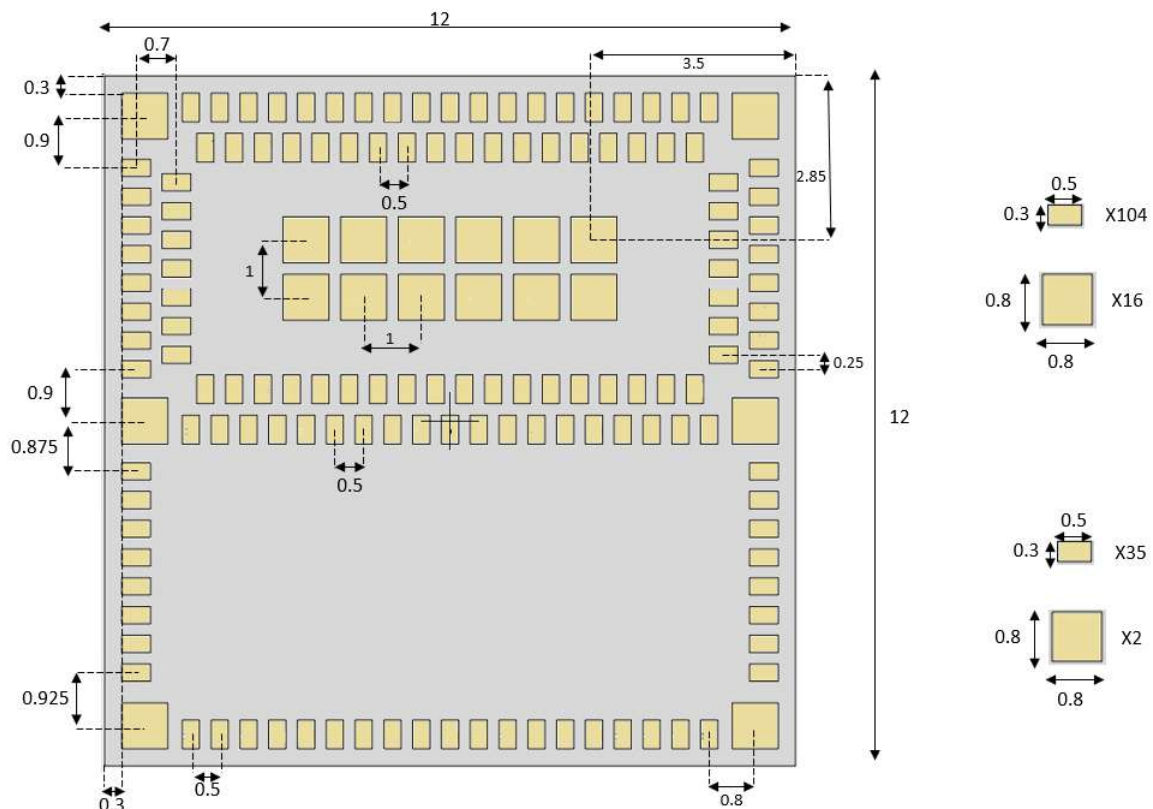
4. Mechanical Outline

4.1. Mechanical Dimensions

Package dimensions (in mm)



Dimensional drawing for 157-Pad LGA Package (in mm)



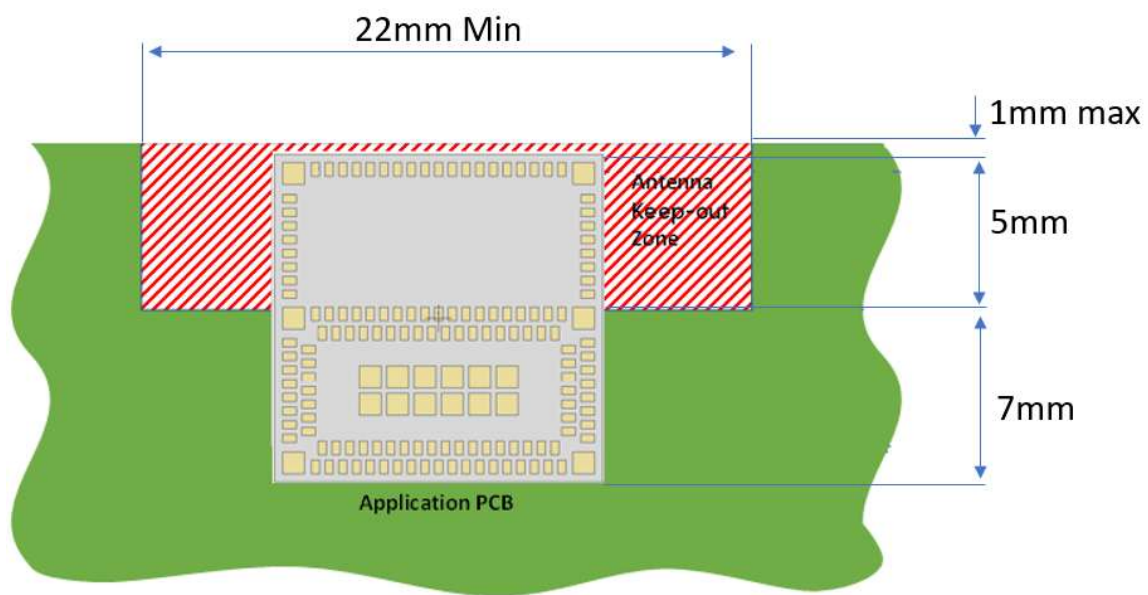
4.2. SMT Assembly Guidelines

For PCB Land Patterns and Solder Mask layout, Insight SiP recommends the use of the same dimensions as the module pads, i.e. 0.3 x 0.5 mm for standard and antenna mechanical pads and 0.8 x 0.8 mm for corner pads.

Please contact Insight SiP for more detailed information.

4.3. Antenna Keep-Out Zone

For optimal antenna performance, it is recommended to respect a metal exclusion zone to the edge of the board: no metal, no traces and no components on any application PCB layer except mechanical LGA pads.

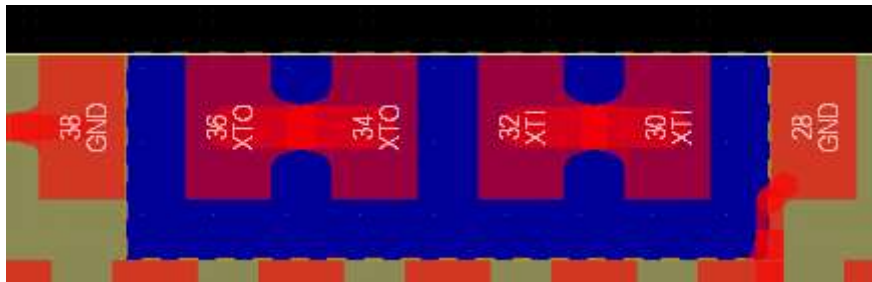


4.4. Layout recommendation for connection of crystal

For optimal performances our module is calibrated to adapt to the internal crystal. This calibration consists in adapting an internal capacitor to fine tune the frequency. When using the internal crystal for your application you need to connect pin 30 to pin 32 and pin 34 to pin 36.

To do so you need a track on your PCB, this track can add parastatic capacitor that could detune the crystal and degrade performances. To avoid this effect pin 30 and pin 32 are next to each other, thus, it is easy to keep a track as short as possible to avoid parasitic effects. (parasitic capacitor on the track between pin 34 and 36 does not have impact on module performance).

The figure below shows the preferred layout around these pins for a 4-layer board (all layers shown with transparence settings on)

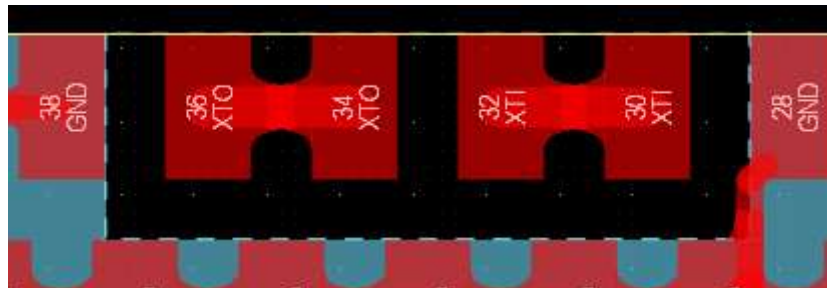


In order to control the parasitic capacitance, there should be no metal on any internal layer under these pads. It is recommended to maintain a keep-out zone on these layers as shown below:

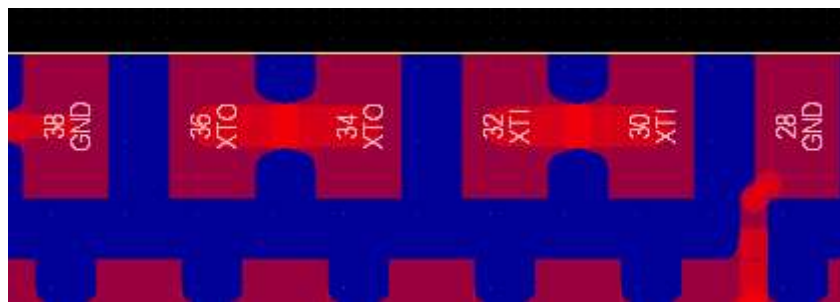
Top layer and internal layer 1:



Top layer and internal layer 2



Top and bottom layers



It is recommended to keep a ground layer on the opposite external side of the PCB.

5. Package & Ordering Information

5.1. Marking

M	/N	:	I	S	P	3	0	8	0										
T	T		Y	Y	W	W	R		B	B	B	B	B	B	B	B	B	B	B

● M/N: ISP3080
WX YYWW/B BBBBBBBBBB

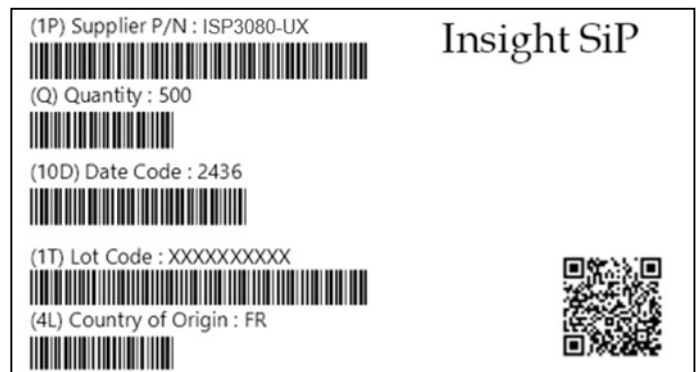
ISP3080	Part Number
TT	2 letters Module Type
YY	2 digits year number
WW	2 digits week number
R	1 letter Hardware revision
BBBBBBBBBB	10 characters Build code

Certification labels for CE, FCC, IC and Telec are printed directly on the module when applicable.

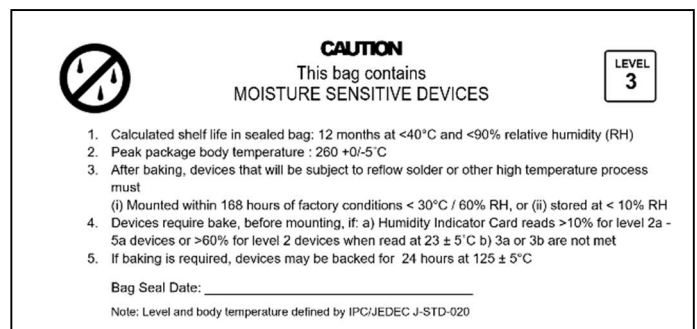
5.2. Package Labelling

A label indicating the Module Part Number, Quantity, Date Code, Lot Code and Country of Origin is applied to the bag, the reel and the box, whichever is applicable.

Information is available with bar code 1D according to Code 39 and bar code 2D according to Data Matrix ECC 200 from ECIA standard.



A second label on the bag is present to indicate the MSL level and packaging date.



5.3. Prototype Packaging

For engineering samples and prototype quantities up to 99 units, deliveries are provided in thermoformed trays.

They are delivered in vacuumed sealed pack with desiccant pack and humidity sensors. Please see section 6.2 for more information on moisture sensitivity.

Please order with “ST” code packaging suffix.

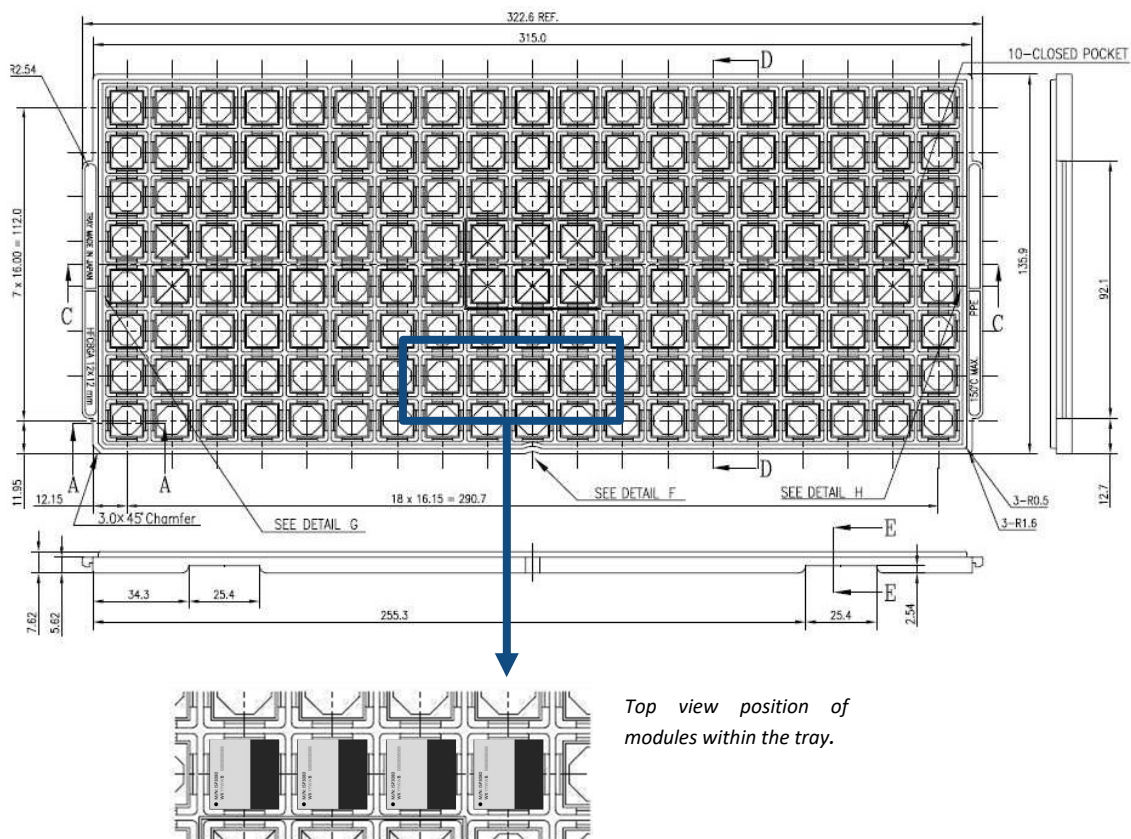


5.4. Jedec Trays

For pre-production volumes, ISP3080 are available in Jedec trays.

They are delivered in vacuumed sealed pack with desiccant pack and humidity sensors. These Jedec trays are also suitable for further baking at 125°C. Please see section 6.2 for more information on moisture sensitivity. Please order with “JT” code packaging suffix.

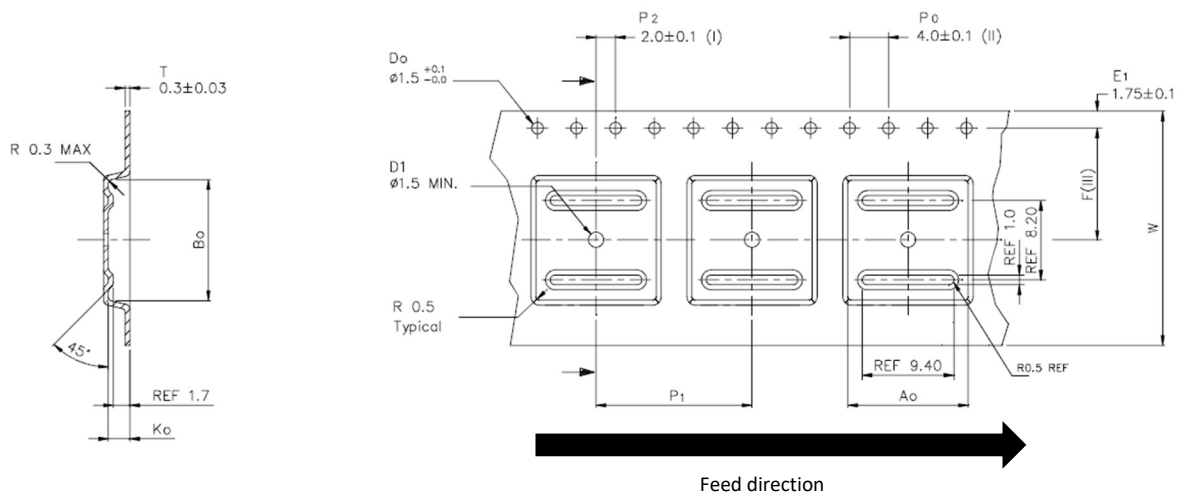
Refer to tray sizes below. Complete information on Jedec trays is available on request.



5.5. Tape and Reel

ISP3080 are also available in Tape & Reel. They are delivered in vacuumed sealed pack with desiccant pack and humidity sensors. Reels are proposed in standard quantities of 500 units (330 mm / 13" reel). Please order with "RS" code packaging suffix for 500-unit reel.

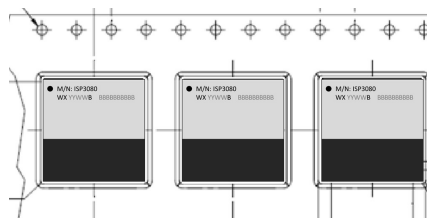
This packaging is not suitable for high temperature baking.



A ₀	12.35 +/−0.1
B ₀	12.35 +/−0.1
K ₀	2.20 +/−0.1
F	11.50 +/−0.1
P ₁	16.00 +/−0.1
W	24.15 +/−0.1

- (I) Measured from centreline of sprocket hole to centreline of pocket.
- (II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
- (III) Measured from centreline of sprocket hole to centreline of pocket.
- (IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATEI



Top view position of modules within the reel.

5.6. Ordering Information

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Part Number

WiFi extra Memory

Evaluation Board

Test board

Standard Tray

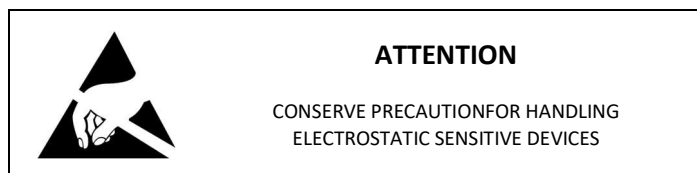
Jedec Tray Packaging

Reel of 500 units

6. Storage & Soldering information

6.1. Storage and Handling

- Keep this product away from other high frequency devices which may interfere with operation such as other transmitters and devices generating high frequencies.
- Do not expose the module to the following conditions:
 - Corrosive gasses such as Cl₂, H₂S, NH₃, SO₂, or NO_x
 - Extreme humidity or salty air
 - Prolonged exposure to direct Sunlight
 - Temperatures beyond those specified for storage
- Do not apply mechanical stress
- Do not drop or shock the module
- Avoid static electricity, ESD and high voltage as these may damage the module



6.2. Moisture Sensitivity

ISP3080 has been tested MSL-3 according to standards.

All plastic packages absorb moisture. During typical solder reflow operations when SMDs are mounted onto a PCB, the entire PCB and device population are exposed to a rapid change in ambient temperature. Any absorbed moisture is quickly turned into superheated steam. This sudden change in vapor pressure can cause the package to swell. If the pressure exerted exceeds the flexural strength of the plastic mold compound, then it is possible to crack the package. Even if the package does not crack, interfacial delamination can occur.

To prevent such failures, baking is mandatory before assembly under the following conditions (per JEDEC standards J-STD-033 and J-STD-020):

- The vacuum-sealed moisture barrier bag has been stored for more than 12 months from the date of sealing.
- The moisture barrier bag seems to be damaged or the humidity indicator card shows humidity levels above the acceptable threshold.
- The bag has been opened, and the components have been exposed to ambient conditions (approximately $\leq 30^{\circ}\text{C}/60\% \text{ RH}$) for more than 168 hours.

In case one the above condition is true, please follow the baking instructions below before assembly:

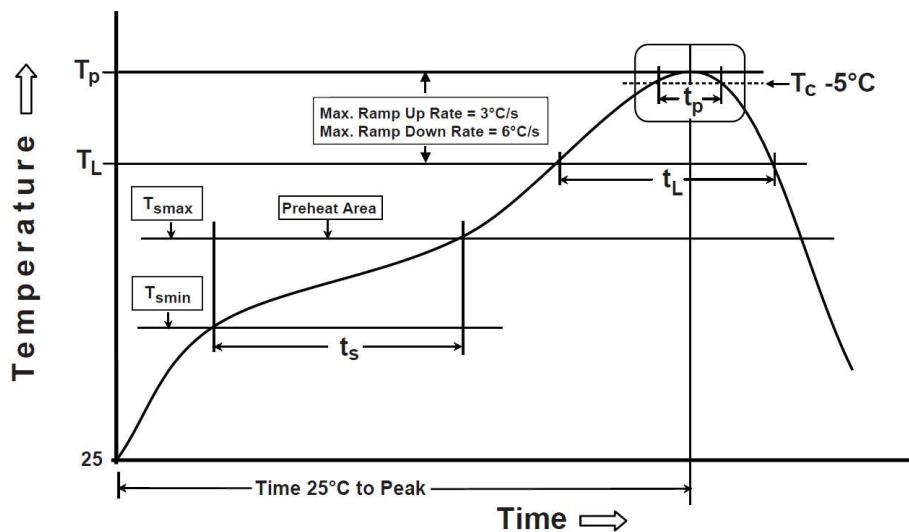
- Remove the modules from the reels, place them in trays or plates capable of withstand elevated temperatures
- Bake them at 125°C for 24 hours (Minimum required bake time for MSL3 components with 1 mm thickness before assembling is 8 hours according to JEDEC J-STD-033D in table 4-1)

After baking, modules can be handled at room conditions (approximately $\leq 30^{\circ}\text{C}/60\% \text{ RH}$) for up to 168 hours before assembly.



6.3. Soldering information

Recommendation for RoHS reflow process is according to Jedec J-STD-020 and 033 standard profiles.



Preheat/Soak	
Temperature Min (T_{smin})	150 °C
Temperature Max (T_{smax})	200 °C
Time (t_s) from (T_{smin} to T_{smax})	60-120 sec
Ramp-up rate (T_L to T_p)	3 °C/sec max
Liquidous temperature (T_L)	217 °C
Time (t_L) maintained above T_L	60-150 sec

Peak package body temperature (T_p)	260°C (+0/-5°C)
Classification Temperature (T_c)	260 °C
Time (t_p) maintained above $T_c - 5^{\circ}\text{C}$	30 sec
Ramp-down rate (T_p to T_L)	6 °C/sec max
Time 25 °C to peak temperature	8 mn max

7. Quality & User information

7.1. Certifications

- CE – Declaration of Conformity N° TR240802
- FCC – Certification pending
- IC – Certification pending
- TELEC – Certification N° 020-230401
- Bluetooth SIG – Declaration ID #D066527
- RoHS3 compliant
- Reach compliant
- Minerals responsible initiative compliant

Further paragraphs will be added to this data sheet once the product is fully certified.

7.2. Discontinuity

Normally a product will continue to be manufactured as long as all of the following are true:

- The manufacturing method is still available.
- There are no replacement products.
- There is demand for it in the market.

In case of obsolescence, Insight SiP will follow Jedec Standard JSD-48. A Product Discontinuation Notice (PDN) will be sent to all distributors and made available on our website. After this, the procedure goes as follows:

- Last Order Date will be 6 months after the PDN was published.
- Last Shipment Date will be 6 months after Last Order Date, i.e. 12 months after PDN.

7.3. Disclaimer

Insight SiP's products are designed and manufactured for general consumer applications, so testing and use of the product shall be conducted at customer's own risk and responsibility. Please conduct validation and verification and sufficient reliability evaluation of the products in actual condition of mounting and operating environment before commercial shipment of the equipment. Please also pay attention (i) to apply soldering method that don't deteriorate reliability, (ii) to minimize any mechanical vibration, shock, exposure to any static electricity, (iii) not to overstress the product during and after the soldering process.

The products are not designed for use in any application which requires especially high reliability where malfunction of these products can reasonably be expected to result in personal injury or damage to the third party's life, body or property, including and not limited to (i) aircraft equipment, (ii) aerospace equipment, (iii) undersea equipment, (iv) power plant control equipment, (v) medical equipment, (vi) transportation equipment, (vii) traffic signal equipment, (viii) disaster prevention / crime prevention equipment.

The only warranty that Insight SiP provides regarding the products is its conformance to specifications provided in datasheets. Insight SiP hereby disclaims all other warranties regarding the products, express or implied, including without limitation any warranty of fitness for a particular purpose, that they are defect-free, or against infringement of intellectual property rights. Insight SiP customers agree to indemnify and defend Insight SiP against all claims, damages, costs and expenses that may be incurred, including without any limitation, attorney fees and costs, due to the use of products.