PE42542

Document category: Product Specification

UltraCMOS® SP4T RF Switch, 9 kHz–18 GHz

Features

- HaRP™ technology enhanced:
  - Fast settling time
  - No gate or phase lag
  - No drift in insertion loss or phase
- Low insertion loss:
  - 1.10 dB @ 3 GHz
  - 2.10 dB @ 13.5 GHz
  - 2.50 dB @ 16 GHz
  - 3.10 dB @ 18 GHz
- High isolation:
  - 55 dB @ 3 GHz
  - 33 dB @ 13.5 GHz
  - 29 dB @ 16 GHz
  - 26 dB @ 18 GHz
- ESD performance:
  - 2500V HBM on all pins
  - 150V MM on all pins
  - 500V CDM on all pins
- Packaging: 29-lead 4 × 4 mm LGA

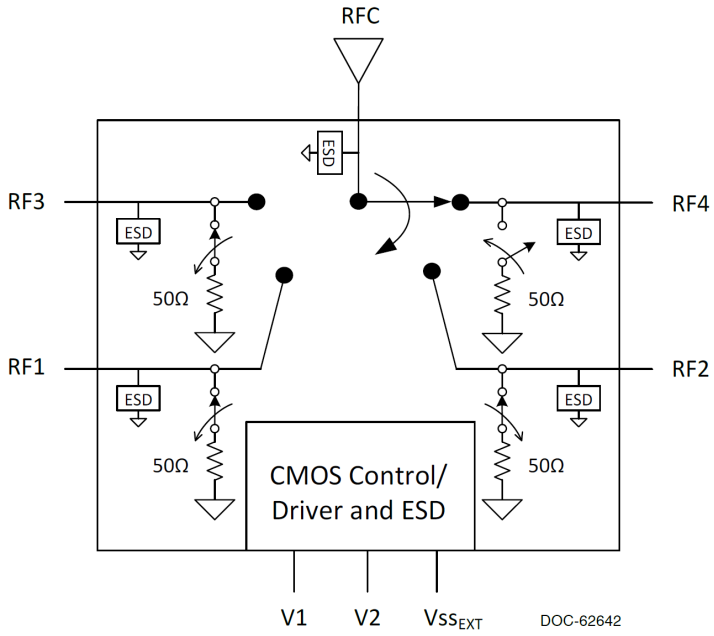

Figure 1. PE42542 functional block diagram

Product description

The PE42542 is a HaRP™ technology-enhanced absorptive SP4T RF switch designed for use in test and measurement, automated test equipment (ATE), microwave, and other wireless applications. This broadband general-purpose switch maintains excellent RF performance and linearity from 9 kHz through 18 GHz. The PE42542 exhibits low insertion loss, high isolation performance, and has fast settling time. No blocking capacitors are required if no DC voltage is present on the RF ports.

The PE42542 is manufactured using the pSemi UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

pSemi's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

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Headquarters: 9369 Carroll Park Dr, San Diego, CA 92121

Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. PE42542 absolute maximum ratings

Parameter or condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	5.5	V
Digital input voltage (V1, V2)	V_{CTRL}	-0.3	3.6	V
RF input power, CW (RFC–RFx)[3] 9 kHz–2.9 MHz ≥ 2.9 MHz–18 GHz	$P_{MAX,CW}$	–	See Figure 2 33	dBm
RF input power, pulsed (RFC–RFx)[4] 9 kHz–2.9 MHz ≥ 2.9 MHz–18 GHz	$P_{MAX,PULSED}$	–	See Figure 2 34	dBm
RF input power into terminated ports, CW (RFx)[3] 9 kHz–1.4 MHz ≥ 1.4 MHz–18 GHz	$P_{MAX,TERM}$	–	See Figure 2 22	dBm
Storage temperature range	T_{ST}	-65	+150	°C
ESD voltage HBM, all pins[3]	$V_{ESD,HBM}$	–	2500	V
ESD voltage MM, all pins[4]	$V_{ESD,MM}$	–	150	V
ESD voltage CDM, all pins[5]	$V_{ESD,CDM}$	–	500	V

1. 100% duty cycle, all bands, 50Ω.
2. Pulsed, 5% duty cycle of 4620 µs period, 50Ω.
3. Human Body Model (MIL_STD 883 Method 3015).
4. Machine Model (JEDEC JESD22-A115).
5. Charged Device Model (JEDEC JESD22-C101).

Recommended operating conditions

Table 2 lists the PE42542 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. PE42542 operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Normal mode (V_{SS_EXT} = 0V)[1]					
Supply voltage	V_{DD}	2.3	–	5.5	V
Supply current	I_{DD}	–	120	200	µA
Bypass mode (V_{SS_EXT} = -3.4V)[2]					
Supply voltage	V_{DD}	2.7	3.4	5.5	V
Supply current	I_{DD}	–	50	80	µA
Negative supply voltage	V_{SS_EXT}	-3.6	–	-3.2	V
Negative supply current	I_{SS}	-40	-16	–	µA
Normal or bypass mode					
Digital input high (V1, V2)	V_{IH}	1.17	–	3.6	V
Digital input low (V1, V2)	V_{IL}	-0.3	–	0.6	V
RF input power, CW (RFC–RFx)[3] 9 kHz–2.9 MHz ≥ 2.9 MHz–18 GHz	$P_{MAX,CW}$	–	–	See Figure 2 30	dBm
RF input power, pulsed (RFC–RFx)[4] 9 kHz–2.9 MHz ≥ 2.9 MHz–18 GHz	$P_{MAX,PULSED}$	–	–	See Figure 2 32	dBm
RF input power into terminated ports, CW (RFx)[3] 9 kHz–1.4 MHz ≥ 1.4 MHz–18 GHz	$P_{MAX,TERM}$	–	–	See Figure 2 20	dBm
Operating temperature range	T_{OP}	-40	+25	+85	°C

1. Normal mode: Connect V_{SS_EXT} (pin 29) to GND (V_{SS_EXT} = 0V) to enable the internal negative voltage generator.
2. Bypass mode: Use V_{SS_EXT} (pin 29) to bypass and disable the internal negative voltage generator.
3. 100% duty cycle, all bands, 50Ω.
4. Pulsed, 5% duty cycle of 4620 µs period, 50Ω.

Electrical specifications

Table 3 lists the PE42542 key electrical specifications at +25 °C (Z_S = Z_L = 50Ω), unless otherwise specified.

- Normal mode: V_{DD} = 3.3V, V_{SS_EXT} = 0V(1)
- Bypass mode: V_{DD} = 3.4V, V_{SS_EXT} = -3.4V(2)

Table 3. PE42542 electrical specifications

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency	–	–	9 k	–	18 G	Hz
Insertion loss	RFC–RFx	9 kHz–10 MHz 10–3000 MHz 3000–7500 MHz 7500–10000 MHz 10000–13500 MHz 13500–16000 MHz 16000–18000 MHz	–	0.70 1.10 1.50 1.75 2.10 3.10 3.90	0.90 1.40 1.95 2.20 2.40 3.50 4.50	dB
Isolation	RFx–RFx	9 kHz–10 MHz 10–3000 MHz 3000–7500 MHz 7500–10000 MHz 10000–13500 MHz 13500–16000 MHz 16000–18000 MHz	80 53 46 42 35 30 26	90 55 48 44 37 31 27	–	dB
Isolation	RFC–RFx	9 kHz–10 MHz 10–3000 MHz 3000–7500 MHz 7500–10000 MHz 10000–13500 MHz 13500–16000 MHz 16000–18000 MHz	80 54 41 36 31 27 24	90 55 42 38 33 29 26	–	dB
Return loss (active and common port)	RFC–RFx	9 kHz–10 MHz 10–3000 MHz 3000–18000 MHz	–	35 15 13	–	dB
Return loss (terminated port)	RFx	9 kHz–18000 MHz	–	16	–	dB
Input 0.1 dB compression point(3)	RFC–RFx	–	–	See Figure 2	–	dBm
Input IP2	RFC–RFx	10–18000 MHz	–	118	–	dBm
Input IP3	RFC–RFx	10–18000 MHz	–	58	–	dBm
Settling time	–	50% CTRL to 0.05 dB final value	–	7	10	µs
Switching time(4)	–	50% CTRL to 90% or 10% of final value	–	3	4.5	µs

Parameter	Path	Condition	Min	Typ	Max	Unit

1. Normal mode: Connect V_{SS_EXT} (pin 29) to GND (V_{SS_EXT} = 0V) to enable the internal negative voltage generator.
2. Bypass mode: Use V_{SS_EXT} (pin 29) to bypass and disable the internal negative voltage generator.
3. The input 0.1 dB compression point is a linearity figure of merit. For the RF input power P_{MAX} (50Ω), see Table 2.
4. The PE42542 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (pin 29 = GND). The switching frequency describes the time duration between switching events. The switching time is the duration between the point that the control signal reaches 50% of the final value and the point that the output signal reaches within 10% or 90% of its target value.

Optional external V_{SS} control (V_{SS_EXT})

For proper operation, the V_{SS_EXT} control pin must be grounded or tied to the V_{SS} voltage specified in Table 2. When the V_{SS_EXT} control pin is grounded, the FETs in the switch are biased with an internal negative voltage generator. For applications that require the lowest possible spurious performance, V_{SS_EXT} can be applied externally to bypass the internal negative voltage generator.

Spurious performance

The PE42542 typical spurious performance is –150 dBm when V_{SS_EXT} = 0V (pin 29 = GND). To improve performance, disable the internal negative voltage generator by setting V_{SS_EXT} = –3.4V.

SP4T control logic

Table 4. PE42542 truth table

State	V1	V2
RF1 on	0	0
RF2 on	1	0
RF3 on	0	1
RF4 on	1	1

Hot switching

The PE42542 maximum hot switching capability is 20 dBm from 1.4 MHz to 18 GHz. The maximum hot switching capability below 1.4 MHz does not exceed the maximum RF CW terminated power shown in Figure 2. Hot switching occurs when RF power is applied while switching between the RF ports.

Power de-rating curves

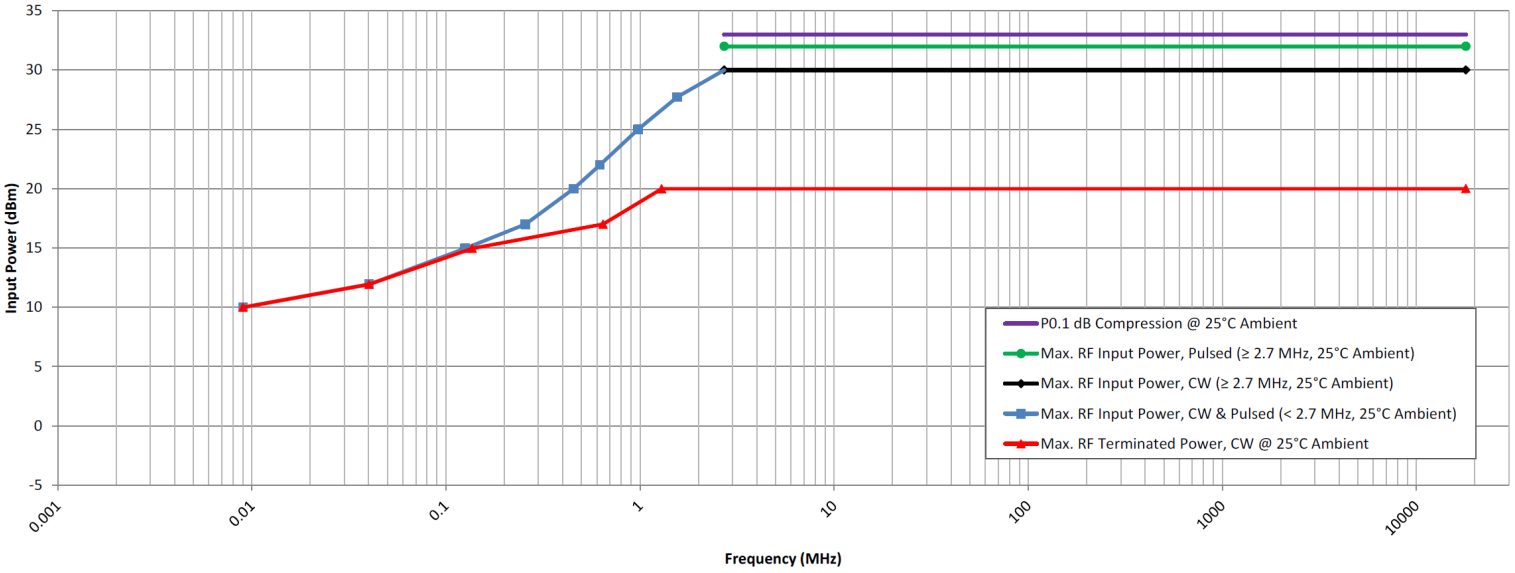


Figure 2. Power de-rating curve for 9 kHz–18 GHz @ 25°C ambient (50Ω)

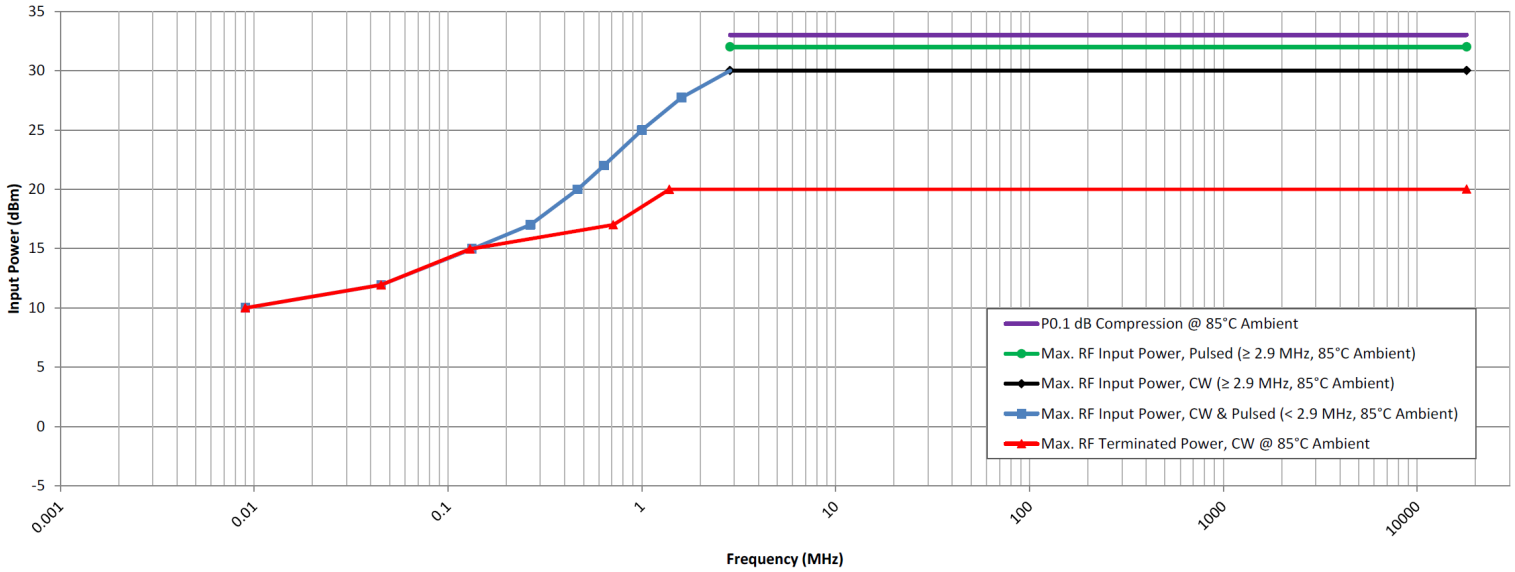


Figure 3. Power de-rating curve for 9 kHz–18 GHz @ 85°C ambient (50Ω)

Typical performance data

Figure 4–Figure 18 show the typical performance data at +25 °C and V_{DD} = 3.3V (Z_S = Z_L = 50Ω), unless otherwise specified.

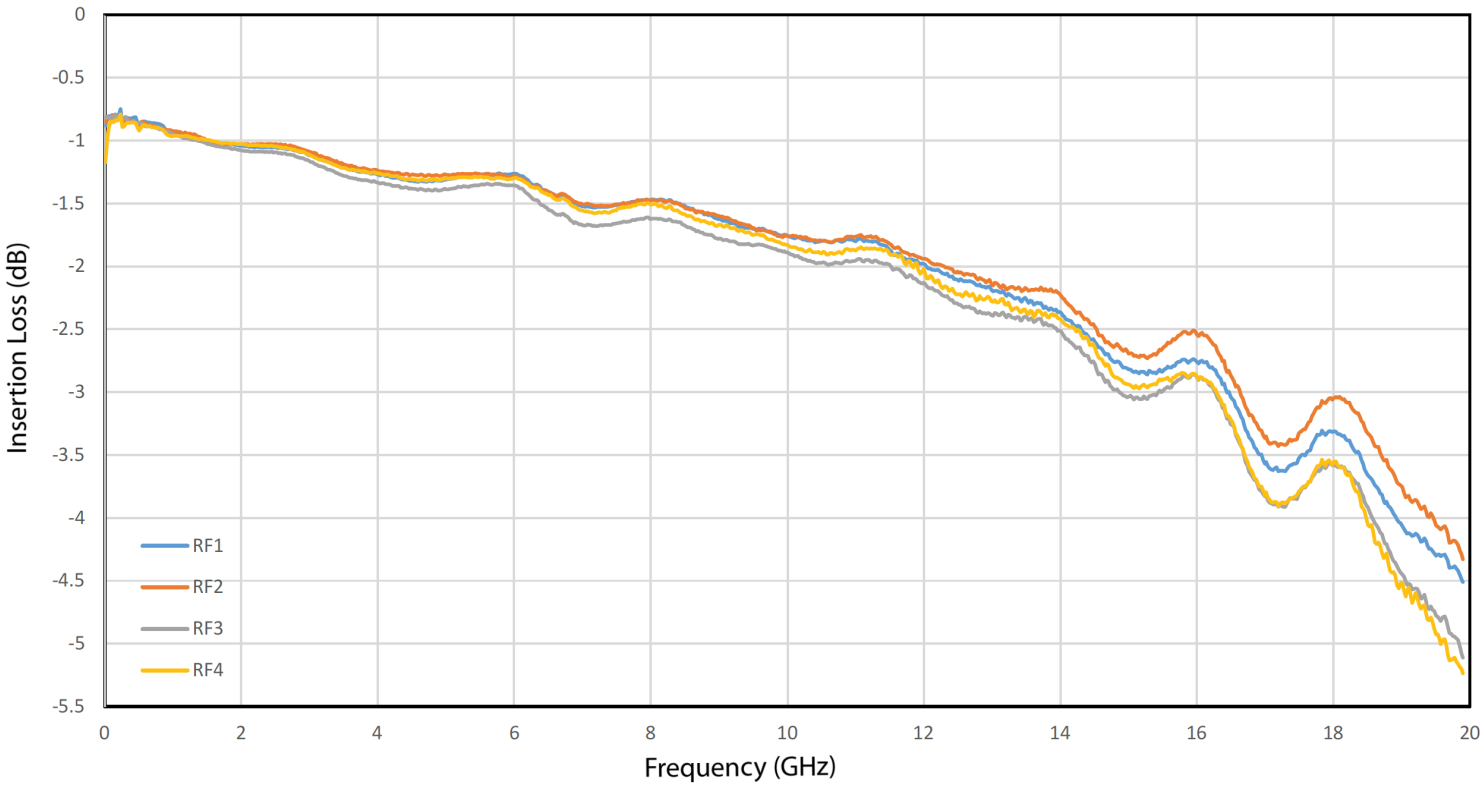


Figure 4. Insertion loss (RFC–RFx)

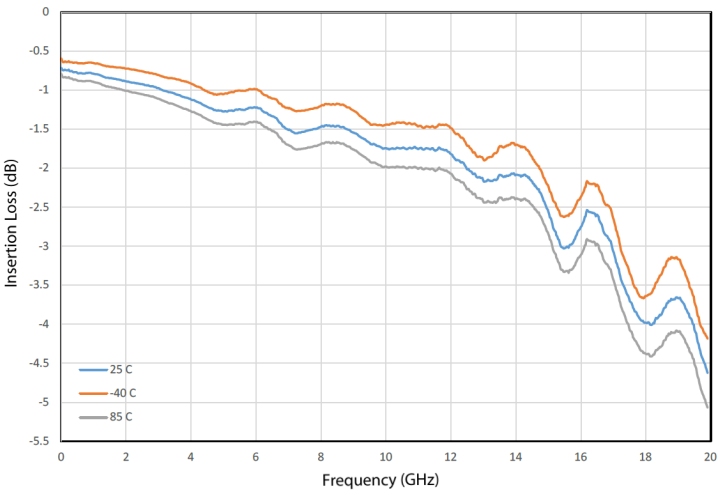


Figure 5. Insertion loss vs. temperature (RFC–RFx)

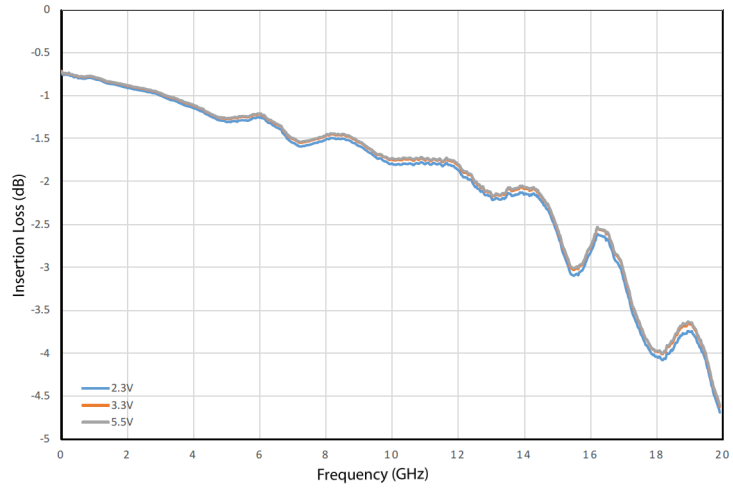


Figure 6. Insertion loss vs. V_{DD} (RFC–RFx)

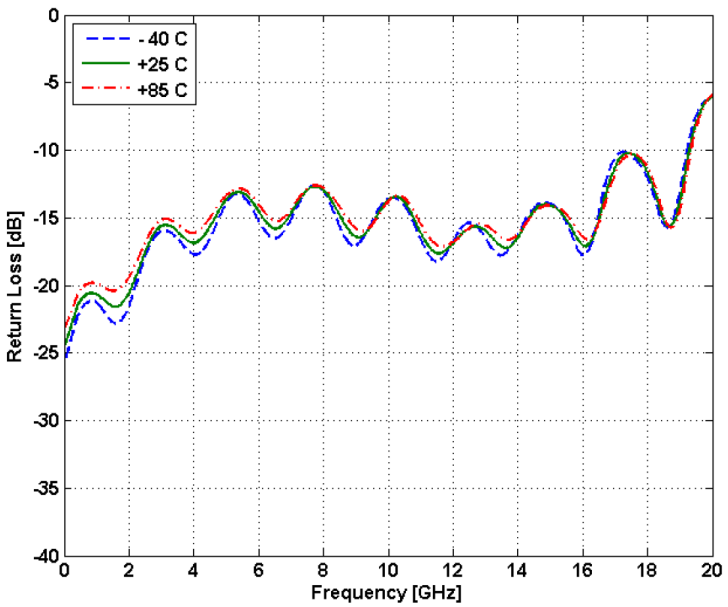


Figure 7. RFC port return loss vs. temperature

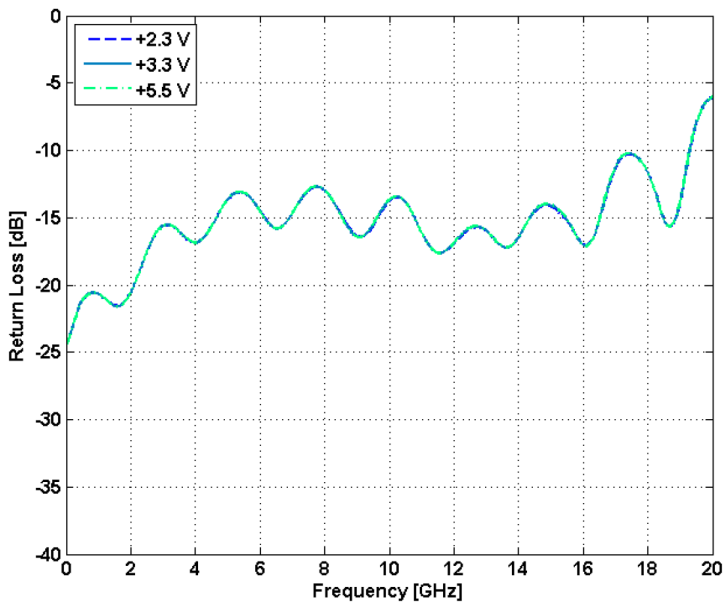


Figure 8. RFC port return loss vs. V_{DD}

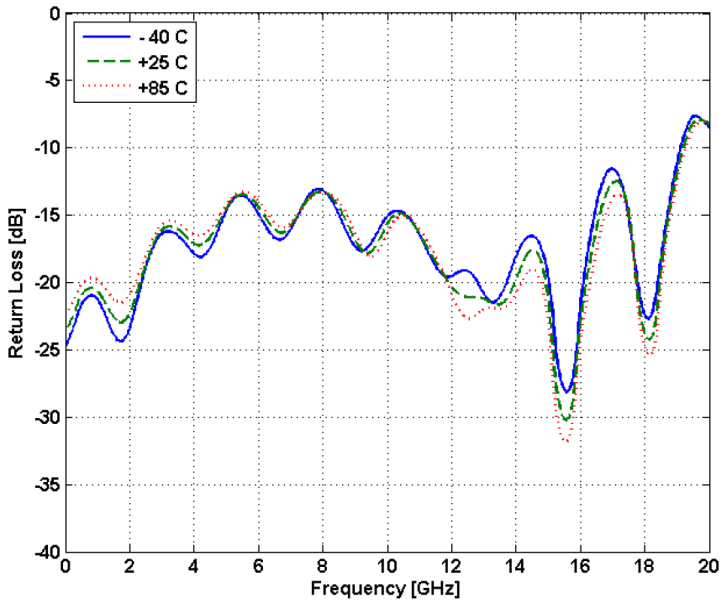


Figure 9. Active port return loss vs. temperature

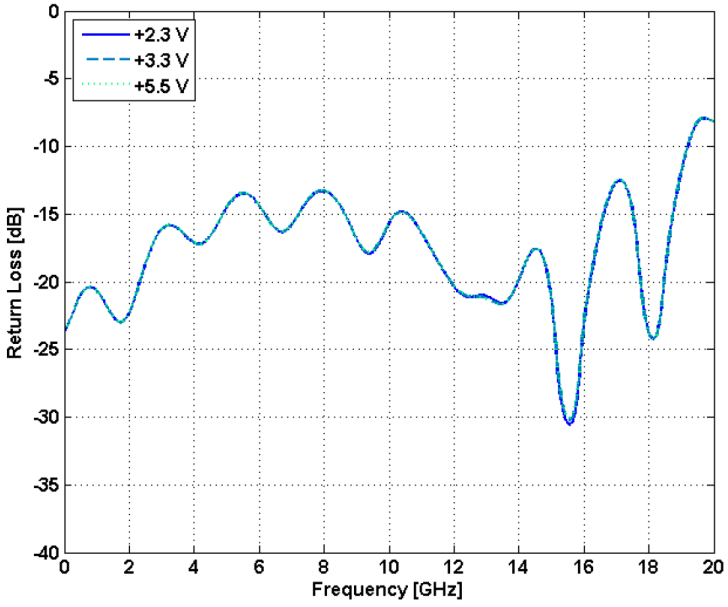


Figure 10. Active port return loss vs. V_{DD}

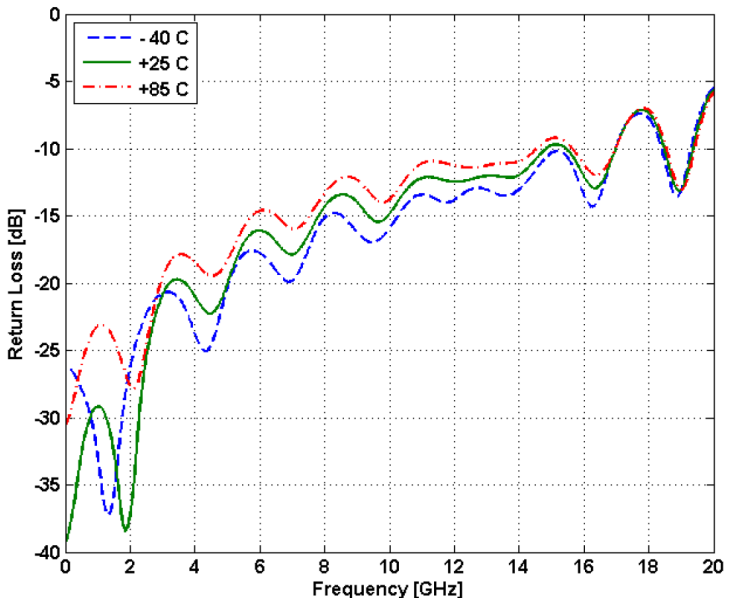


Figure 11. Terminated port return loss vs. temperature

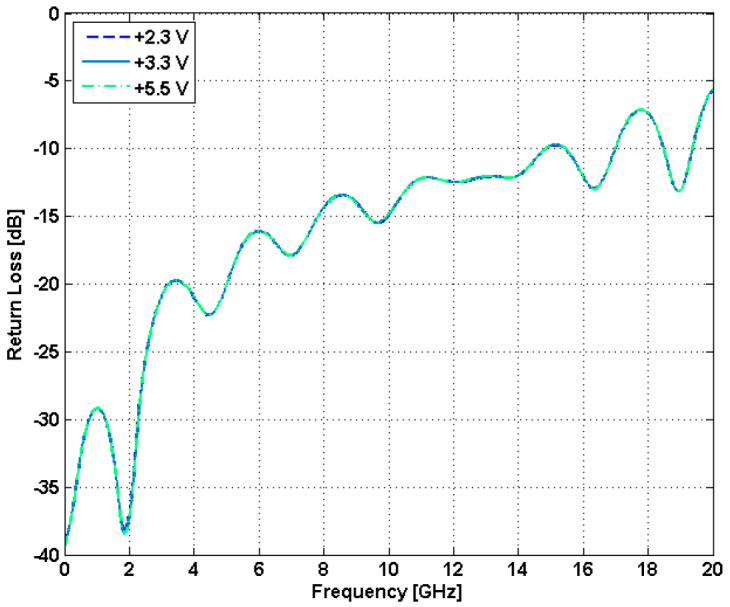


Figure 12. Terminated port return loss vs. V_{DD}

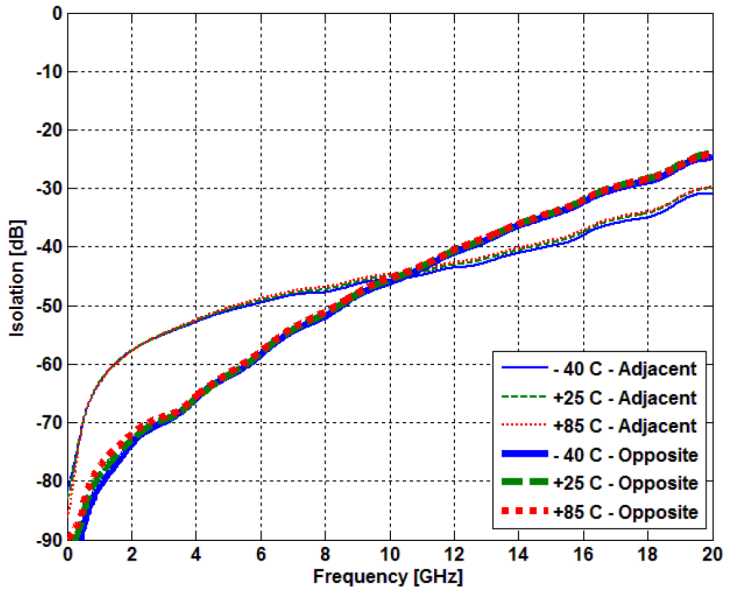


Figure 13. Isolation vs. temperature (RFx–RFx)(*)

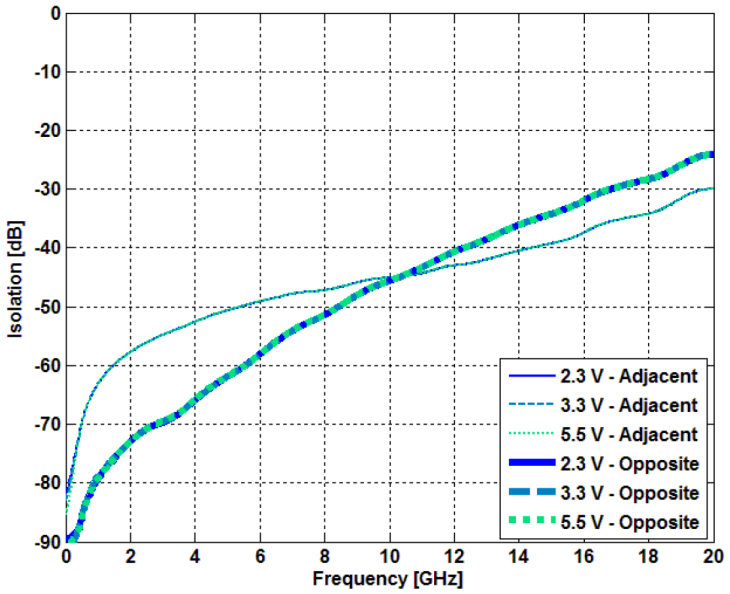


Figure 14. Isolation vs. V_{DD} (RFx–RFx)(*)

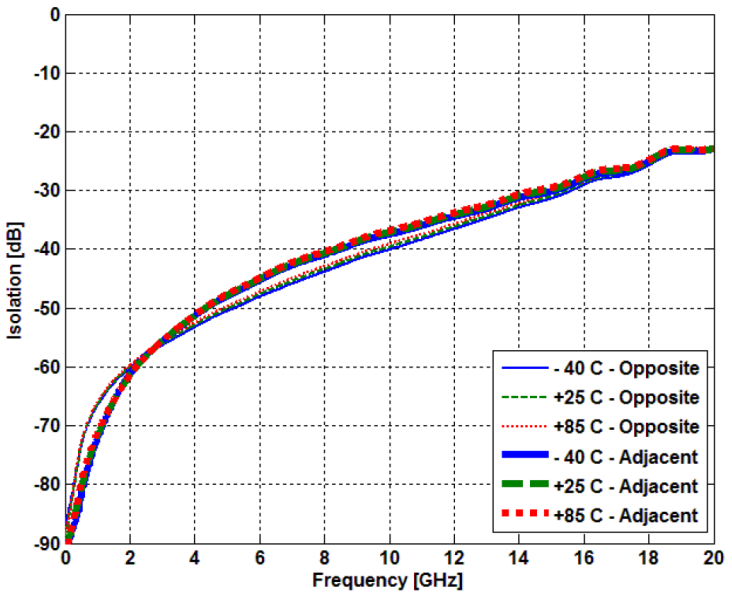


Figure 15. Isolation vs. temperature (RFC–RFx, RF1 or RF2 active)(*)

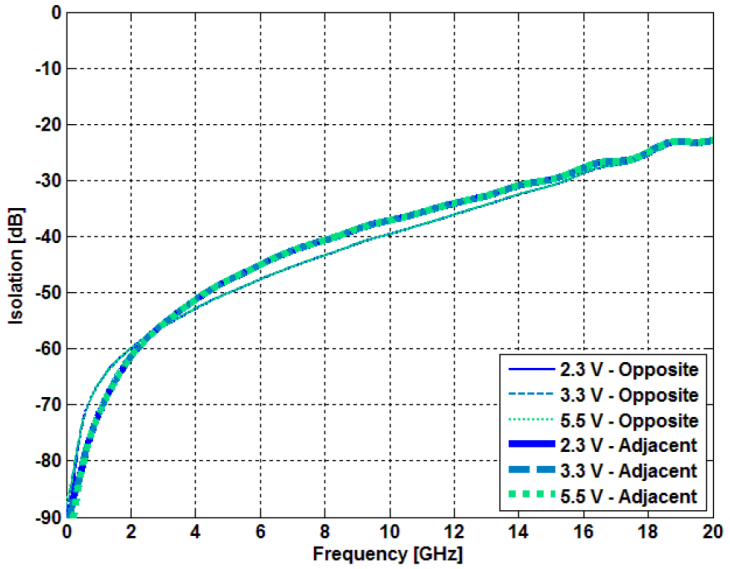


Figure 16. Isolation vs. V_{DD} (RFC–RFx, RF1 or RF2 active)(*)

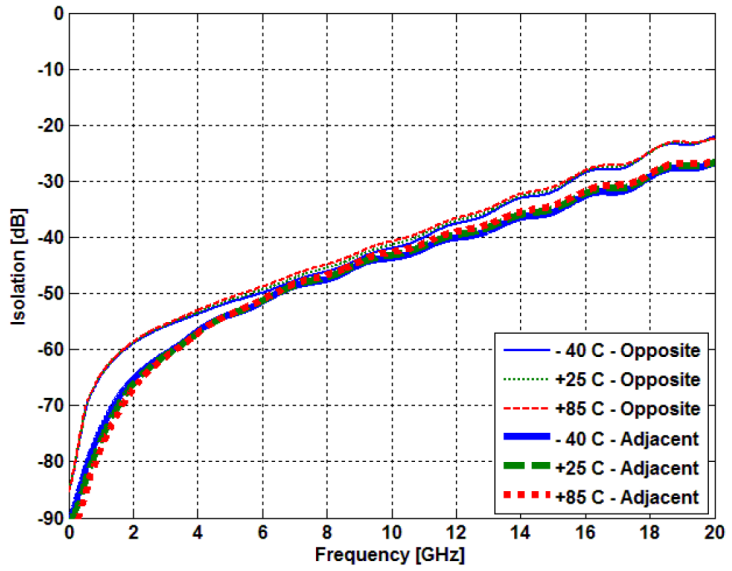


Figure 17. Isolation vs. temperature (RFC–RFx, RF3 or RF4 active)(*)

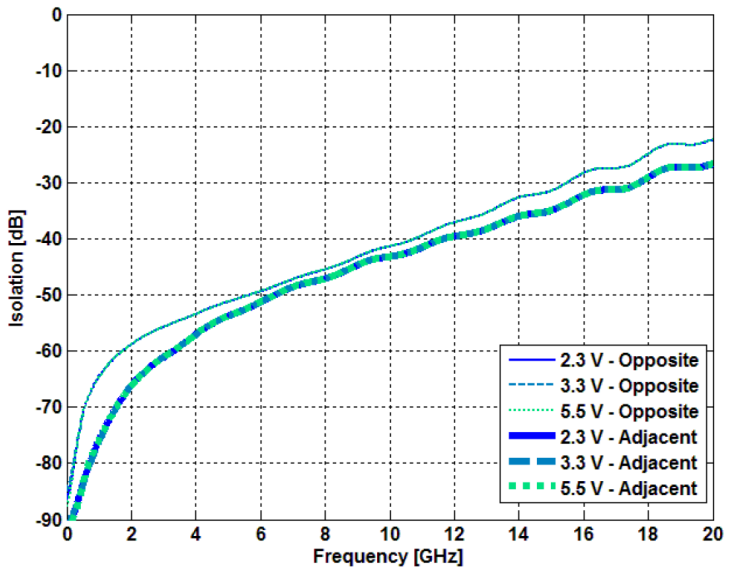


Figure 18. Isolation vs. V_{DD} (RFC–RFx, RF3 or RF4 active)(*)

* RF1 is adjacent to RF3, RF2 is adjacent to RF4, and RF1 and RF3 are opposite RF2 and RF4.

Evaluation kit

pSemi designed the SP4T switch evaluation board to help you evaluate the pSemi PE42542. The RF common port is connected through a 50Ω transmission line via the SMA connector, J1. The RF1, RF2, RF3, and RF4 ports connect through 50Ω transmission lines via SMA connectors J4, J3, J2, and J5, respectively. A 50Ω through transmission line is available via SMA connectors J6 and J7, which you can use to de-embed the loss of the PCB. J13 provides DC and digital inputs to the device.

The board is constructed of a four metal layer material with a total thickness of 62 mils. The top RF layer is Rogers 4360 material with a thickness of 32 mils and the εr = 6.4. The middle layers provide ground for the transmission lines. The transmission lines were designed using a coplanar waveguide with a ground plane model using a trace width of 18 mils, trace gaps of 7 mils and metal thickness of 2.1 mils.

To realize the true performance of the PE42542, design the PCB so that the RF transmission lines and sensitive DC I/O traces are heavily isolated from one another.

High frequency insertion loss and return loss can be further improved by external series inductive tuning traces in the customer application board layout. For example, to improve the 12–18 GHz performance, use ~180 pH for the RFx ports and ~50 pH for the RFC port.

pSemi recommends using vector de-embed to accurately calculate the device under test (DUT) performance. For more information, see Application Note 39, *Vector De-embedding of the PE42542 and PE42543 SP4T RF Switches*. To ease the vector de-embedding, download the Half Fixture Thru File from the pSemi website.

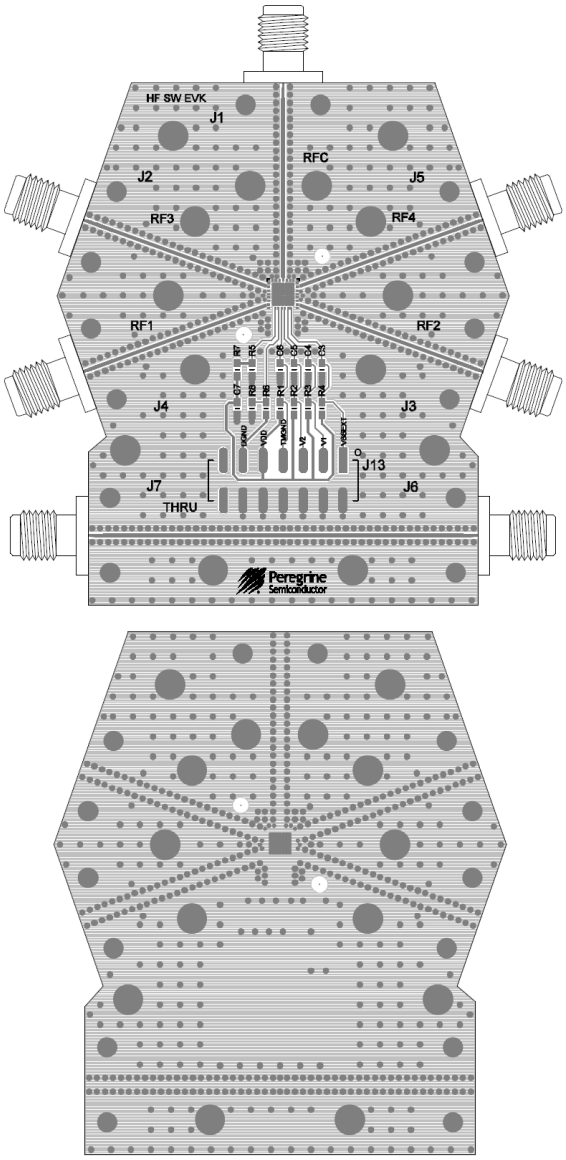
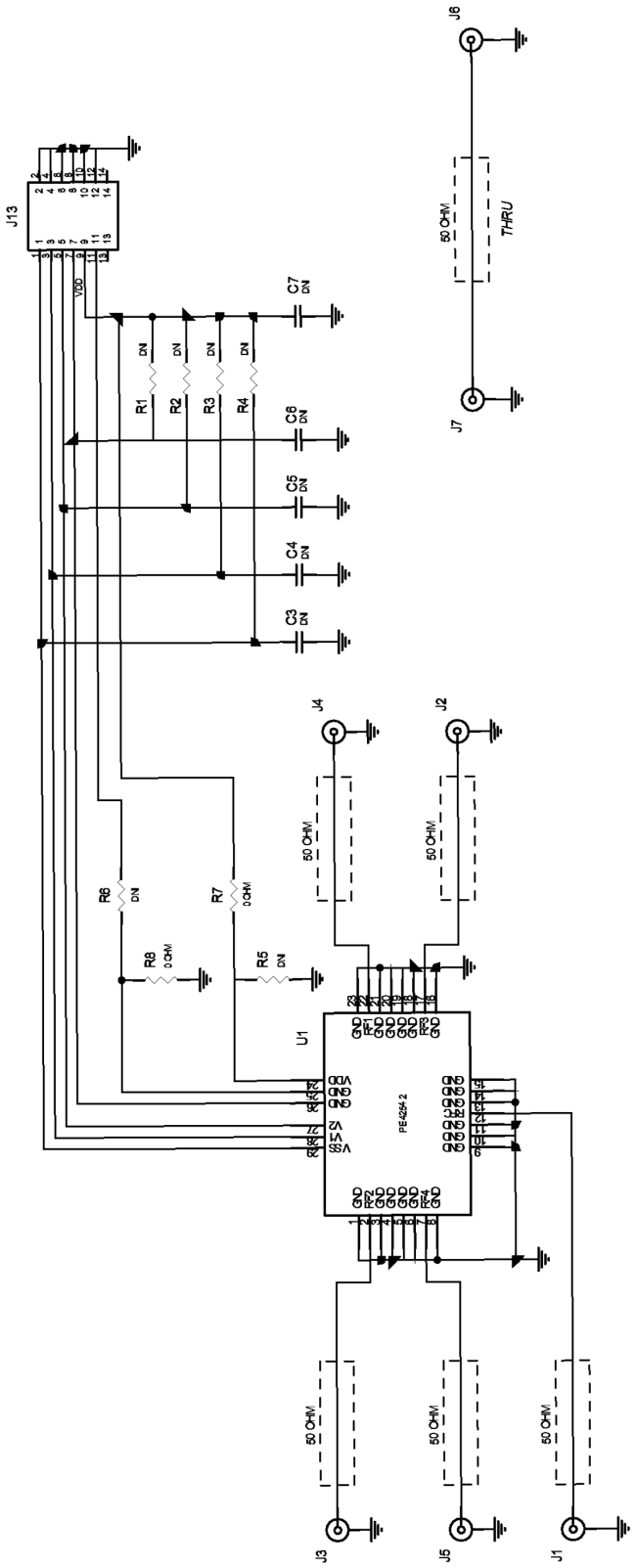


Figure 19. Evaluation board layout

Evaluation board schematic



CAUTION: Contains parts and assemblies susceptible to damage by electrostatic discharge (ESD).

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Figure 20. Evaluation board schematic

Pin information

Figure 21 shows the PE42542 pin map for the 29-lead 4 × 4 mm LGA package, and Table 4 lists the description for each pin.

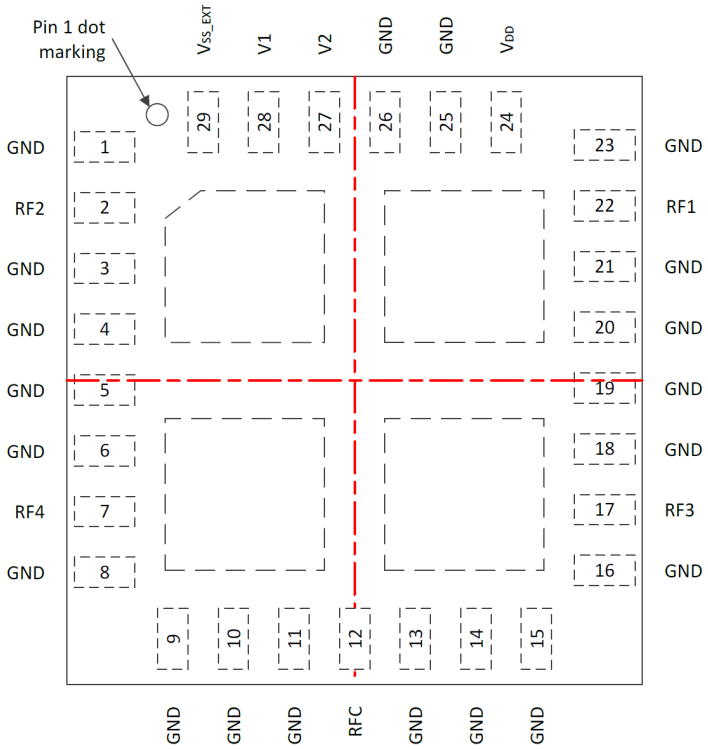


Figure 21. Pin configuration (top view)

Table 4. PE42542 pin descriptions

Pin no.	Pin name	Description
1, 3–6, 8–11, 13–16, 18–21, 23, 25, 26	GND	Ground
2(1)	RF2	RF port 2
7(1)	RF4	RF port 4
12(1)	RFC	RF common
17(1)	RF3	RF port 3
22(1)	RF1	RF port 1
24	V_{DD}	Supply voltage (nominal 3.3V)
27	V2	Digital control logic input 2
28	V1	Digital control logic input 1
29(2)	V_{SS_EXT}	External VSS negative voltage control
Pad	GND	Ground

1. RF pins 2, 7, 12, 17, and 22 must be at 0 VDC. These RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2. Use V_{SS_EXT} (pin 29) to bypass and disable the internal negative voltage generator. Connect V_{SS_EXT} (pin 29) to GND (V_{SS_EXT} = 0V) to enable the internal negative voltage generator.

Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE42542 moisture sensitivity level rating for the 29-lead 4 × 4 mm LGA package is MSL3.

Package drawing

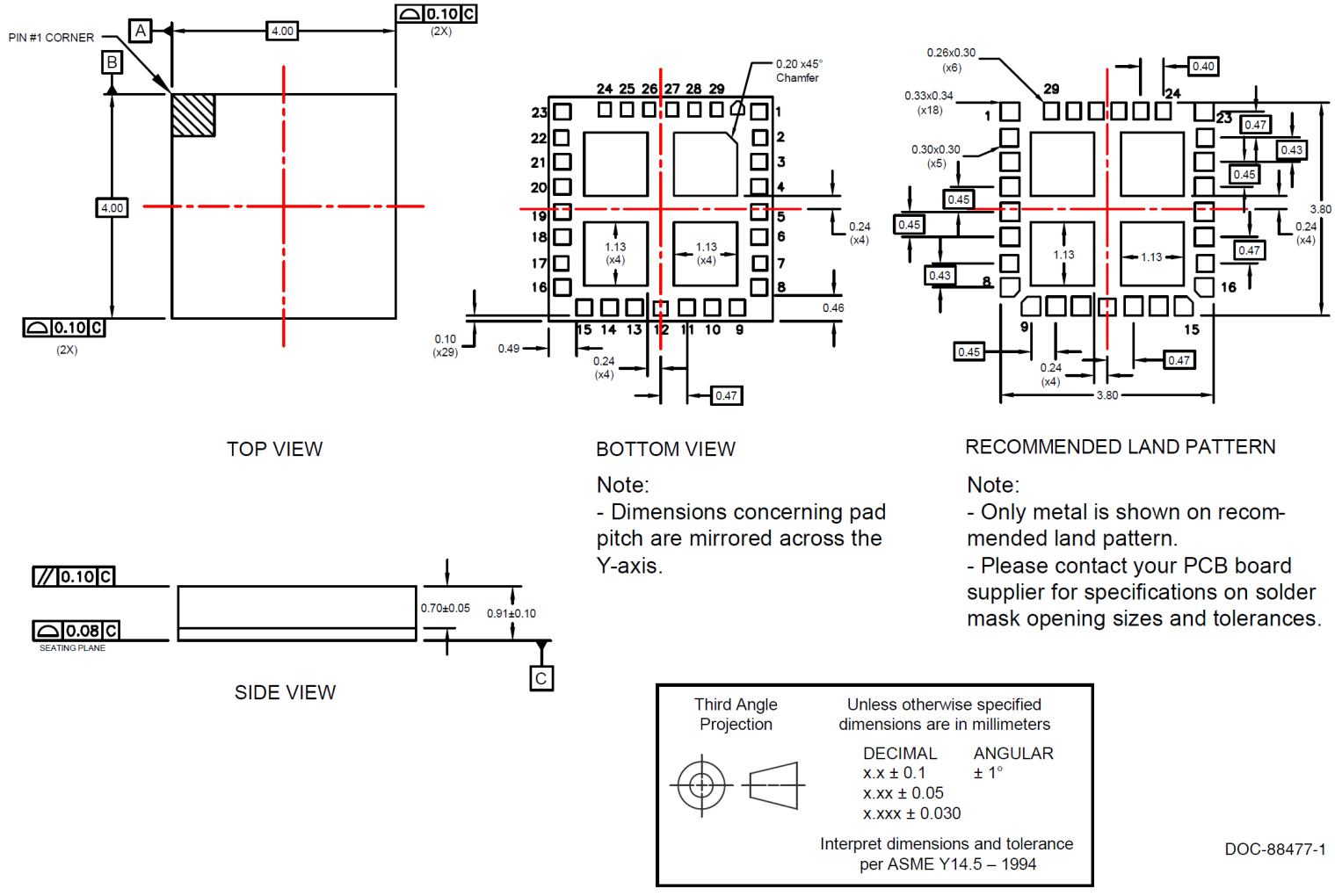
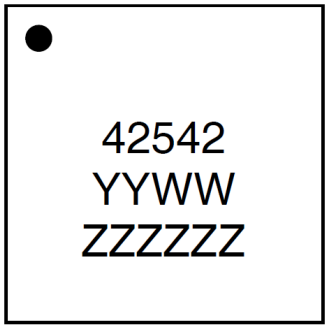


Figure 22. Package mechanical drawing for the 29-lead 4 × 4 mm LGA package

Top-marking specification



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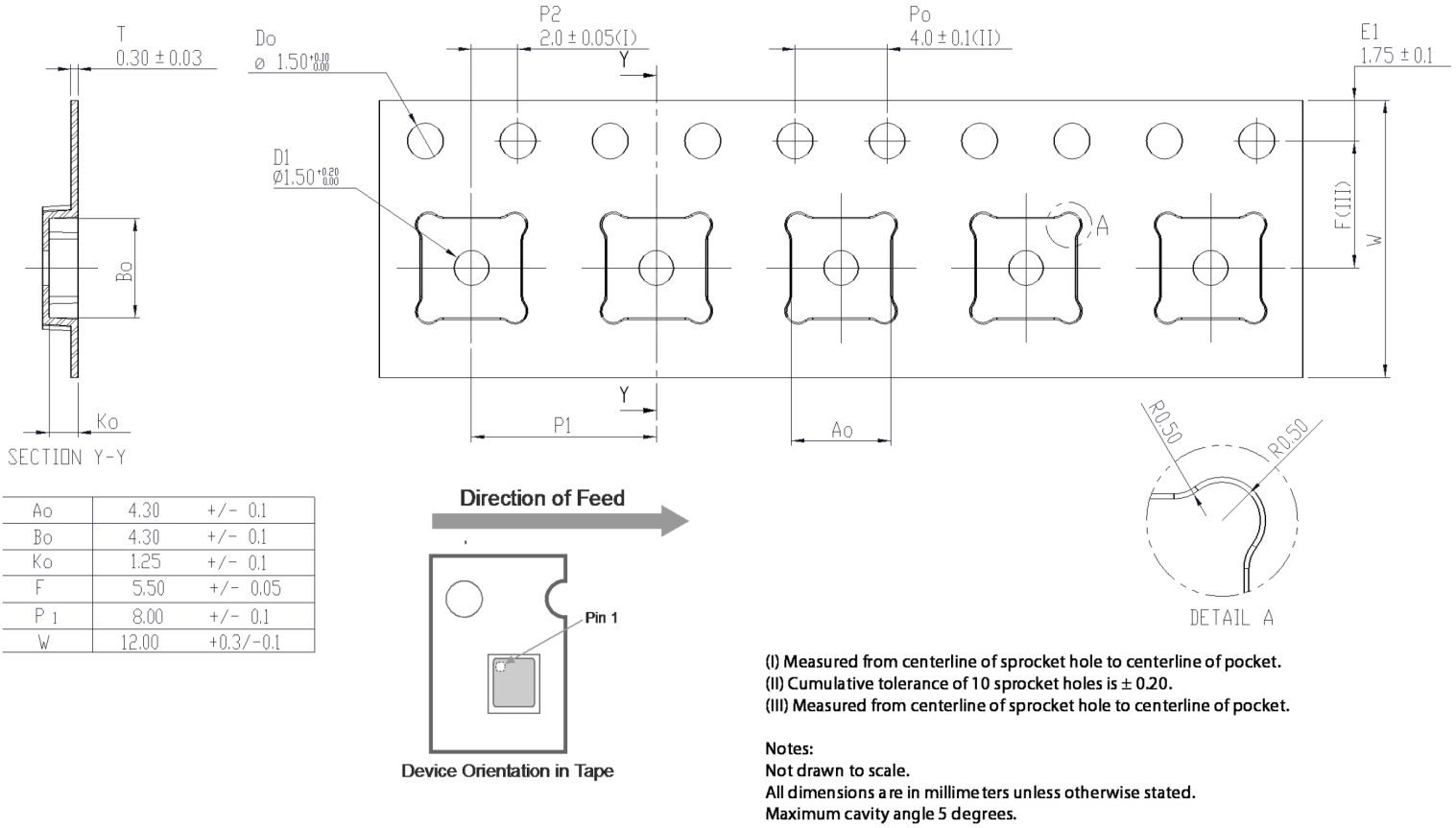
● = Pin 1 designator
YYWW = Date code, last two digits of assembly year and work week
ZZZZZZ = Last six characters of the assembly lot code

Figure 23. PE42542 package marking specification

Tape and reel specification



Ao	4.30	+/- 0.1
Bo	4.30	+/- 0.1
Ko	1.25	+/- 0.1
F	5.50	+/- 0.05
P 1	8.00	+/- 0.1
W	12.00	+0.3/-0.1

(I) Measured from centerline of sprocket hole to centerline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20.
(III) Measured from centerline of sprocket hole to centerline of pocket.

Notes:
Not drawn to scale.
All dimensions are in millimeters unless otherwise stated.
Maximum cavity angle 5 degrees.

Figure 24. Tape and reel specification for the 29-lead 4 × 4 mm LGA package

Ordering information

Order code	Description	Packaging	Shipping method
PE42542C-X	PE42542 SP4T RF switch	29-lead 4 × 4 mm LGA	500 units/T&R
EK42542-03	PE42542 evaluation kit	Evaluation kit	1/box

Document categories

Advance Information	The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
Preliminary Specification	The data sheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice to supply the best possible product.
Product Specification	The data sheet contains final data. In the event that pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).
Product Brief	This document contains a shortened version of the data sheet. For the full data sheet, contact sales@psemi.com.

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Patent statement	pSemi products are protected under one or more of the following U.S. patents: http://patents.psemi.com

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