PE42543

Product Specification

UltraCMOS® SP4T RF Switch, 9 kHz–18 GHz

Features

- HaRP™ technology-enhanced:
  - Fast settling time
  - No gate and phase lag
  - No drift in insertion loss or phase
- Fast switching time: 500 ns
- Low insertion loss:
  - 1.20 dB at 3 GHz
  - 2.30 dB at 13.5 GHz
  - 3.10 dB at 16 GHz
  - 4.10 dB at 18 GHz
- High isolation:
  - 55 dB at 3 GHz
  - 32 dB at 13.5 GHz
  - 28 dB at 16 GHz
  - 25 dB at 18 GHz
- ESD performance:
  - 2000V HBM on all pins
  - 150V MM on all pins
  - 250V CDM on all pins
- Packaging: 29-lead 4 × 4 mm LGA

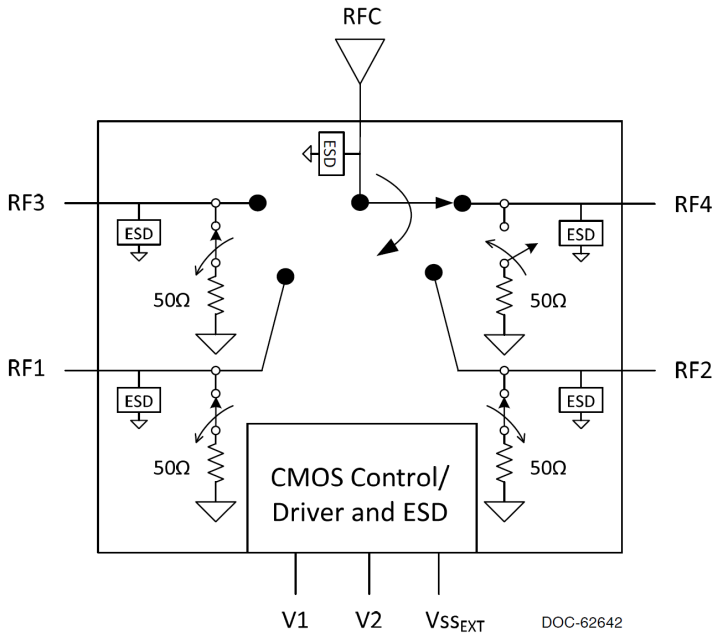

Figure 1. PE42543 functional diagram

Product description

The PE42543 is a HaRP™ technology-enhanced absorptive SP4T RF switch designed for use in test, automated test equipment (ATE), microwave, and other wireless applications. This broadband general-purpose switch is a pin-compatible version of the pSemi PE42542 with faster switching time and settling time. It exhibits low insertion loss, high isolation and linearity performance from 9 kHz through 18 GHz. No blocking capacitors are required if no DC voltage is present on the RF ports.

The PE42543 is manufactured using pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

pSemi's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

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Table 1. Absolute maximum ratings

Parameter or condition	Symbol	Min	Max	Unit
Maximum junction temperature	–	–	+150	°C
Storage temperature range	T_{ST}	-60	+150	°C
Supply voltage	V_{DD}	-0.3	5.5	V
Digital input voltage, V1 and V2	V_{CTRL}	-0.3	3.6	V
RF input power, CW (RFC–RFx):(1) - 9 kHz–27.5 MHz - ≥27.5 MHz–18 GHz	$P_{MAX,ABS}$	–	See Figure 2 33	dBm
RF input power, pulsed (RFC–RFx):(2) - 9 kHz–27.5 MHz - ≥27.5 MHz–18 GHz	$P_{MAX,PULSED}$	–	See Figure 2 34	dBm
RF input power into terminated ports, CW (RFx):(1) - 9 kHz–27.5 MHz - ≥27.5 MHz–18 GHz	$P_{MAX,TERM}$	–	See Figure 2 32	dBm
ESD voltage HBM, all pins(3)	$V_{ESD,HBM}$	–	2000	V
ESD voltage MM, all pins(4)	$V_{ESD,MM}$	–	150	V
ESD voltage CDM, all pins(5)	$V_{ESD,CDM}$	–	250	V

Notes:
1. 100% duty cycle, all bands, 50Ω
2. Pulsed, 5% duty cycle of 4620-µs period, 50Ω
3. Human Body Model (MIL_STD 883 Method 3015)
4. Machine Model (JEDEC JESD22-A115)
5. Charged Device Model (JEDEC JESD22-C101)

Recommended operating conditions

Table 2 lists the PE42543 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. Recommended operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Normal mode (V_{SS_EXT} = 0V)(1)					
Supply voltage	V_{DD}	2.3	–	5.5	V
Supply current	I_{DD}	–	120	200	µA
Bypass mode (V_{SS_EXT} = -3.4V)(2)					
Supply voltage (VDD ≥ 3.4V for Table 3 full specification compliance	V_{DD}	2.7	3.4	5.5	V
Supply current	I_{DD}	–	50	80	µA
Negative supply voltage	V_{SS_EXT}	-3.6	–	-3.2	V
Negative supply current	I_{SS}	-40	-16	–	µA
Normal or bypass mode					
Digital input high, V1 and V2	V_{IH}	1.17	–	3.6	V
Digital input low, V1 and V2	V_{IL}	-0.3	–	0.6	V
RF input power, CW (RFC–RFx):(3) - 9 kHz–27.5 MHz - ≥27.5 MHz–18 GHz	$P_{MAX,CW}$	–	–	See Figure 2 30	dBm
RF input power, pulsed (RFC–RFx):(4) - 9 kHz–27.5 MHz - ≥27.5 MHz–18 GHz	$P_{MAX,PULSED}$	–	–	See Figure 2 32	dBm
RF input power into terminated ports, CW (RFx):(3) - 9 kHz–27.5 MHz - ≥27.5 MHz–18 GHz	$P_{MAX,TERM}$	–	–	See Figure 2 20	dBm
Operating temperature range	T_{OP}	-40	+25	+85	°C

Notes:
1. Normal mode: Connect V_{SS_EXT} (pin 29) to GND (V_{SS_EXT} = 0V) to enable the internal negative voltage generator.
2. Bypass mode: Use V_{SS_EXT} (pin 29) to bypass and disable the internal negative voltage generator.
3. 100% duty cycle, all bands, 50Ω.
4. Pulsed, 5% duty cycle of 4620 µs period, 50Ω.

Electrical specifications

Table 3 lists the PE42543 key electrical specifications at +25 °C (Z_S = Z_L = 50Ω), unless otherwise specified.

- Normal mode: V_{DD} = 3.3V, V_{SS_EXT} = 0V. Connect V_{SS_EXT} (pin 29) to GND (V_{SS_EXT} = 0V) to enable the internal negative voltage generator.
- Bypass mode: V_{DD} =3.4V, V_{SS_EXT} = -3.4V. Use V_{SS_EXT} (pin 29) to bypass and disable the internal negative voltage generator.

Table 3. Electrical specifications

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency	–	–	9 KHz	–	18 GHz	As shown
Insertion loss	RFC–RFx	9 kHz–10 MHz 10–3000 MHz 3000–7500 MHz 7500–10000 MHz 10000–13500 MHz 13500–16000 MHz 16000–18000 MHz	–	0.70 1.20 1.65 2.10 2.30 3.10 4.10	0.85 1.50 2.05 2.55 2.80 3.60 4.70	dB
Isolation	RFx–RFx	9 kHz–10 MHz 10–3000 MHz 3000–7500 MHz 7500–10000 MHz 10000–13500 MHz 13500–16000 MHz 16000–18000 MHz	80 53 46 41 36 31 27	90 55 48 43 38 33 29	–	dB
Isolation	RFC–RFx	9 kHz–10 MHz 10–3000 MHz 3000–7500 MHz 7500–10000 MHz 10000–13500 MHz 13500–16000 MHz 16000–18000 MHz	78 54 41 36 31 27 24	90 55 42 38 32 28 25	–	dB
Return loss, active and common port	RFC–RFx	9 kHz–10 MHz 10–3000 MHz 3000–18000 MHz	–	22 15 14	–	dB
Return loss, terminated port	RFx	9 kHz–18000 MHz	–	14	–	dB
Input 0.1dB compression point(1)	RFC–RFx	–	–	See Figure 2	–	dBm
Input IP2	RFC–RFx	30–18000 MHz	–	113	–	dBm
Input IP3	RFC–RFx	30–18000 MHz	–	59	–	dBm
Settling time	–	50% CTRL to 0.05 dB of final value	–	2	3	µs
Switching time(2)	–	50% CTRL to 90% or 10% of final value	–	500	800	ns

Parameter	Path	Condition	Min	Typ	Max	Unit

Notes:
1. The input 0.1-dB compression point is a linearity figure of merit. For the maximum RF input power (P_{MAX}, 50Ω), see Table 2.
2. The PE42543 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (pin 29 = GND). The switching frequency describes the time duration between switching events. The switching time is the duration between the point that the control signal reaches 50% of the final value and the point that the output signal reaches within 10% or 90% of its target value.

Spurious performance

The PE42543 typical spurious performance is –150 dBm when V_{SS_EXT} = 0V (pin 29 = GND). To improve performance, disable the internal negative voltage generator by setting V_{SS_EXT} = –3.4V.

Optional external VSS control (V_{SS_EXT})

For proper operation, the V_{SS_EXT} control pin must be grounded or tied to the V_{SS} voltage specified in Table 2. When the V_{SS_EXT} control pin is grounded, the switch FETs are biased with an internal negative voltage generator. For applications that require the lowest possible spur performance, apply V_{SS_EXT} externally to bypass the internal negative voltage generator.

Hot-switching capability

The maximum hot switching capability of the PE42543 is 20 dBm from 18.8 MHz to 18 GHz. The maximum hot switching capability below 18.8 MHz does not exceed the maximum RF CW terminated power. See Figure 2. Hot switching occurs when RF power is applied while switching between the RF ports.

Control logic

Table 4. Truth table

State	V1	V2
RF1 on	0	0
RF2 on	1	0
RF3 on	0	1
RF4 on	1	1

Power derating curves

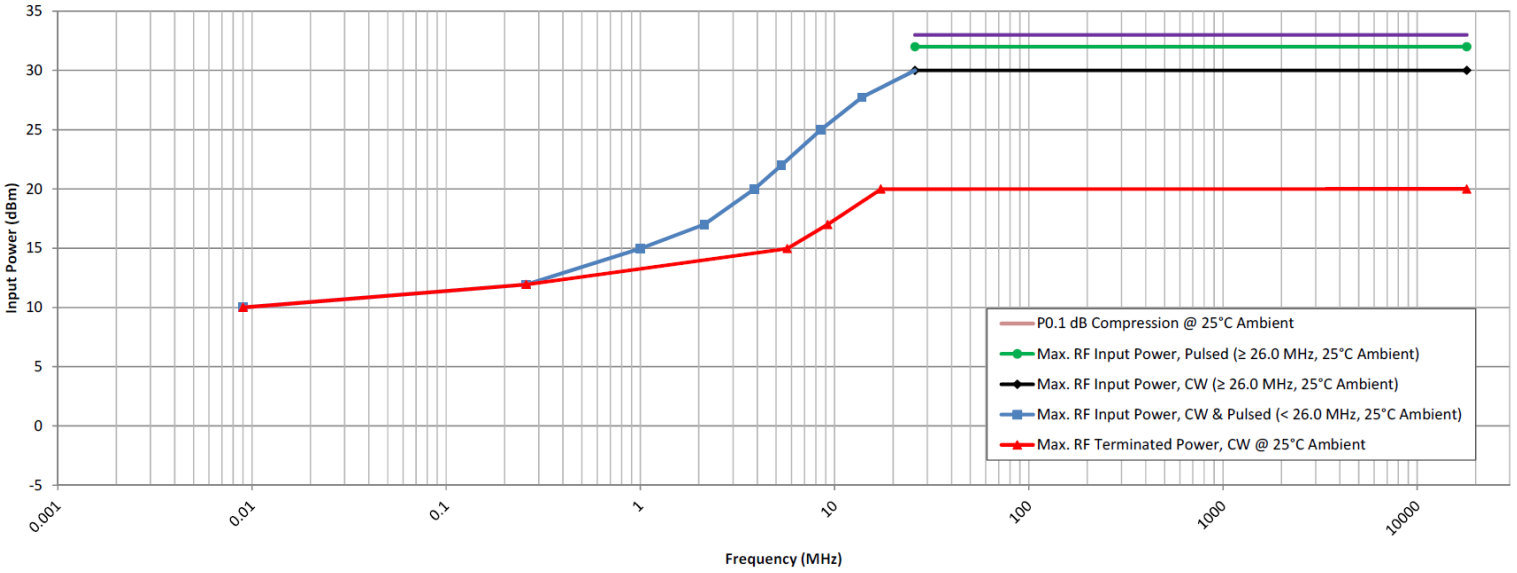


Figure 2. Power derating curve for 9 kHz–18 GHz @ 25°C ambient (50Ω)

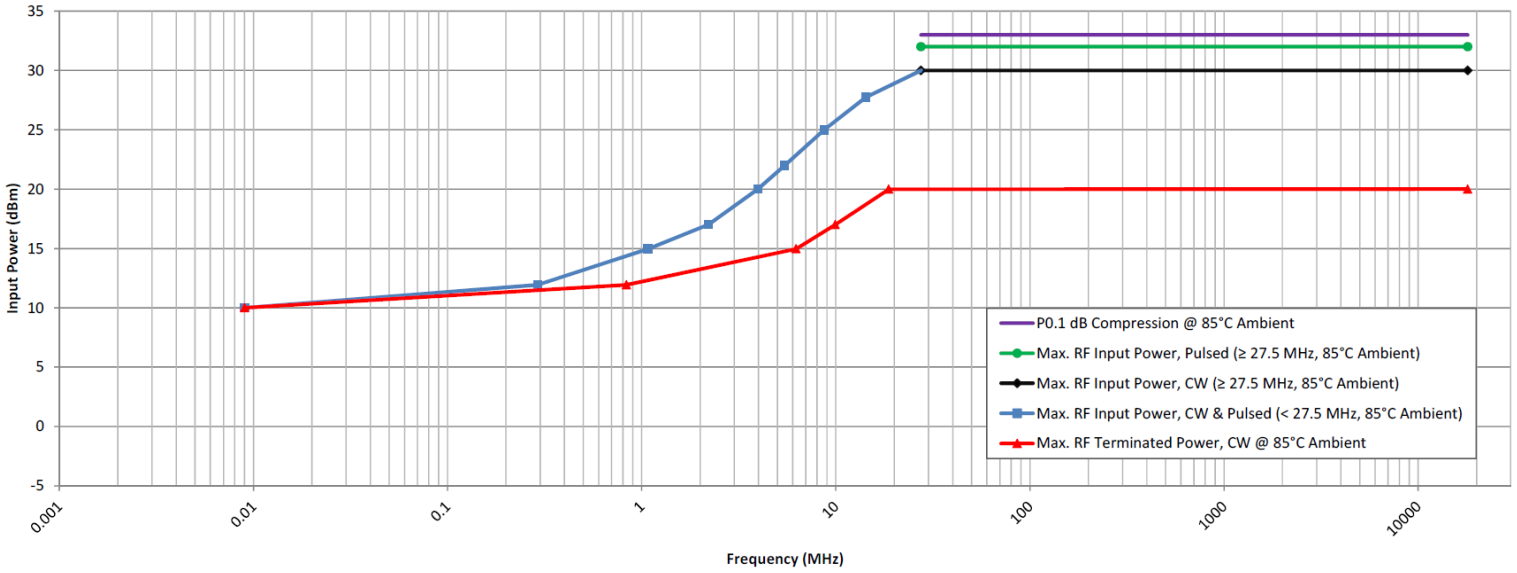


Figure 3. Power derating curve for 9 kHz–18 GHz @ 85°C ambient (50Ω)

Typical performance data

Figures 4–18 show the typical performance data at +25 °C and V_{DD} = 3.3V (Z_S = Z_L = 50Ω), unless otherwise specified.

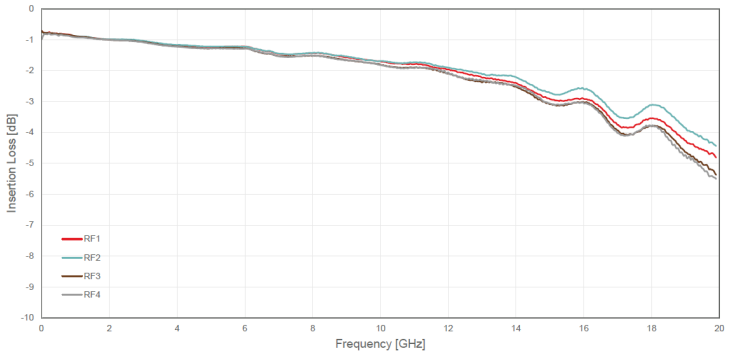


Figure 4. Insertion loss (RFC–RFx)

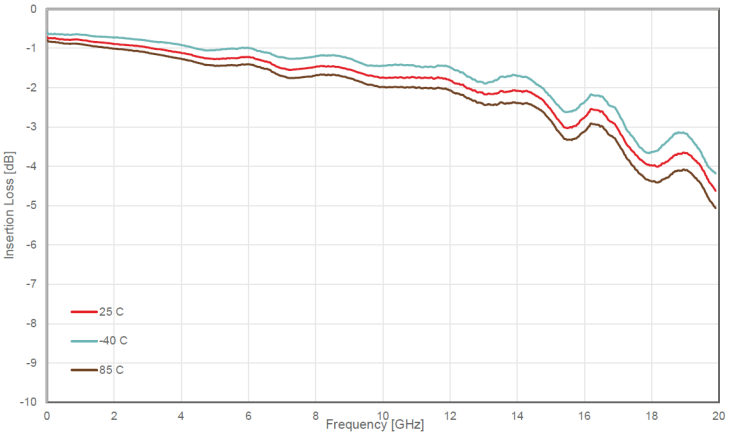


Figure 5. Insertion loss vs. temperature (RFC–RFx)

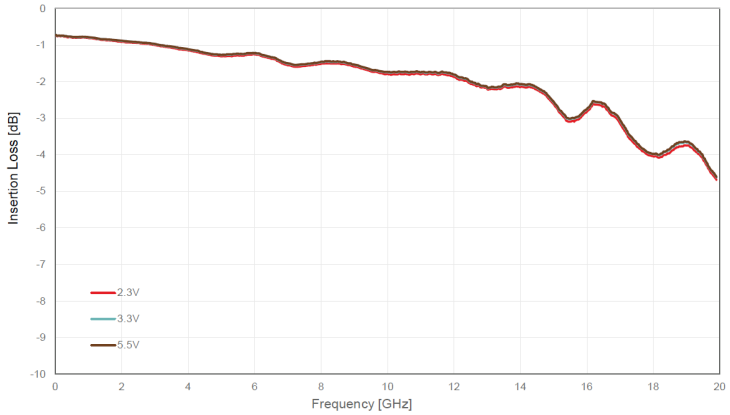


Figure 6. Insertion loss vs. V_{DD} (RFC–RFx)

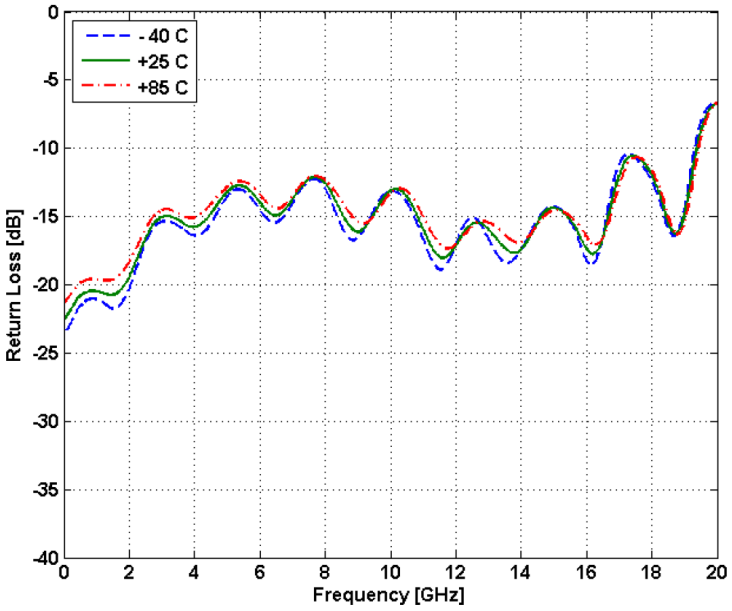


Figure 7. RFC port return loss vs. temperature

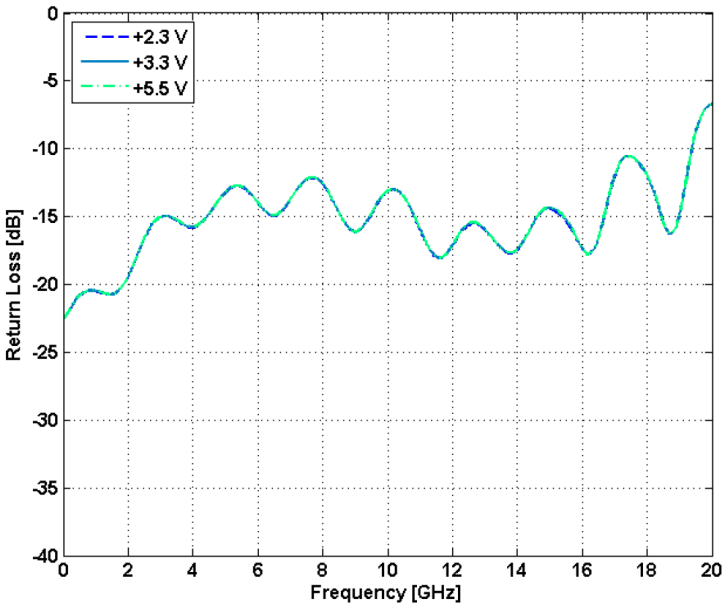


Figure 8. RFC port return loss vs. V_{DD}

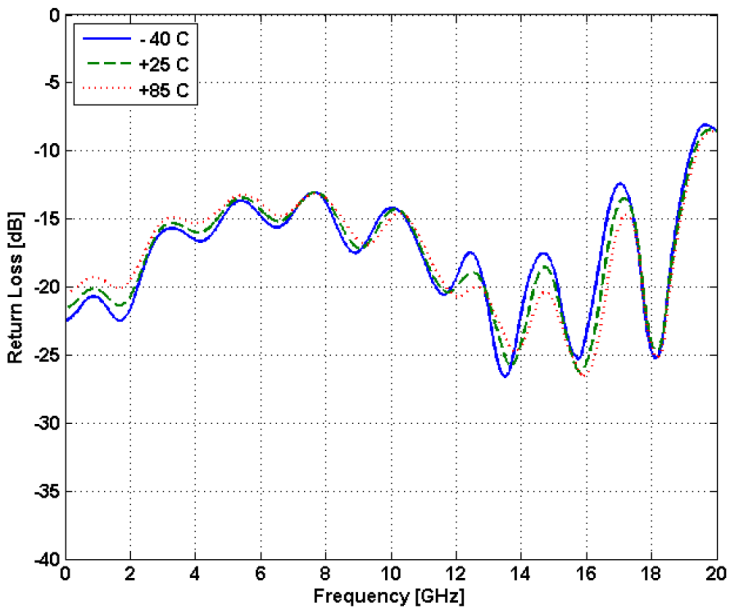


Figure 9. Active port return loss vs. temperature

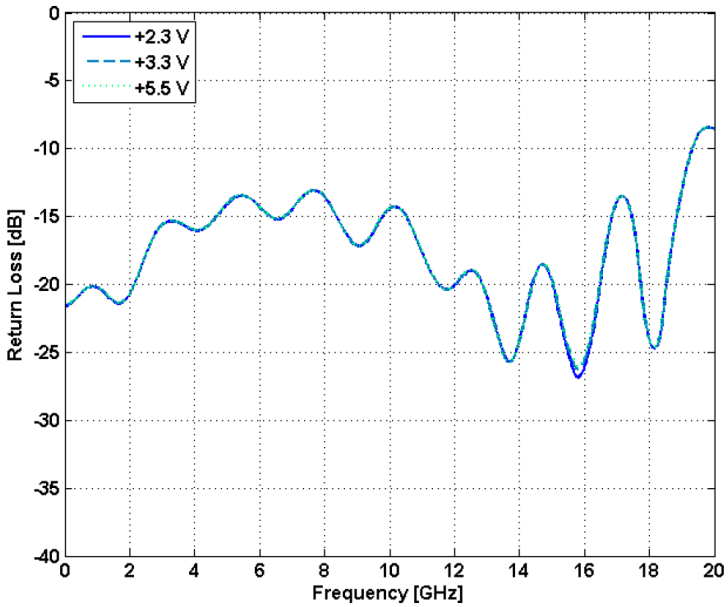


Figure 10. Active port return loss vs. V_{DD}

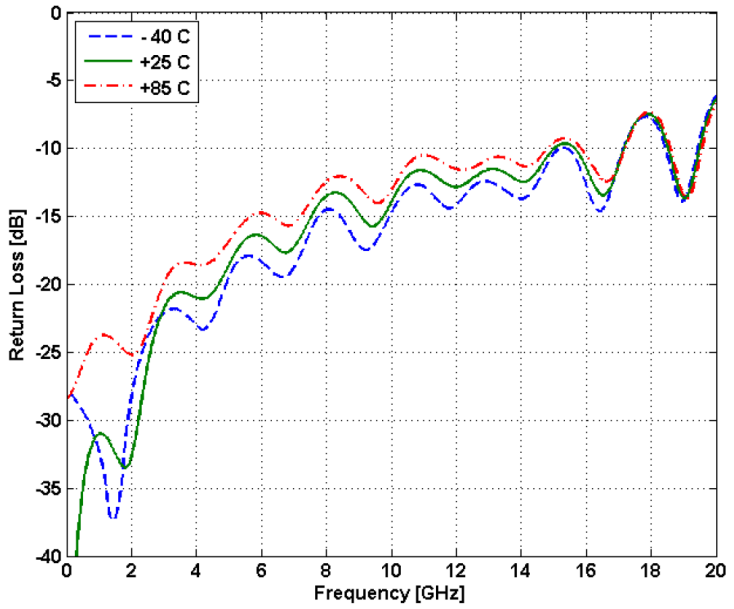


Figure 11. Terminated port return loss vs. temperature

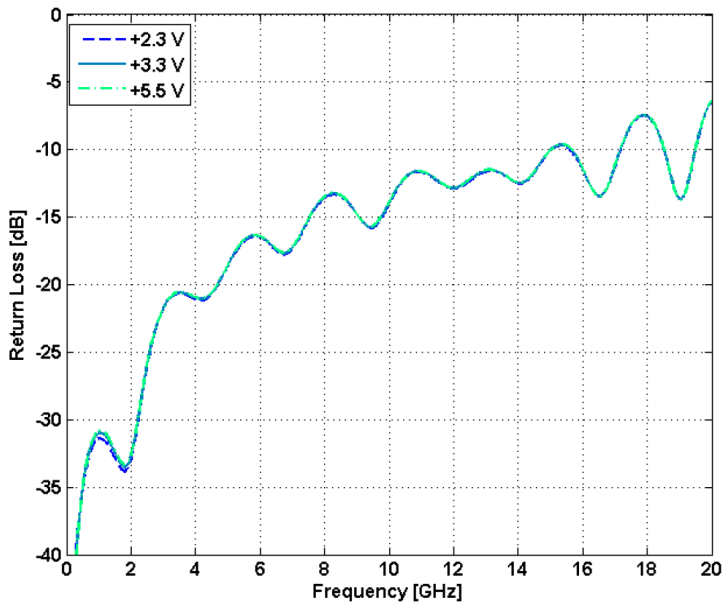


Figure 12. Terminated port return loss vs. V_{DD}

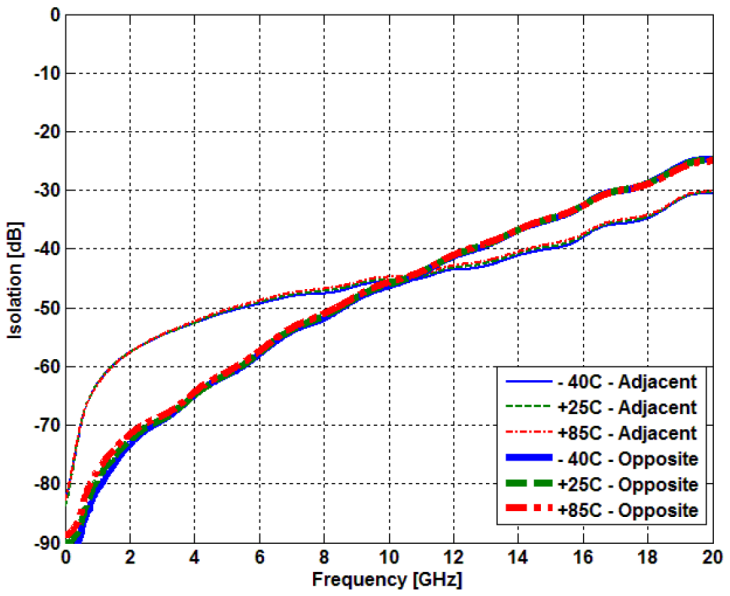


Figure 13. Isolation vs. temperature (RFx–RFx)(*)

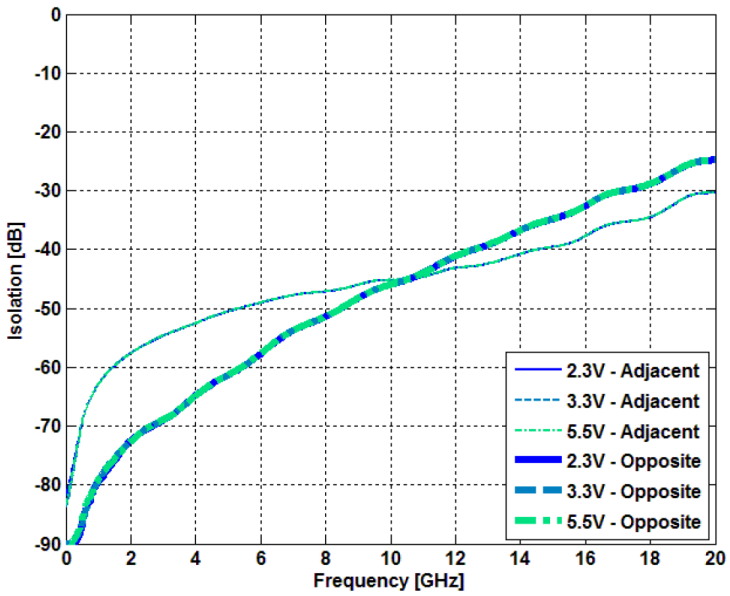


Figure 14. Isolation vs. V_{DD} (RFx–RFx)(*)

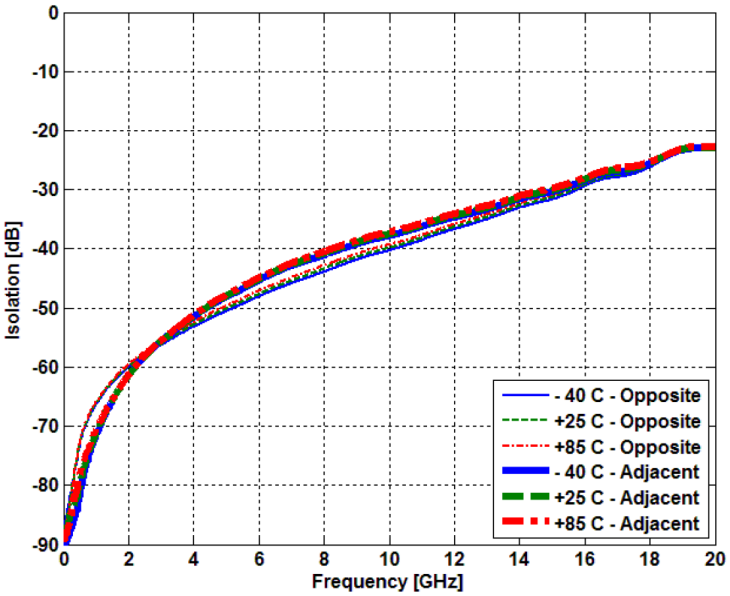


Figure 15. Isolation vs. temperature (RFC–RFx, RF1 or RF2 active)(*)

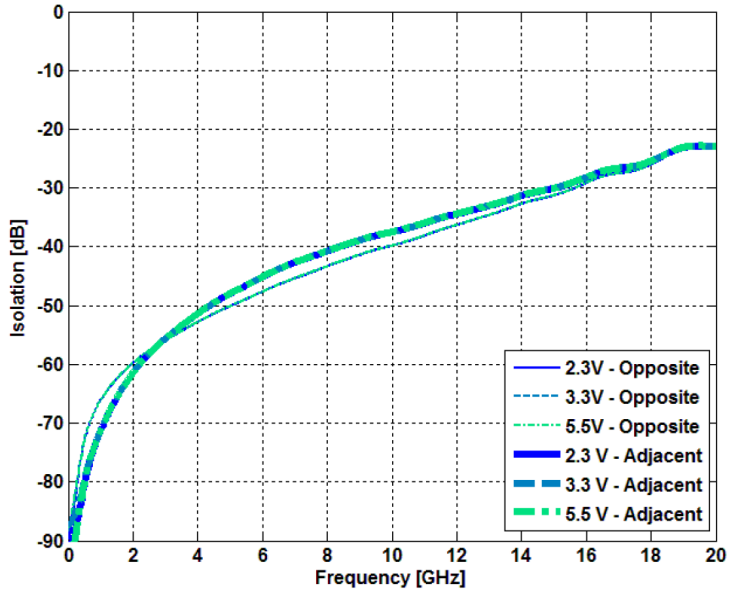


Figure 16. Isolation vs. V_{DD} (RFC–RFx, RF1 or RF2 active)(*)

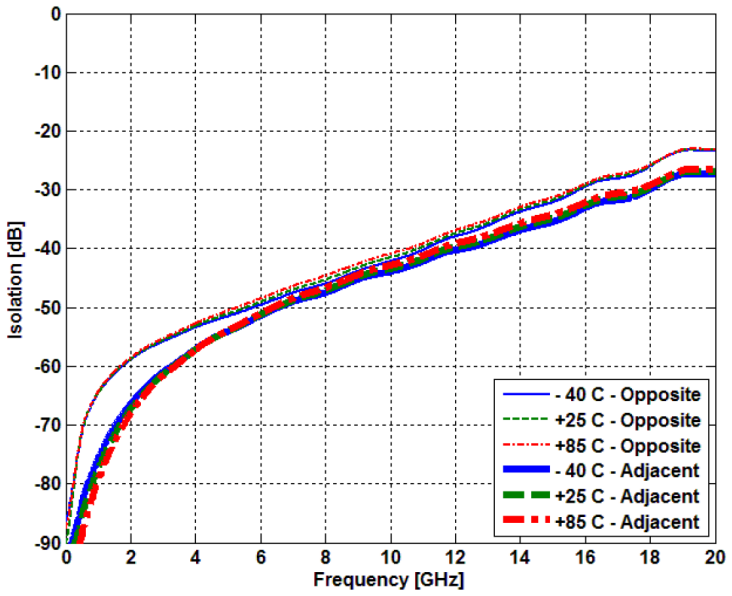


Figure 17. Isolation vs. temperature (RFC–RFx, RF3 or RF4 active)(*)

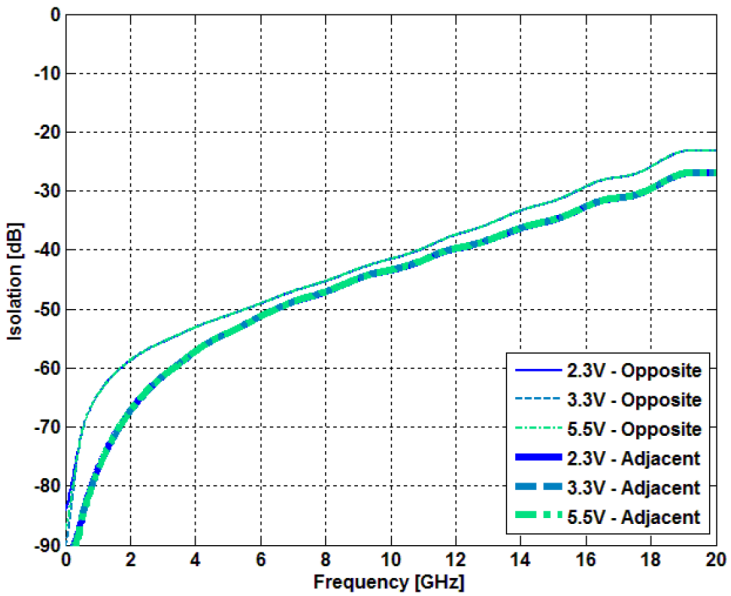


Figure 18. Isolation vs. V_{DD} (RFC–RFx, RF3 or RF4 active)(*)

Note: * RF1 is adjacent to RF3, RF2 is adjacent to RF4, and RF1 and RF3 are opposite RF2 and RF4.

Evaluation kit

pSemi designed the SP4T switch evaluation board to ease your evaluation of the pSemi PE42543. The RF common port connects through a 50Ω transmission line via SMA connector J1. Ports RF1, RF2, RF3, and RF4 connect through 50Ω transmission lines via SMA connectors J4, J3, J2, and J5, respectively. A 50Ω through transmission line is available via SMA connectors J6 and J7 to de-embed the loss of the PCB. J13 provides DC and digital inputs to the device.

The board is constructed of a four metal layer material with a total thickness of 62 mils. The top RF layer is Rogers 4360 material with a thickness of 32 mils and the er = 6.4. The middle layers provide ground for the transmission lines. The transmission lines were designed using a coplanar waveguide with a ground plane model using a trace width of 18 mils, trace gaps of 7 mils and metal thickness of 2.1 mils.

To realize the true performance of the PE42543, design the PCB so that the RF transmission lines and sensitive DC I/O traces are heavily isolated from one another.

To improve high-frequency insertion loss and return loss performance, add external series inductive tuning traces in your application board layout. For example, to improve 12–18 GHz performance, use ~180 pH for the RFx ports and ~50 pH for the RFC port.

To accurately calculate the performance of the DUT, pSemi recommends vector de-embed. For more information, see *Application Note 39: Vector De-embedding of the PE42542 and PE42543 SP4T RF Switches*. To ease the vector de-embedding, download the half thru line data file from the pSemi website.

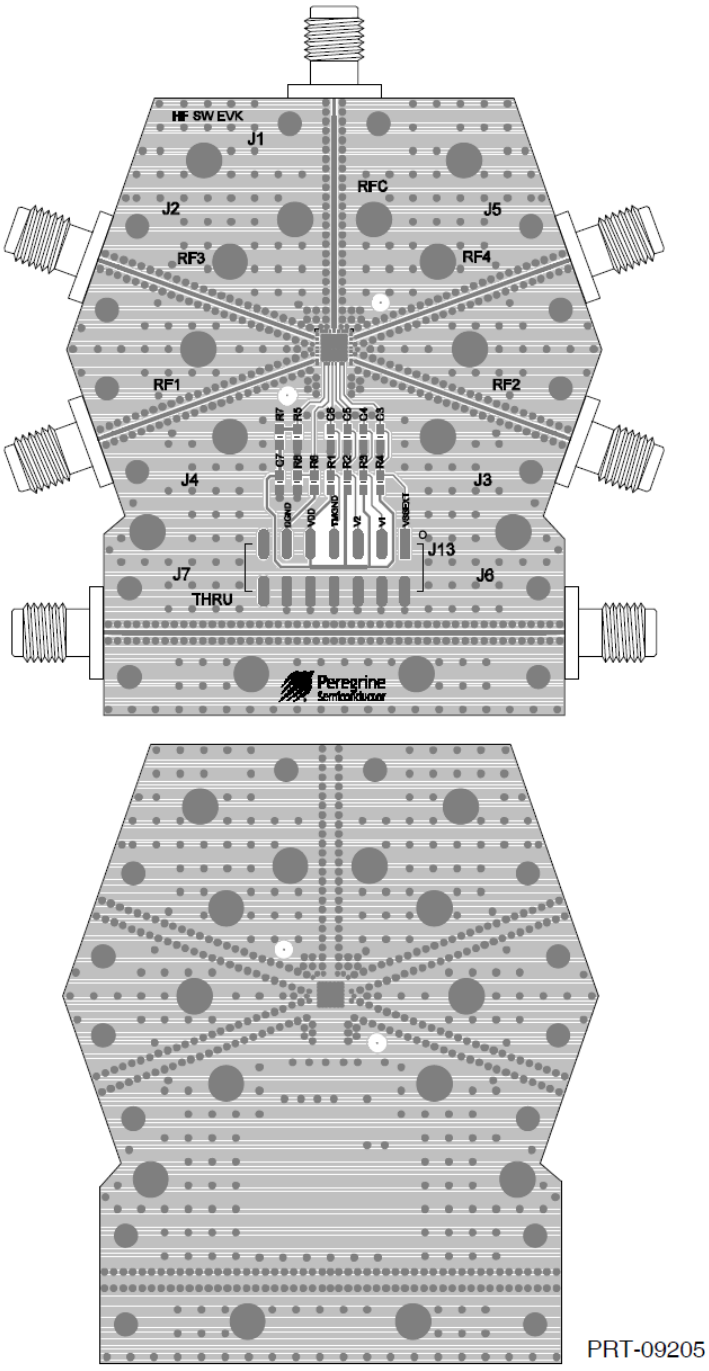


Figure 19. Evaluation board layout

Evaluation board schematic

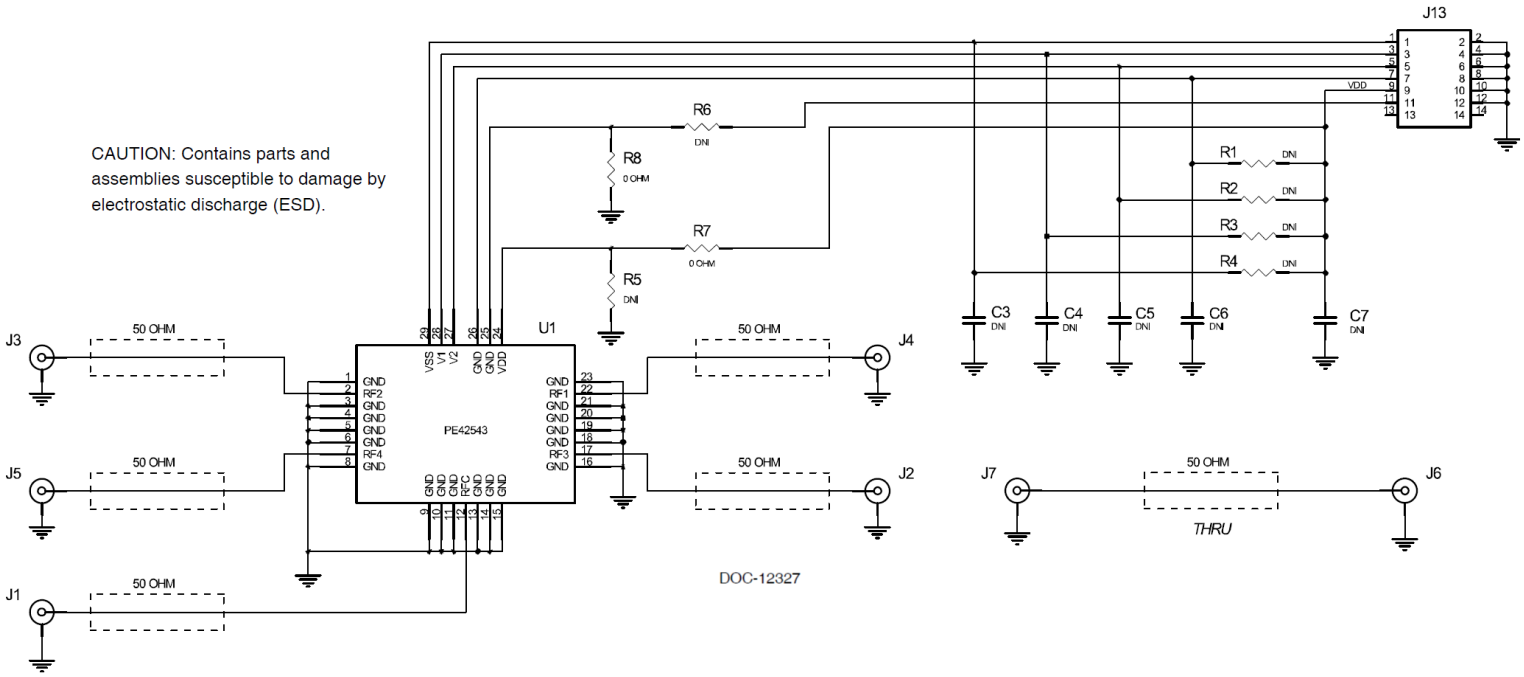


Figure 20. Evaluation board schematic

Pin configuration

Figure 21 shows the pin configuration for the 29-lead 4 × 4 mm LGA package, and Table 5 lists the description for each pin.

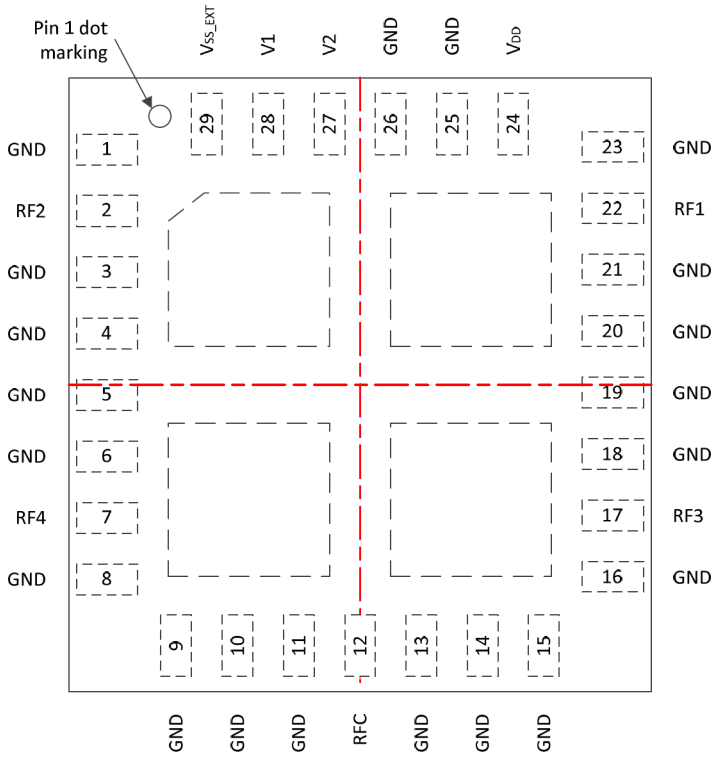


Figure 21. Pin configuration, top view

Table 5. Pin descriptions

Pin no.	Pin name	Description
1, 3–6, 8–11, 13–16, 18–21, 23	GND	Ground
2[1]	RF2	RF port 2
7[1]	RF4	RF port 4
12[1]	RFC	RF common
17[1]	RF3	RF port 3
22[1]	RF1	RF port 1
24	V_{DD}	Supply voltage (nominal 3.3V)
27	V2	Digital control logic input 2
28	V1	Digital control logic input 1
29[2]	V_{SS_EXT}	External V_{SS} negative voltage control
Pad	GND	Exposed pad. Ground for proper operation.

Notes:
1. RF pins 2, 7, 12, 17, and 22 must be at 0 VDC. These RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2. Use V_{SS_EXT} (pin 29) to bypass and disable the internal negative voltage generator. Connect V_{SS_EXT} (pin 29) to GND (V_{SS_EXT} = 0V) to enable the internal negative voltage generator.

Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE42543 moisture sensitivity level rating for the 29-lead 4 × 4 mm LGA package is MSL3.

Package drawing

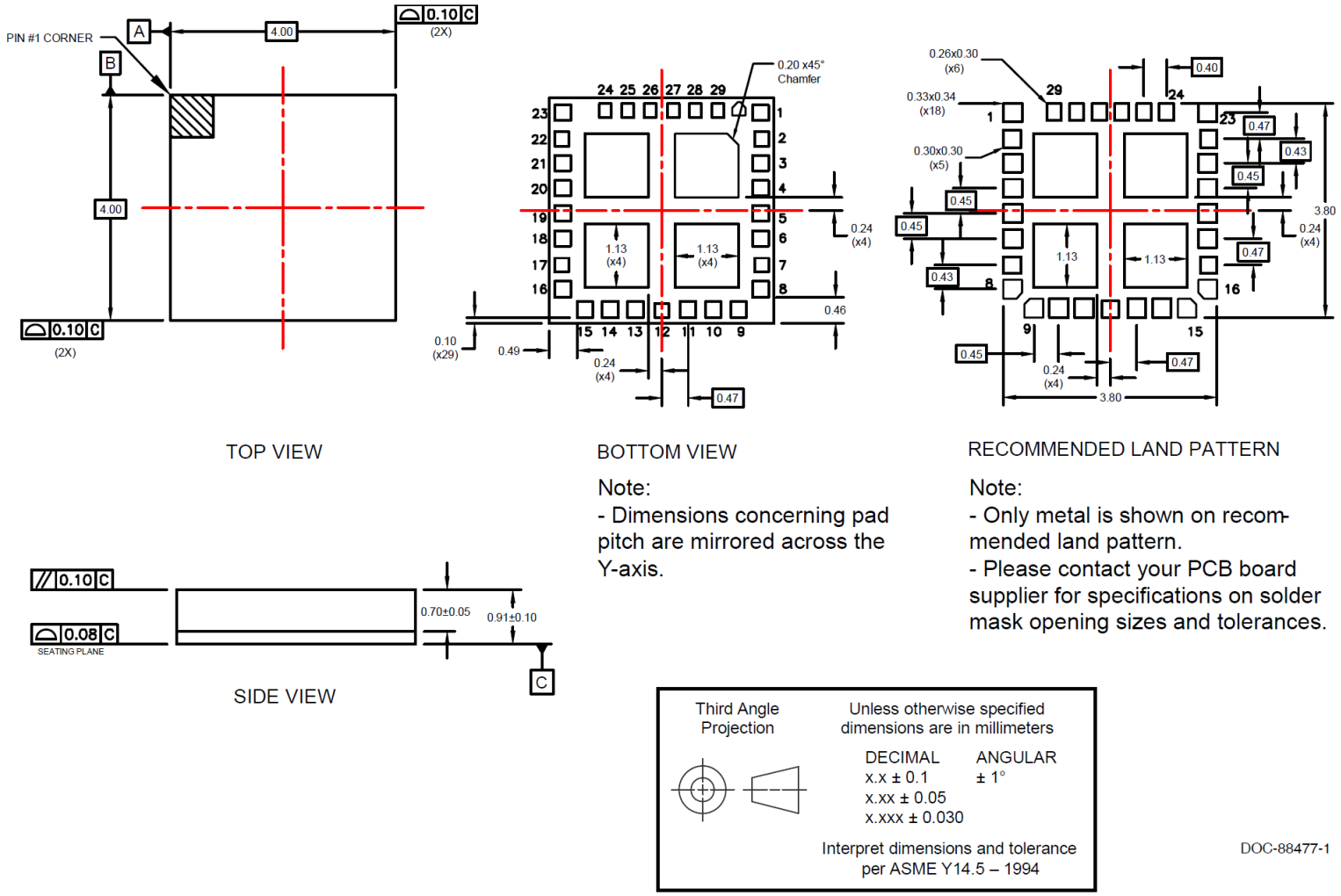


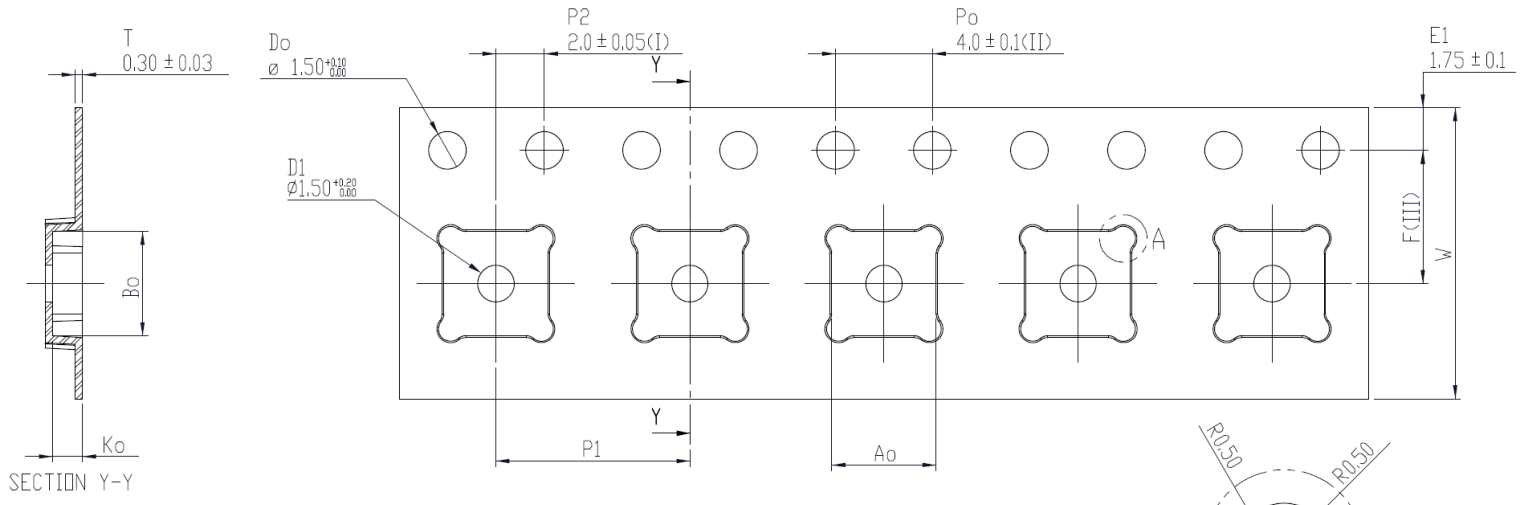
Figure 22. Package mechanical drawing for the 29-lead 4 × 4 mm LGA package

Top-marking specification

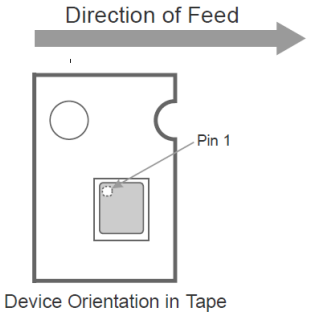
● = Pin 1 designator
YYWW = Date code, last two digits of assembly year and work week
ZZZZZZ = Last six characters of the assembly lot code

Figure 23. Package marking specification

Tape and reel specification



Ao	4.30	+/- 0.1
Bo	4.30	+/- 0.1
Ko	1.25	+/- 0.1
F	5.50	+/- 0.05
P 1	8.00	+/- 0.1
W	12.00	+0.3/-0.1



Device Orientation in Tape

(I) Measured from centerline of sprocket hole to centerline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20.
(III) Measured from centerline of sprocket hole to centerline of pocket.

Notes:
Not drawn to scale.
All dimensions are in millimeters unless otherwise stated.
Maximum cavity angle 5 degrees.

Figure 24. Tape and reel specification for the 29-lead 4 × 4 mm LGA package

Ordering information

Order code	Description	Packaging	Shipping method
PE42543C-X	PE42543 SP4T RF switch	Green 29-lead 4 × 4 mm LGA	500 units/T&R
EK42543-04	PE42543 evaluation kit	Evaluation kit	1/box

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