

ISO774x High-Speed, Robust-EMC Reinforced and Basic Quad-Channel Digital Isolators

1 Features

- 100Mbps data rate
- Robust isolation barrier:
 - >30-year projected lifetime at 1500V_{RMS} working voltage
 - Up to 5000V_{RMS} isolation rating
 - Up to 12.8kV surge capability
 - ±100kV/μs typical CMTI
- Wide supply range: 2.25V to 5.5V
- 2.25V to 5.5V level translation
- Default output *high* (ISO774x) and *low* (ISO774xF) options
- Wide temperature range: –55°C to 125°C
- Low power consumption, typical 1.5mA per channel at 1Mbps
- Low propagation delay: 10.7ns typical (5V Supplies)
- Robust electromagnetic compatibility (EMC)
 - System-level ESD, EFT, and surge immunity
 - ±8kV IEC 61000-4-2 contact discharge protection across isolation barrier
 - Low emissions
- Wide-SOIC (DW-16)and QSOP (DBQ-16) package options
 - For Ultra-wide package options, supporting >21.2mm Creepage, refer to [ISO7741U](#) and [ISO7742U](#)
 - For smaller, cost-optimized packages (up to 50% smaller for reinforced isolation), further improved noise immunity (up to 250kV/us CMTI) and higher data rate support (up to 150Mbps), refer to [ISO644x](#)
- Automotive version available: [ISO774x-Q1](#)
- Safety-related certifications:
 - DIN EN IEC 60747-17 (VDE 0884-17)
 - UL 1577 component recognition program
 - IEC 61010-1, IEC 62368-1, IEC 60601-1, and GB 4943.1 certifications

2 Applications

- [Energy storage systems](#)
- [Industrial automation](#)
- [Motor control](#)
- [Power supplies](#)
- [Solar inverters](#)
- [Medical equipment](#)

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE (NOM)
ISO7740 ISO7741 ISO7742	SOIC (DW)	10.30mm × 10.30mm	10.30mm × 7.50mm
	SSOP (DBQ)	4.90mm × 6.0mm	4.90mm × 3.90mm
ISO7741B	SOIC (DW)	10.30mm × 10.30mm	10.30mm × 7.50mm

(1) For more information, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

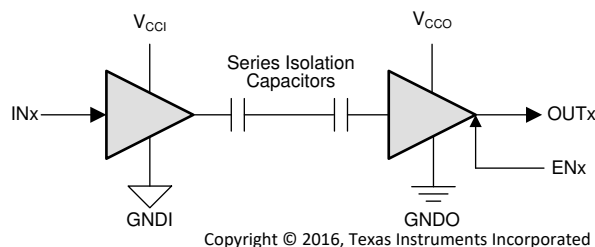


3 Description

The ISO774x devices are high-performance, quad-channel digital isolators with 5000V_{RMS} (DW package) and 3000V_{RMS} (DBQ package) isolation ratings per UL 1577. This family includes devices with reinforced insulation ratings according to VDE, CSA, TUV and CQC. The ISO7741B device is designed for applications that require basic insulation ratings only.

The ISO774x devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO₂) insulation barrier. These devices come with enable pins which can be used to put the respective outputs in high impedance for multi-controller driving applications and to reduce power consumption. The ISO7740 device has all four channels in the same direction, the ISO7741 device has three forward and one reverse-direction channels, and the ISO7742 device has two forward and two reverse-direction channels. If the input power or signal is lost, default output is *high* for devices without suffix F and *low* for devices with suffix F. See the [Device Functional Modes](#) section for further details.

Used in conjunction with isolated power supplies, these devices help prevent noise currents on data buses, such as RS-485, RS-232, and CAN, or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through remarkable chip design and layout techniques, electromagnetic compatibility of the ISO774x devices significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO774x devices are available in 16-pin SOIC and QSOP packages.



V_{CCI}=Input supply, V_{CCO}=Output supply
GNDI=Input ground, GNDO=Output ground

Simplified Schematic

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4 Pin Configuration and Functions

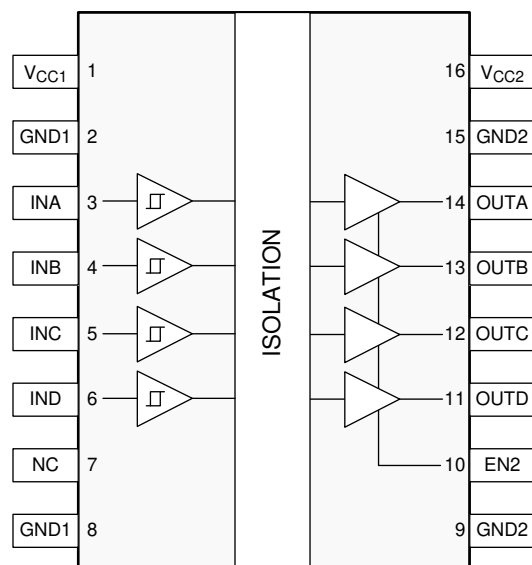


Figure 4-1. ISO7740 DW and DBQ Packages 16-Pin SOIC-WB and QSOP Top View

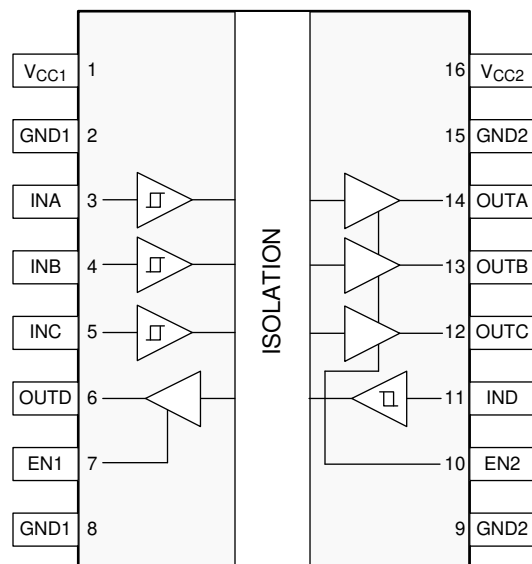


Figure 4-2. ISO7741 DW and DBQ Packages 16-Pin SOIC-WB and QSOP Top View

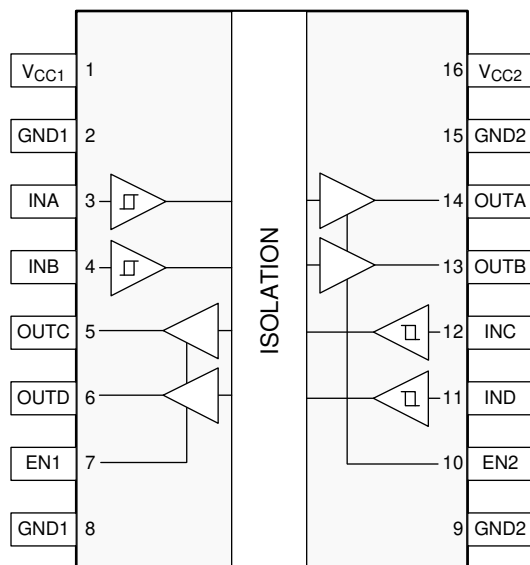


Figure 4-3. ISO7742 DW and DBQ Packages 16-Pin SOIC-WB and QSOP Top View

Table 4-1. Pin Functions

NAME	PIN			Type ⁽¹⁾	DESCRIPTION
	ISO7740	ISO7741	ISO7742		
EN1	—	7	7	I	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
EN2	10	10	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
GND1	2	2	2	—	Ground connection for V _{CC1}
	8	8	8		
GND2	9	9	9	—	Ground connection for V _{CC2}
	15	15	15		
INA	3	3	3	I	Input, channel A
INB	4	4	4	I	Input, channel B
INC	5	5	12	I	Input, channel C
IND	6	11	11	I	Input, channel D
NC	7	—	—	—	Not connected
OUTA	14	14	14	O	Output, channel A
OUTB	13	13	13	O	Output, channel B
OUTC	12	12	5	O	Output, channel C
OUTD	11	6	6	O	Output, channel D
V _{CC1}	1	1	1	—	Power supply, side 1
V _{CC2}	16	16	16	—	Power supply, side 2

5 Specifications

5.1 Absolute Maximum Ratings

See⁽¹⁾

		MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage ⁽²⁾	-0.5	6	V
V	Voltage at INx, OUTx, ENx	-0.5	$V_{CCX} + 0.5$ ⁽³⁾	V
I_O	Output current	-15	15	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
- (2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
- (3) Maximum voltage must not exceed 6 V.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±1500	
		Contact discharge per IEC 61000-4-2; Isolation barrier withstand test ^{(1) (2)}	±7000	

- (1) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
- (2) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _{CC1} , V _{CC2}	Supply Voltage		2.25		5.5	V
V _{CC(UVLO+)}	UVLO threshold when supply voltage is rising			2	2.25	V
V _{CC(UVLO-)}	UVLO threshold when supply voltage is falling		1.7	1.8		V
V _{HYS(UVLO)}	Supply voltage UVLO hysteresis		100	200		mV
I _{OH}	High level output current	V _{CCO} = 5 V ⁽¹⁾	-4			mA
		V _{CCO} = 3.3 V	-2			
		V _{CCO} = 2.5 V	-1			
I _{OL}	Low level output current	V _{CCO} = 5 V	4			mA
		V _{CCO} = 3.3 V	2			
		V _{CCO} = 2.5 V	1			
V _{IH}	High level Input voltage		0.7 x V _{CCI} ⁽¹⁾		V _{CCI}	V
V _{IL}	Low level Input voltage		0		0.3 x V _{CCI}	V
DR	Data Rate ⁽²⁾		50			Mbps
T _A	Ambient temperature		-55	25	125	°C

(1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} .

(2) 100 Mbps is the maximum specified data rate, although higher data rates are possible.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		ISO774x			UNIT
		DW (SOIC)	DUW (SSOP)	DBQ (QSOP)	
		16 PINS	16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	83.4	75.2	109	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	46	31.9	54.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	48	57.3	51.9	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	19.1	12.3	14.2	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	47.5	55.4	51.4	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO7740						
P _D	Maximum power dissipation (both sides)	V _{CC1} = V _{CC2} = 5.5 V, T _J = 150°C, C _L = 15 pF, Input a 50-MHz 50% duty cycle square wave			210	mW
P _{D1}	Maximum power dissipation (side-1)				45	mW
P _{D2}	Maximum power dissipation (side-2)				165	mW
ISO7741						
P _D	Maximum power dissipation (both sides)	V _{CC1} = V _{CC2} = 5.5 V, T _J = 150°C, C _L = 15 pF, Input a 50-MHz 50% duty cycle square wave			215	mW
P _{D1}	Maximum power dissipation (side-1)				75	mW
P _{D2}	Maximum power dissipation (side-2)				140	mW
ISO7742						
P _D	Maximum power dissipation (both sides)	V _{CC1} = V _{CC2} = 5.5 V, T _J = 150°C, C _L = 15 pF, Input a 50-MHz 50% duty cycle square wave			210	mW
P _{D1}	Maximum power dissipation (side-1)				105	mW
P _{D2}	Maximum power dissipation (side-2)				105	mW

5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE			UNIT	
			DW-16	DUW-16	DBQ-16		
CLR	External clearance ⁽¹⁾	Shortest terminal-to-terminal distance through air	>8	>21.2	>3.7	mm	
CPG	External creepage ⁽¹⁾	Shortest terminal-to-terminal distance across the package surface	>8	>21.2	>3.7	mm	
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	>17	>17	µm	
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	>600	>600	V	
	Material group	According to IEC 60664-1	I	I	I		
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V _{RMS}	I-IV	I-IV	I-III		
		Rated mains voltage ≤ 600 V _{RMS}	I-IV	I-IV	n/a		
		Rated mains voltage ≤ 1000 V _{RMS}	I-III	I-III	n/a		
DIN EN IEC 60747-17 (VDE 0884-17) ⁽²⁾							
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	ISO774x	2121	2121	566	V _{PK}
			ISO7741B	1414	n/a	n/a	V _{PK}
V _{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDb) Test; See Figure 8-7	ISO774x	1500	1500	400	V _{RMS}
			ISO7741B	1000	n/a	n/a	
		DC voltage	ISO774x	2121	2121	566	V _{DC}
			ISO7741B	1414	n/a	n/a	
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (qualification); V _{TEST} = 1.2 x V _{IOTM} , t = 1 s (100% production)	8000	8000	4242	V _{PK}	
V _{IMP}	Maximum impulse voltage ⁽³⁾	Tested in air, 1.2/50-µs waveform per IEC 62368-1	ISO774x	8000	10000	5000	V _{PK}
			ISO7741B	6000	n/a	n/a	
V _{IOSM}	Maximum surge isolation voltage ⁽⁴⁾	V _{IOSM} ≥ 1.3 x V _{IMP} ; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	ISO774x	12800	13000	10000	V _{PK}
			ISO7741B	7800	n/a	n/a	
q _{pd}	Apparent charge ⁽⁵⁾	Method a, After Input-output safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 x V _{IORM} , t _m = 10 s	≤5	≤5	≤5	pC	
		Method a, After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.6 x V _{IORM} , t _m = 10 s (ISO774x) V _{pd(m)} = 1.3 x V _{IORM} , t _m = 10 s (ISO7741B)	≤5	≤5	≤5		
			Method b: At routine test (100% production) and preconditioning (type test); V _{ini} = 1.2 x V _{IOTM} , t _{ini} = 1 s; V _{pd(m)} = 1.875 x V _{IORM} (ISO774x) or V _{pd(m)} = 1.5 x V _{IORM} (ISO7741B), t _m = 1 s (method b1) or V _{pd(m)} = V _{ini} , t _m = t _{ini} (method b2)	≤5	≤5		≤5
C _{IO}	Barrier capacitance, input to output ⁽⁶⁾	V _{IO} = 0.4 x sin (2πft), f = 1 MHz	≅1	≅1	≅1	pF	
R _{IO}	Isolation resistance ⁽⁶⁾	V _{IO} = 500 V, T _A = 25°C	>10 ¹²	>10 ¹²	>10 ¹²	Ω	
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	>10 ¹¹	>10 ¹¹	>10 ¹¹		
		V _{IO} = 500 V at T _S = 150°C	>10 ⁹	>10 ⁹	>10 ⁹		
	Pollution degree		2	2	2		
	Climatic category		55/125/21	55/12/5/21	55/125/21		
UL 1577							

PARAMETER		TEST CONDITIONS		VALUE			UNIT
				DW-16	DUW-16	DBQ-16	
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, $t = 60$ s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, $t = 1$ s (100% production)		5000	5700	3000	V_{RMS}

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package.
- (4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (6) All pins on each side of the barrier tied together creating a two-terminal device.

5.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 62368-1 and IEC 60601-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1	Certified according to EN 61010-1 and EN 62368-1
Reinforced certificate: 40040142 Basic certificate: 40047657	Master contract number: 220991	File number: E181974	Certificate numbers: CQC21001304083 (DW-16) CQC18001199097 (DBQ-16)	Client ID number: 77311

5.8 Safety Limiting Values

Safety limiting⁽¹⁾ intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I _S	Safety input, output, or supply current	R _{θJA} = 83.4°C/W, V _I = 5.5 V, T _J = 150°C, T _A = 25°C, see Figure 5-1			273	mA
		R _{θJA} = 83.4°C/W, V _I = 3.6 V, T _J = 150°C, T _A = 25°C, see Figure 5-1			416	
		R _{θJA} = 83.4°C/W, V _I = 2.75 V, T _J = 150°C, T _A = 25°C, see Figure 5-1			545	
P _S	Safety input, output, or total power	R _{θJA} = 83.4°C/W, T _J = 150°C, T _A = 25°C, see Figure 5-3			1499	mW
T _S	Maximum safety temperature				150	°C
DBQ-16 PACKAGE						
I _S	Safety input, output, or supply current	R _{θJA} = 109°C/W, V _I = 5.5 V, T _J = 150°C, T _A = 25°C, see Figure 5-2			209	mA
		R _{θJA} = 109°C/W, V _I = 3.6 V, T _J = 150°C, T _A = 25°C, see Figure 5-2			319	
		R _{θJA} = 109°C/W, V _I = 2.75 V, T _J = 150°C, T _A = 25°C, see Figure 5-2			417	
P _S	Safety input, output, or total power	R _{θJA} = 109°C/W, T _J = 150°C, T _A = 25°C, see Figure 5-4			1147	mW
T _S	Maximum safety temperature				150	°C
DUW-16 PACKAGE						
I _S	Safety input, output, or supply current	R _{θJA} = 75.2°C/W, V _I = 5.5 V, T _J = 150°C, T _A = 25°C			302	mA
		R _{θJA} = 75.2°C/W, V _I = 3.6 V, T _J = 150°C, T _A = 25°C			462	
		R _{θJA} = 75.2°C/W, V _I = 2.75 V, T _J = 150°C, T _A = 25°C			605	
P _S	Safety input, output, or total power				1662	mW
T _S	Maximum safety temperature	R _{θJA} = 75.2°C/W, T _J = 150°C, T _A = 25°C			150	°C

- (1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, R_{θJA}, in the table above is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

T_J = T_A + R_{θJA} × P, where P is the power dissipated in the device.

T_{J(max)} = T_S = T_A + R_{θJA} × P_S, where T_{J(max)} is the maximum allowed junction temperature.

P_S = I_S × V_I, where V_I is the maximum input voltage.

5.9 Electrical Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -4\text{ mA}$; See Figure 6-1	$V_{CCO} - 0.4$ ⁽¹⁾	4.8		V
V_{OL}	Low-level output voltage	$I_{OL} = 4\text{ mA}$; See Figure 6-1		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold			$0.6 \times V_{CCI}$	$0.7 \times V_{CCI}$	V
$V_{IT-(IN)}$	Falling input switching threshold		$0.3 \times V_{CCI}$	$0.4 \times V_{CCI}$		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$	$0.2 \times V_{CCI}$		V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}$ ⁽¹⁾ at INx			10	μA
I_{IL}	Low-level input current	$V_{IL} = 0\text{ V}$ at INx	-10			μA
I_{IH}	High-level input current	$V_{IH} = V_{CCI}$ ⁽¹⁾ at ENx			20	μA
I_{IL}	Low-level input current	$V_{IL} = 0\text{ V}$ at ENx	-20			μA
CMTI	Common mode transient immunity	$V_I = V_{CCI}$ or 0 V , $V_{CM} = 1200\text{ V}$; See Figure 6-4	85	100		$\text{kV}/\mu\text{s}$
C_I	Input Capacitance ⁽²⁾	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi f t)$, $f = 1\text{ MHz}$, $V_{CC} = 5\text{ V}$		2		pF

(1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC}

(2) Measured from input pin to same side ground.

5.10 Supply Current Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT		
ISO7740									
Supply current - Disable	EN2 = 0 V; V _I = V _{CC1} ⁽¹⁾ (ISO7740); V _I = 0 V (ISO7740 with F suffix)		I _{CC1}		1.2	2.3	mA		
			I _{CC2}		0.3	0.8			
	EN2 = 0 V; V _I = 0 V ⁽¹⁾ (ISO7740); V _I = V _{CC1} (ISO7740 with F suffix)		I _{CC1}		5.5	7.8			
			I _{CC2}		0.3	0.8			
Supply current - DC signal	EN2 = V _{CC2} ; V _I = V _{CC1} ⁽¹⁾ (ISO7740); V _I = 0 V (ISO7740 with F suffix)		I _{CC1}		1.2	2.3			
			I _{CC2}		2	3.6			
	EN2 = V _{CC2} ; V _I = 0 V (ISO7740); V _I = V _{CC1} (ISO7740 with F suffix)		I _{CC1}		5.5	7.8			
			I _{CC2}		2.2	3.9			
Supply current - AC signal	All channels switching with square wave clock input; C _L = 15 pF	1 Mbps	I _{CC1}		3.3	4.7			
			I _{CC2}		2.3	4			
		10 Mbps	I _{CC1}		3.4	4.9			
			I _{CC2}		4.2	6.4			
		100 Mbps	I _{CC1}		3.8	6.6			
			I _{CC2}		22.7	29.5			
		ISO7741							
		Supply current - Disable	EN1 = EN2 = 0 V; V _I = V _{CCI} (ISO7741); V _I = 0 V (ISO7741 with F suffix)		I _{CC1}		1	2.2	mA
I _{CC2}					0.8	1.6			
EN1 = EN2 = 0 V; V _I = 0 V (ISO7741); V _I = V _{CCI} (ISO7741 with F suffix)			I _{CC1}		4.3	6.3			
			I _{CC2}		1.8	2.8			
Supply current - DC signal	EN1 = EN2 = V _{CCI} ; V _I = V _{CCI} ⁽¹⁾ (ISO7741); V _I = 0 V (ISO7741 with F suffix)		I _{CC1}		1.5	2.9			
			I _{CC2}		2	3.7			
	EN1 = EN2 = V _{CCI} ; V _I = 0 V (ISO7741); V _I = V _{CCI} (ISO7741 with F suffix)		I _{CC1}		4.8	6.8			
			I _{CC2}		3.2	5.2			
Supply current - AC signal	All channels switching with square wave clock input; C _L = 15 pF	1 Mbps	I _{CC1}		3.2	4.8			
			I _{CC2}		2.8	4.6			
		10 Mbps	I _{CC1}		3.7	5.5			
			I _{CC2}		4.2	6.4			
		100 Mbps	I _{CC1}		11.4	14.4			
			I _{CC2}		21	25			
		ISO7742							
		Supply current - Disable	EN1 = EN2 = 0 V; V _I = V _{CCI} ⁽¹⁾ (ISO7742); V _I = 0 V (ISO7742 with F suffix)		I _{CC1} , I _{CC2}		0.9	2	mA
EN1 = EN2 = 0 V; V _I = 0 V ⁽¹⁾ (ISO7742); V _I = V _{CCI} (ISO7742 with F suffix)			I _{CC1} , I _{CC2}		3	4.6			
Supply current - DC signal	EN1 = EN2 = V _{CCI} ; V _I = V _{CCI} ⁽¹⁾ (ISO7742); V _I = 0 V (ISO7742 with F suffix)		I _{CC1} , I _{CC2}		1.7	3.5			
	EN1 = EN2 = V _{CCI} ; V _I = 0 V (ISO7742); V _I = V _{CCI} (ISO7742 with F suffix)		I _{CC1} , I _{CC2}		4	6			
Supply current - AC signal	All channels switching with square wave clock input; C _L = 15 pF	1 Mbps	I _{CC1} , I _{CC2}		3	4.9			
		10 Mbps	I _{CC1} , I _{CC2}		4	6			
		100 Mbps	I _{CC1} , I _{CC2}		13.4	18.3			

(1) V_{CCI} = Input-side V_{CC}

5.11 Electrical Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -2\text{mA}$; See Figure 6-1	$V_{CCO} - 0.3$ ⁽¹⁾	3.2		V
V_{OL}	Low-level output voltage	$I_{OL} = 2\text{mA}$; See Figure 6-1		0.1	0.3	V
$V_{IT+(IN)}$	Rising input switching threshold			$0.6 \times V_{CCI}$	$0.7 \times V_{CCI}$ ⁽¹⁾	V
$V_{IT-(IN)}$	Falling input switching threshold		$0.3 \times V_{CCI}$	$0.4 \times V_{CCI}$		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$	$0.2 \times V_{CCI}$		V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}$ ⁽¹⁾ at INx			10	μA
I_{IL}	Low-level input current	$V_{IL} = 0 \text{ V}$ at INx	-10			μA
I_{IH}	High-level input current	$V_{IH} = V_{CCI}$ ⁽¹⁾ at ENx			30	μA
I_{IL}	Low-level input current	$V_{IL} = 0 \text{ V}$ at ENx	-30			μA
CMTI	Common mode transient immunity	$V_I = V_{CCI}$ or 0 V , $V_{CM} = 1200 \text{ V}$; See Figure 6-4	85	100		$\text{kV}/\mu\text{s}$

(1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC}

5.12 Supply Current Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7740							
Supply current - Disable	EN2 = 0 V; V _I = V _{CC1} ⁽¹⁾ (ISO7740); V _I = 0 V (ISO7740 with F suffix)		I _{CC1}		1.2	2.3	mA
			I _{CC2}		0.3	0.7	
	EN2 = 0 V; V _I = 0 V ⁽¹⁾ (ISO7740); V _I = V _{CC1} (ISO7740 with F suffix)		I _{CC1}		5.5	7.8	
			I _{CC2}		0.3	0.7	
Supply current - DC signal	EN2 = V _{CC2} ; V _I = V _{CC1} ⁽¹⁾ (ISO7740); V _I = 0 V (ISO7740 with F suffix)		I _{CC1}		1.2	2.2	
			I _{CC2}		1.9	3.6	
	EN2 = V _{CC2} ; V _I = 0 V (ISO7740); V _I = V _{CC1} (ISO7740 with F suffix)		I _{CC1}		5.5	7.8	
			I _{CC2}		2.2	3.9	
Supply current - AC signal	All channels switching with square wave clock input; C _L = 15 pF	1 Mbps	I _{CC1}		3.3	4.7	
			I _{CC2}		2.2	3.9	
		10 Mbps	I _{CC1}		3.4	4.7	
			I _{CC2}		3.6	5.6	
		100 Mbps	I _{CC1}		3.3	5.7	
			I _{CC2}		17	22.3	
ISO7741							
Supply current - Disable	EN1 = EN2 = 0 V; V _I = V _{CCI} (ISO7741); V _I = 0 V (ISO7741 with F suffix)		I _{CC1}		1	2.1	mA
			I _{CC2}		0.8	1.5	
	EN1 = EN2 = 0 V; V _I = 0 V (ISO7741); V _I = V _{CCI} (ISO7741 with F suffix)		I _{CC1}		4.3	6.3	
			I _{CC2}		1.9	2.7	
Supply current - DC signal	EN1 = EN2 = V _{CCI} ; V _I = V _{CCI} ⁽¹⁾ (ISO7741); V _I = 0 V (ISO7741 with F suffix)		I _{CC1}		1.5	2.8	
			I _{CC2}		2	3.7	
	EN1 = EN2 = V _{CCI} ; V _I = 0 V (ISO7741); V _I = V _{CCI} (ISO7741 with F suffix)		I _{CC1}		4.8	6.8	
			I _{CC2}		3.2	5.1	
Supply current - AC signal	All channels switching with square wave clock input; C _L = 15 pF	1 Mbps	I _{CC1}		3.2	4.7	
			I _{CC2}		2.7	4.5	
		10 Mbps	I _{CC1}		3.5	5.2	
			I _{CC2}		3.7	5.8	
		100 Mbps	I _{CC1}		8	11	
			I _{CC2}		15	19.5	
ISO7742							
Supply current - Disable	EN1 = EN2 = 0 V; V _I = V _{CCI} ⁽¹⁾ (ISO7742); V _I = 0 V (ISO7742 with F suffix)		I _{CC1} , I _{CC2}		0.9	2	mA
	EN1 = EN2 = 0 V; V _I = 0 V ⁽¹⁾ (ISO7742); V _I = V _{CCI} (ISO7742 with F suffix)		I _{CC1} , I _{CC2}		3	4.6	
Supply current - DC signal	EN1 = EN2 = V _{CCI} ; V _I = V _{CCI} ⁽¹⁾ (ISO7742); V _I = 0 V (ISO7742 with F suffix)		I _{CC1} , I _{CC2}		1.7	3.4	
	EN1 = EN2 = V _{CCI} ; V _I = 0 V (ISO7742); V _I = V _{CCI} (ISO7742 with F suffix)		I _{CC1} , I _{CC2}		4	5.9	
Supply current - AC signal	All channels switching with square wave clock input; C _L = 15 pF	1 Mbps	I _{CC1} , I _{CC2}		2.9	4.8	
		10 Mbps	I _{CC1} , I _{CC2}		3.6	5.6	
		100 Mbps	I _{CC1} , I _{CC2}		10.3	14.4	

(1) V_{CCI} = Input-side V_{CC}

5.13 Electrical Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage $I_{OH} = -1\text{mA}$; See Figure 6-1	$V_{CCO} - 0.2^{(1)}$	2.45		V
V_{OL}	Low-level output voltage $I_{OL} = 1\text{mA}$; See Figure 6-1		0.05	0.2	V
$V_{IT+(IN)}$	Rising input switching threshold		$0.6 \times V_{CCI}$	$0.7 \times V_{CCI}$	V
$V_{IT-(IN)}$	Falling input switching threshold	$0.3 \times V_{CCI}$	$0.4 \times V_{CCI}$		V
$V_{I(HYS)}$	Input threshold voltage hysteresis	$0.1 \times V_{CCI}$	$0.2 \times V_{CCI}$		V
I_{IH}	High-level input current $V_{IH} = V_{CCI}^{(1)}$ at INx			10	μA
I_{IL}	Low-level input current $V_{IL} = 0 \text{ V}$ at INx	-10			μA
I_{IH}	High-level input current $V_{IH} = V_{CCI}^{(1)}$ at ENx			30	μA
I_{IL}	Low-level input current $V_{IL} = 0 \text{ V}$ at ENx	-30			μA
CMTI	Common mode transient immunity $V_I = V_{CCI}$ or 0 V , $V_{CM} = 1200 \text{ V}$; See Figure 6-4	85	100		$\text{kV}/\mu\text{s}$

(1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC}

5.14 Supply Current Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7740							
Supply current - Disable	EN2 = 0 V; V _I = V _{CC1} ⁽¹⁾ (ISO7740); V _I = 0 V (ISO7740 with F suffix)		I _{CC1}		1.2	2.2	mA
			I _{CC2}		0.3	0.7	
	EN2 = 0 V; V _I = 0 V ⁽¹⁾ (ISO7740); V _I = V _{CC1} (ISO7740 with F suffix)		I _{CC1}		5.5	7.8	
			I _{CC2}		0.3	0.7	
Supply current - DC signal	EN2 = V _{CC2} ; V _I = V _{CC1} ⁽¹⁾ (ISO7740); V _I = 0 V (ISO7740 with F suffix)		I _{CC1}		1.2	2.2	
			I _{CC2}		1.9	3.6	
	EN2 = V _{CC2} ; V _I = 0 V (ISO7740); V _I = V _{CC1} (ISO7740 with F suffix)		I _{CC1}		5.4	7.8	
			I _{CC2}		2.2	3.9	
Supply current - AC signal	All channels switching with square wave clock input; C _L = 15 pF	1 Mbps	I _{CC1}		3.3	4.7	
			I _{CC2}		2.2	3.9	
		10 Mbps	I _{CC1}		3.4	4.8	
			I _{CC2}		3.2	5.1	
		100 Mbps	I _{CC1}		3.2	5.5	
			I _{CC2}		13	17.7	
ISO7741							
Supply current - Disable	EN1 = EN2 = 0 V; V _I = V _{CCI} (ISO7741); V _I = 0 V (ISO7741 with F suffix)		I _{CC1}		1.5	2.2	mA
			I _{CC2}		0.8	2.8	
	EN1 = EN2 = 0 V; V _I = 0 V (ISO7741); V _I = V _{CCI} (ISO7741 with F suffix)		I _{CC1}		4.3	6.3	
			I _{CC2}		1.8	2.8	
Supply current - DC signal	EN1 = EN2 = V _{CCI} ; V _I = V _{CCI} ⁽¹⁾ (ISO7741); V _I = 0 V (ISO7741 with F suffix)		I _{CC1}		1.4	2.9	
			I _{CC2}		2	3.9	
	EN1 = EN2 = V _{CCI} ; V _I = 0 V (ISO7741); V _I = V _{CCI} (ISO7741 with F suffix)		I _{CC1}		4.7	6.8	
			I _{CC2}		3.2	5.21	
Supply current - AC signal	All channels switching with square wave clock input; C _L = 15 pF	1 Mbps	I _{CC1}		3.1	4.8	
			I _{CC2}		2.7	4.7	
		10 Mbps	I _{CC1}		3.4	5.2	
			I _{CC2}		3.5	5.64	
		100 Mbps	I _{CC1}		5.6	8.7	
			I _{CC2}		10.8	15	
ISO7742							
Supply current - Disable	EN1 = EN2 = 0 V; V _I = V _{CCI} ⁽¹⁾ (ISO7742); V _I = 0 V (ISO7742 with F suffix)		I _{CC1} , I _{CC2}		0.9	1.9	mA
	EN1 = EN2 = 0 V; V _I = 0 V ⁽¹⁾ (ISO7742); V _I = V _{CCI} (ISO7742 with F suffix)		I _{CC1} , I _{CC2}		3	4.6	
Supply current - DC signal	EN1 = EN2 = V _{CCI} ; V _I = V _{CCI} ⁽¹⁾ (ISO7742); V _I = 0 V (ISO7742 with F suffix)		I _{CC1} , I _{CC2}		1.7	3.4	
	EN1 = EN2 = V _{CCI} ; V _I = 0 V (ISO7742); V _I = V _{CCI} (ISO7742 with F suffix)		I _{CC1} , I _{CC2}		4	5.9	
Supply current - AC signal	All channels switching with square wave clock input; C _L = 15 pF	1 Mbps	I _{CC1} , I _{CC2}		2.9	4.7	
		10 Mbps	I _{CC1} , I _{CC2}		3.4	5.4	
		100 Mbps	I _{CC1} , I _{CC2}		8.3	11.9	

(1) V_{CCI} = Input-side V_{CC}

5.15 Switching Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 6-1	6	12.7	17	ns
PWD	Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				5.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time ⁽²⁾	Same-direction channels			4	ns
$t_{sk(pp)}$	Part-to-part skew time ⁽³⁾				4.4	ns
t_r	Output signal rise time	See Figure 6-1		1.1	3.9	ns
t_f	Output signal fall time			1.1	3.9	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 6-2		14	22	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			13	20	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO774x			11	20	ns
	Enable propagation delay, high impedance-to-high output for ISO774x with F suffix			3	8.5	μs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO774x			2.5	8.5	μs
	Enable propagation delay, high impedance-to-low output for ISO774x with F suffix			7	20	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V. See Figure 6-4		0.1	0.3	μs
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		1.4		ns

(1) Also known as pulse skew.

(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.16 Switching Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL}	Propagation delay time	See Figure 6-1	6	13.5	18.5	ns
PWD	Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				5.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time ⁽²⁾	Same-direction channels			4.4	ns
$t_{sk(pp)}$	Part-to-part skew time ⁽³⁾				5	ns
t_r	Output signal rise time	See Figure 6-1		0.6	3	ns
t_f	Output signal fall time			0.6	3	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 6-2		19	31	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			18	30	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO774x			14	30	ns
	Enable propagation delay, high impedance-to-high output for ISO774x with F suffix			3.2	8.5	μs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO774x			2.5	8.5	μs
	Enable propagation delay, high impedance-to-low output for ISO774x with F suffix			17	30	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V. See Figure 6-4		0.1	0.3	μs
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		1.3		ns

(1) Also known as pulse skew.

(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.17 Switching Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL}	Propagation delay time	See Figure 6-1	7.5	14	21	ns
PWD	Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				5.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time ⁽²⁾	Same-direction channels			4.4	ns
$t_{sk(pp)}$	Part-to-part skew time ⁽³⁾				5.3	ns
t_r	Output signal rise time	See Figure 6-1		0.8	3.5	ns
t_f	Output signal fall time			0.8	3.5	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 6-2		24	41	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			22	40	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO774x			18	40	ns
	Enable propagation delay, high impedance-to-high output for ISO774x with F suffix			3.3	8.5	μs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO774x			2.7	8.5	μs
	Enable propagation delay, high impedance-to-low output for ISO774x with F suffix			18	40	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V. See Figure 6-4		0.1	0.3	μs
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		1.5		ns

(1) Also known as pulse skew.

(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.18 Insulation Characteristics Curves

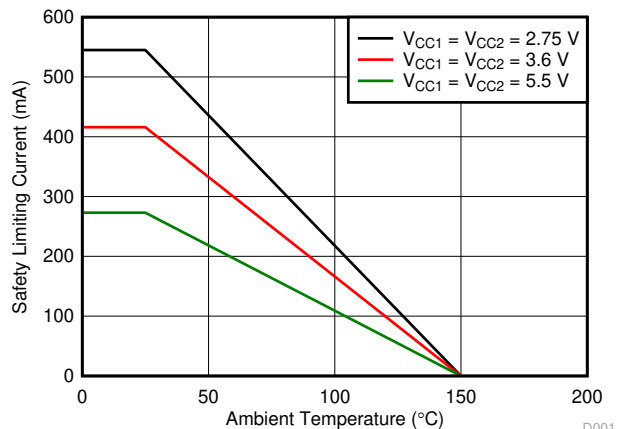


Figure 5-1. Thermal Derating Curve for Safety Limiting Current for DW-16 Package

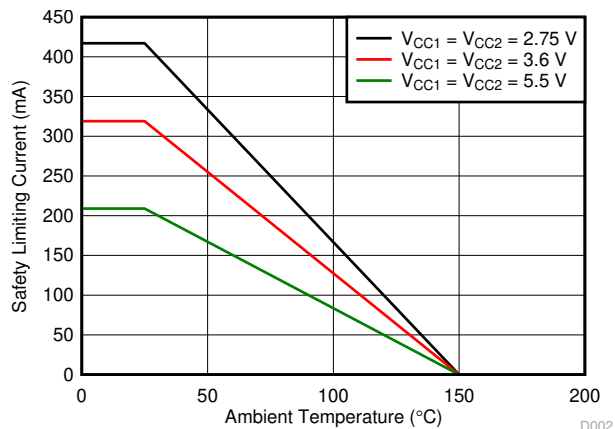


Figure 5-2. Thermal Derating Curve for Safety Limiting Current for DBQ-16 Package

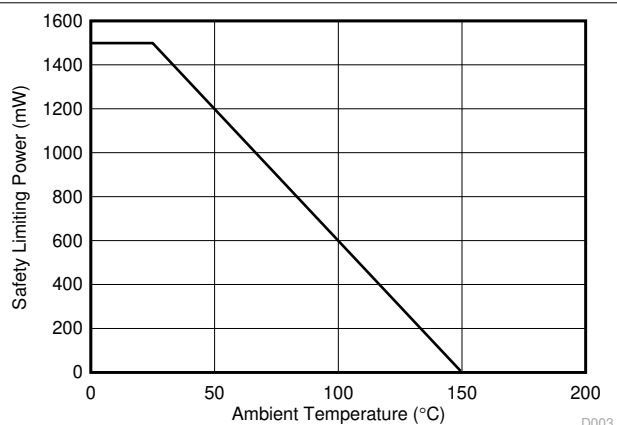


Figure 5-3. Thermal Derating Curve for Safety Limiting Power for DW-16 Package

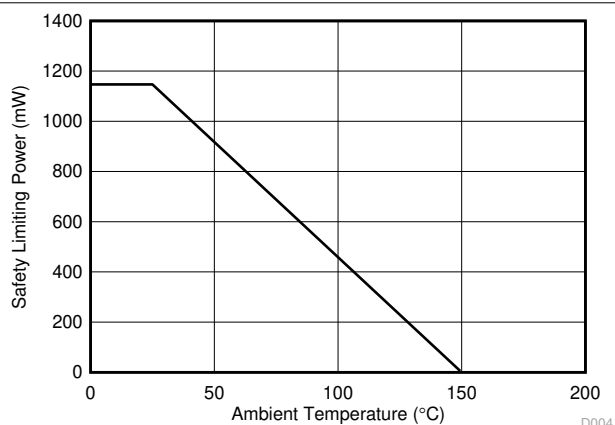


Figure 5-4. Thermal Derating Curve for Safety Limiting Power for DBQ-16 Package

5.19 Typical Characteristics

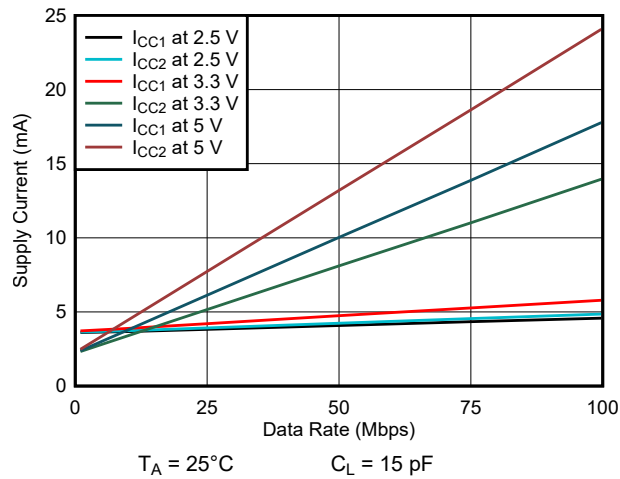


Figure 5-5. ISO7740 Supply Current vs Data Rate (With 15-pF Load)

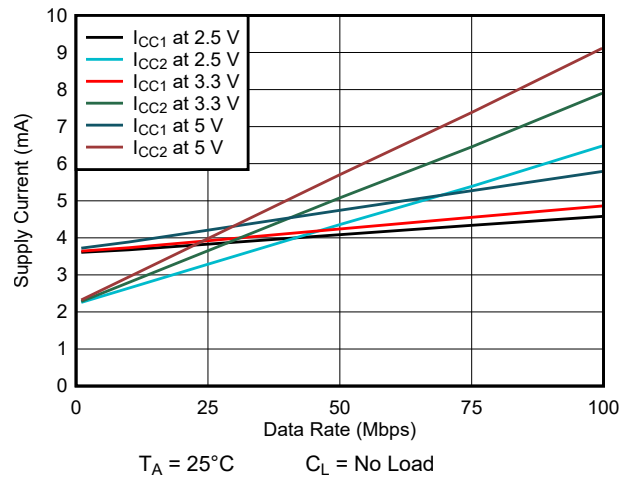


Figure 5-6. ISO7740 Supply Current vs Data Rate (With No Load)

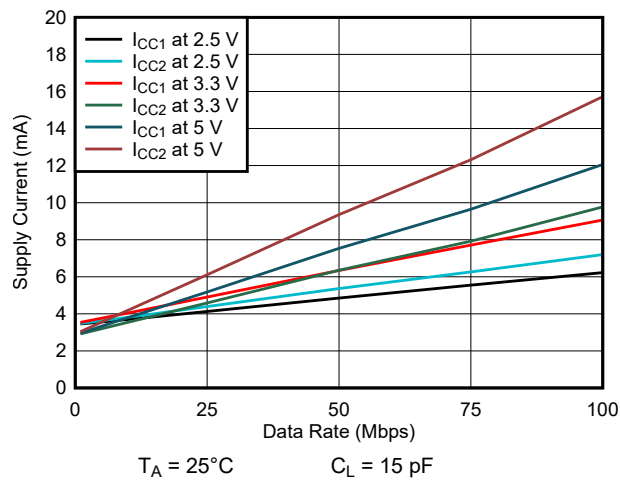


Figure 5-7. ISO7741 Supply Current vs Data Rate (With 15-pF Load)

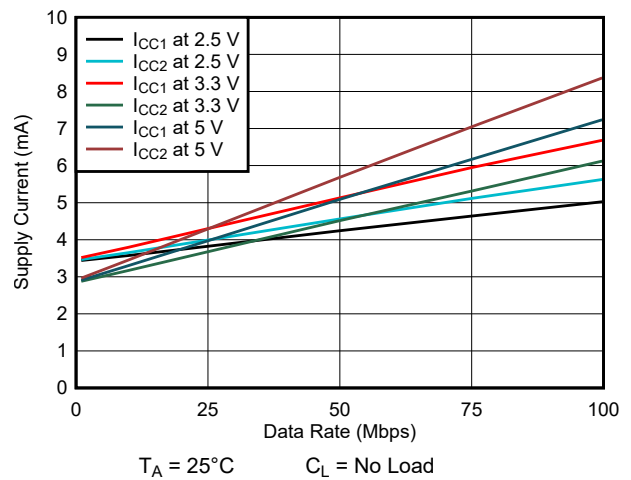


Figure 5-8. ISO7741 Supply Current vs Data Rate (With No Load)

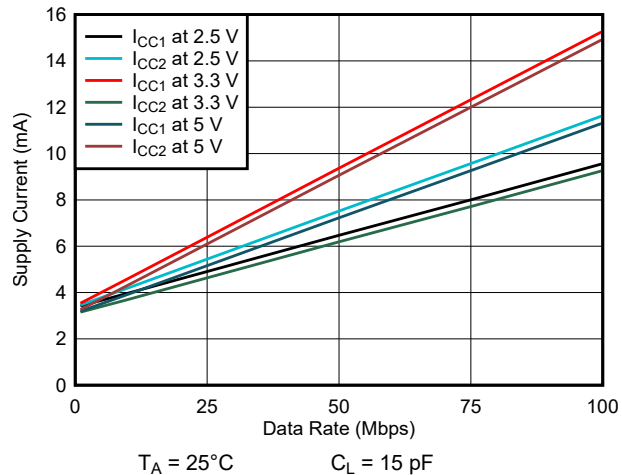


Figure 5-9. ISO7742 Supply Current vs Data Rate (With 15-pF Load)

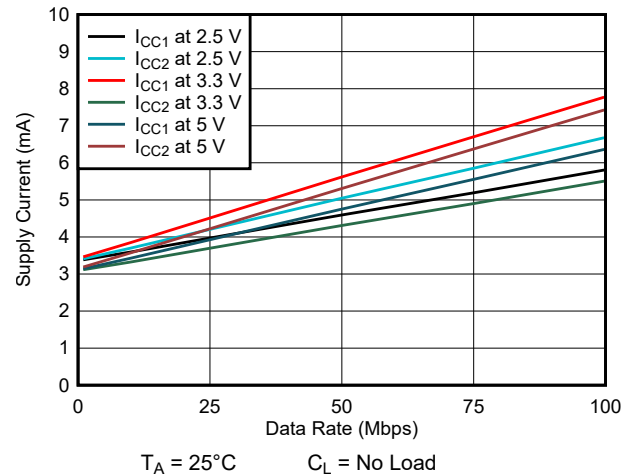


Figure 5-10. ISO7742 Supply Current vs Data Rate (With No Load)

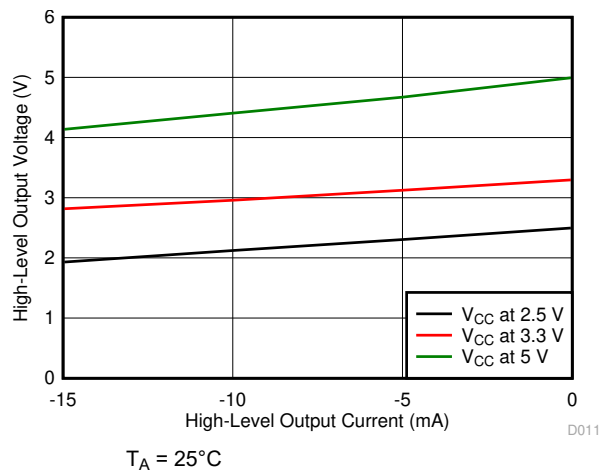


Figure 5-11. High-Level Output Voltage vs High-level Output Current

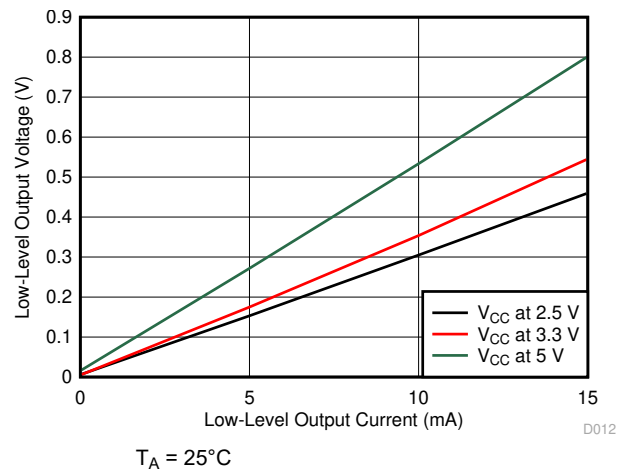


Figure 5-12. Low-Level Output Voltage vs Low-Level Output Current

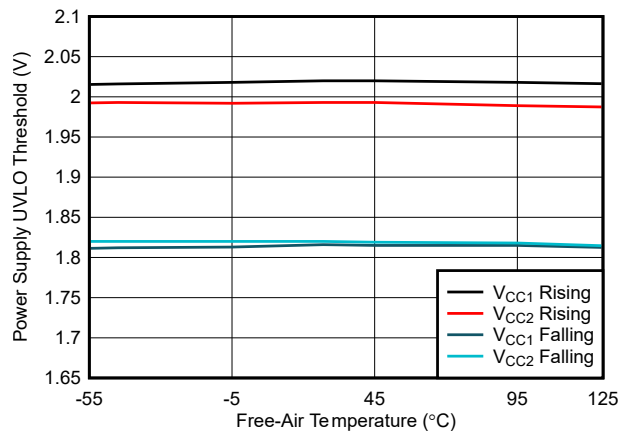


Figure 5-13. Power Supply Undervoltage Threshold vs Free-Air Temperature

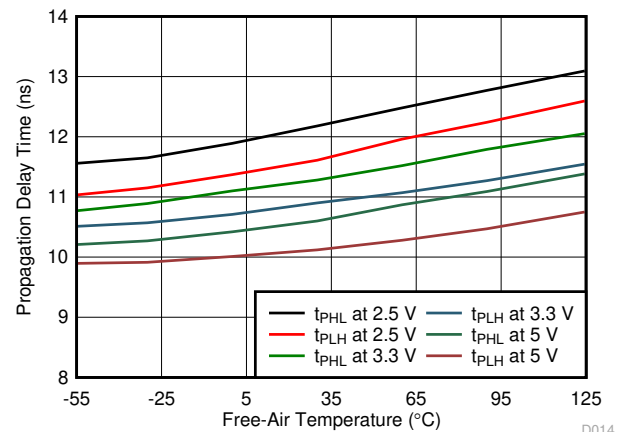
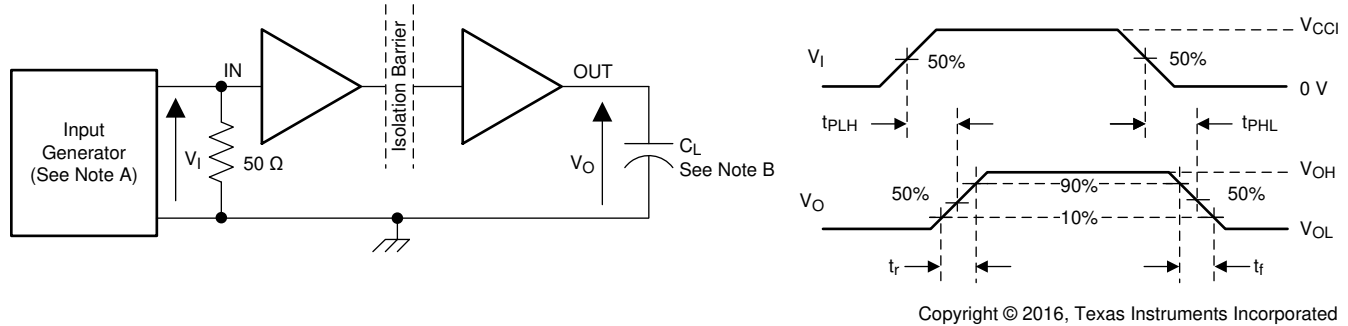


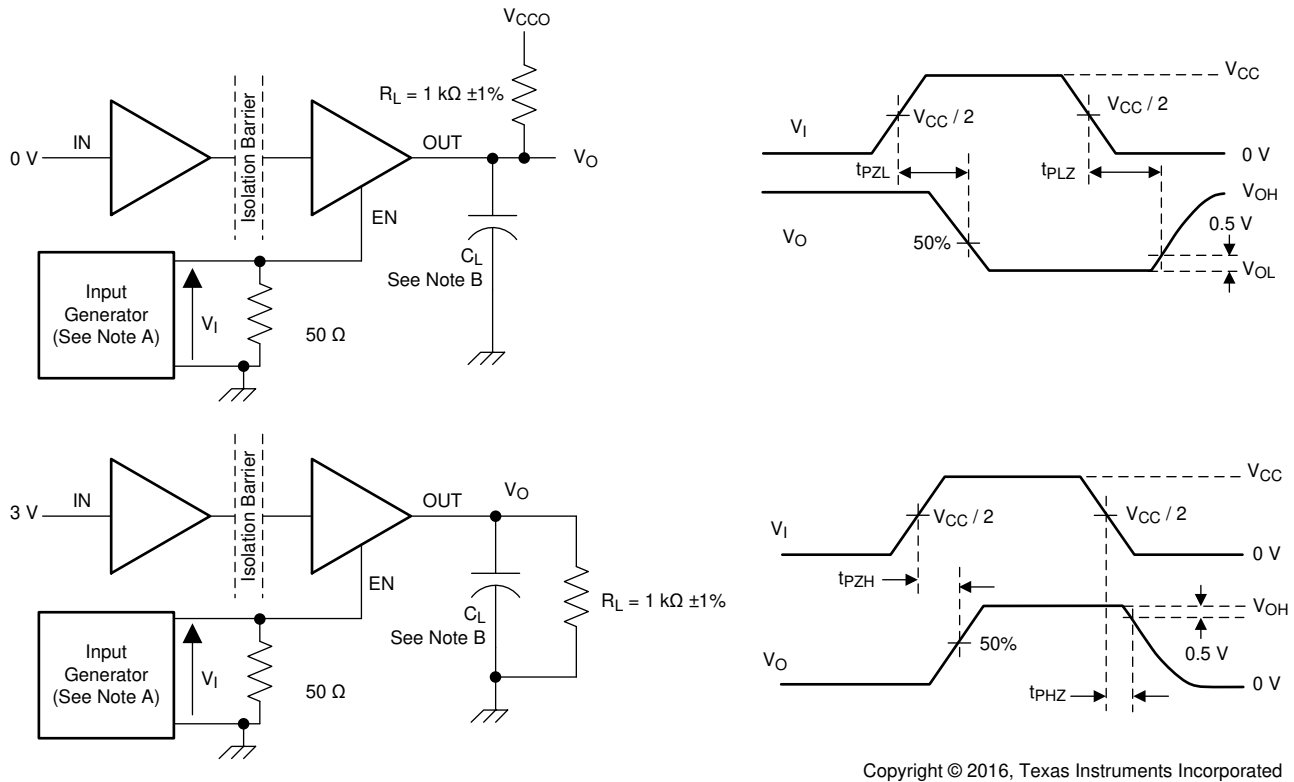
Figure 5-14. Propagation Delay Time vs Free-Air Temperature

6 Parameter Measurement Information



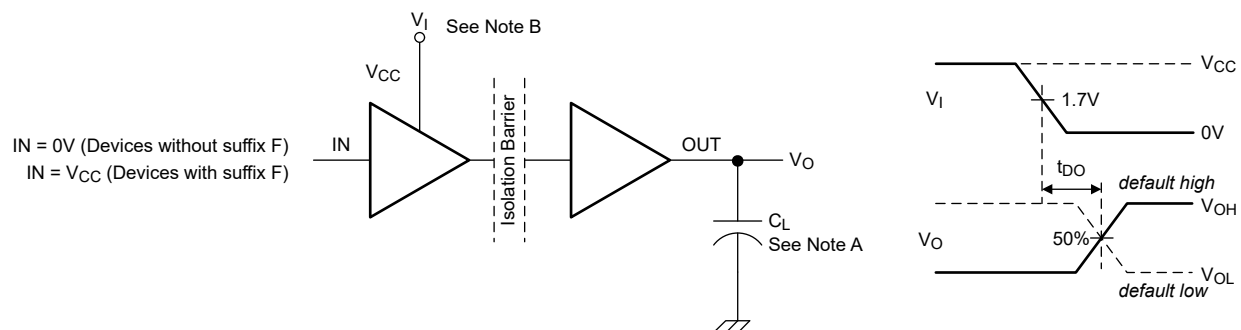
- A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 50$ kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_O = 50 \Omega$. At the input, 50Ω resistor is required to terminate Input Generator signal. The $50\text{-}\Omega$ resistor is not needed in the actual application.
- B. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 6-1. Switching Characteristics Test Circuit and Voltage Waveforms



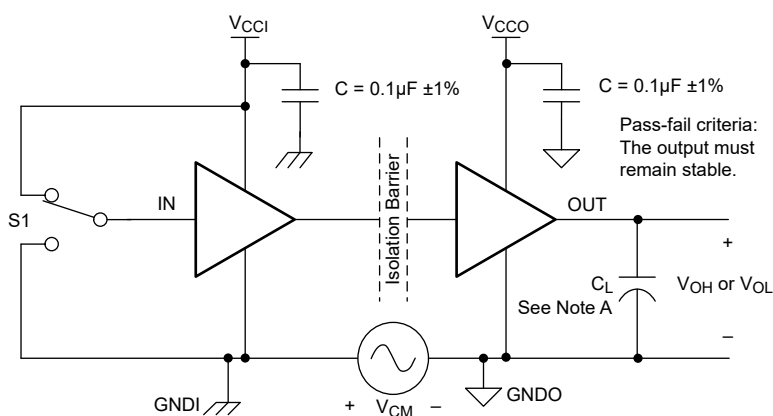
- A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 10$ kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_O = 50 \Omega$.
- B. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 6-2. Enable/Disable Propagation Delay Time Test Circuit and Waveform



- A. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.
B. Power Supply Ramp Rate = 10 mV/ns

Figure 6-3. Default Output Delay Time Test Circuit and Voltage Waveforms



- A. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 6-4. Common-Mode Transient Immunity Test Circuit

7 Detailed Description

7.1 Overview

The ISO774x family of devices uses an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the ENx pin is low then the output goes to high impedance. The ISO774x devices also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, [Figure 7-1](#), shows a functional block diagram of a typical channel.

7.2 Functional Block Diagram

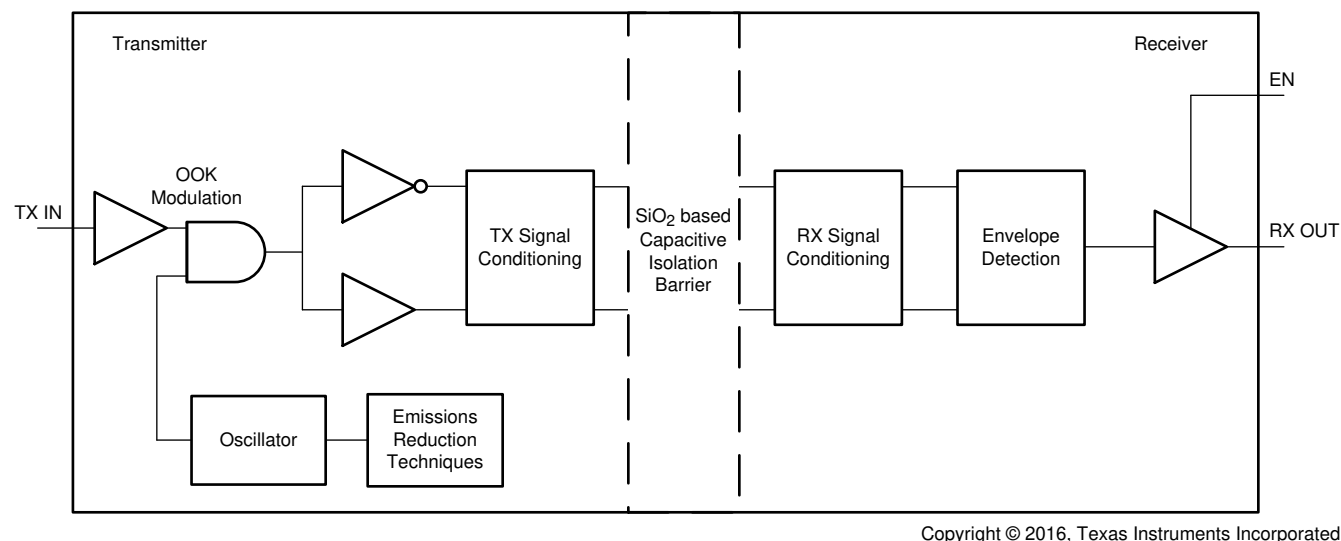


Figure 7-1. Conceptual Block Diagram of a Digital Capacitive Isolator

[Figure 7-2](#) shows a conceptual detail of how the ON-OFF keying scheme works.

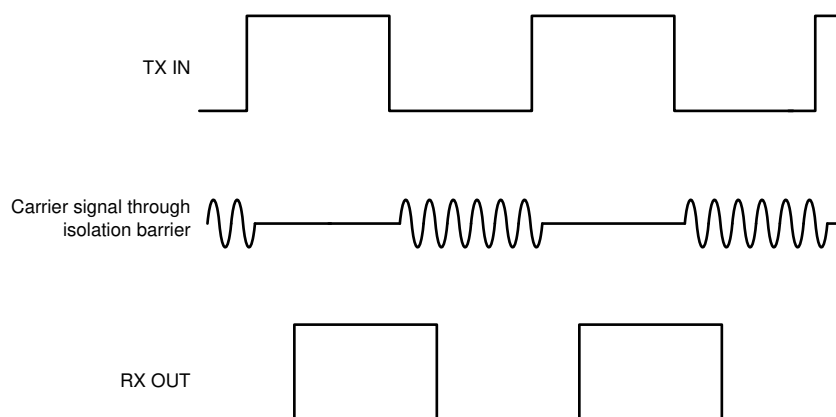


Figure 7-2. On-Off Keying (OOK) Based Modulation Scheme

7.3 Feature Description

Table 7-1 provides an overview of the device features.

Table 7-1. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE	RATED ISOLATION
ISO7740	4 Forward, 0 Reverse	100 Mbps	High	DW-16	5000 V _{RMS} (DW), 5700 V _{RMS} (DUW) / 8000 V _{PK}
				DBQ-16	3000 V _{RMS} / 4242 V _{PK}
ISO7740 with F suffix	4 Forward, 0 Reverse	100 Mbps	Low	DW-16	5000 V _{RMS} (DW), 5700 V _{RMS} (DUW) / 8000 V _{PK}
				DBQ-16	3000 V _{RMS} / 4242 V _{PK}
ISO7741	3 Forward, 1 Reverse	100 Mbps	High	DW-16	5000 V _{RMS} (DW), 5700 V _{RMS} (DUW) / 8000 V _{PK}
				DBQ-16	3000 V _{RMS} / 4242 V _{PK}
ISO7741 with F suffix	3 Forward, 1 Reverse	100 Mbps	Low	DW-16	5000 V _{RMS} (DW), 5700 V _{RMS} (DUW) / 8000 V _{PK}
				DBQ-16	3000 V _{RMS} / 4242 V _{PK}
ISO7741B	3 Forward, 1 Reverse	100 Mbps	High	DW-16	5000 V _{RMS} (DW), 5700 V _{RMS} (DUW) / 8000 V _{PK}
ISO7741B with F suffix	3 Forward, 1 Reverse	100 Mbps	Low	DW-16	5000 V _{RMS} (DW), 5700 V _{RMS} (DUW) / 8000 V _{PK}
ISO7742	2 Forward, 2 Reverse	100 Mbps	High	DW-16	5000 V _{RMS} (DW), 5700 V _{RMS} (DUW) / 8000 V _{PK}
				DBQ-16	3000 V _{RMS} / 4242 V _{PK}
ISO7742 with F suffix	2 Forward, 2 Reverse	100 Mbps	Low	DW-16	5000 V _{RMS} (DW), 5700 V _{RMS} (DUW) / 8000 V _{PK}
				DBQ-16	3000 V _{RMS} / 4242 V _{PK}

7.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO774x family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by providing purely differential internal operation.

7.4 Device Functional Modes

Table 7-2 lists the functional modes for the ISO774x devices.

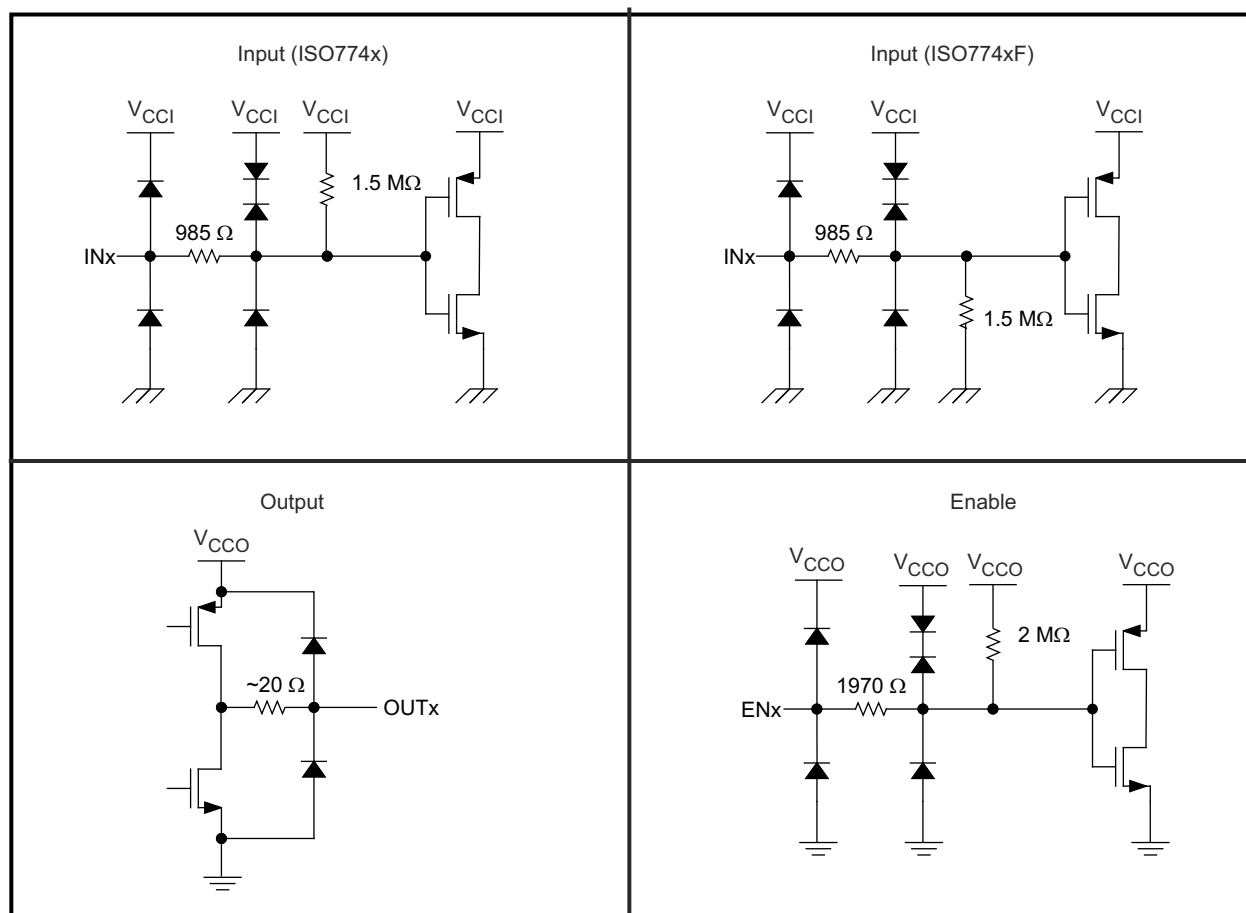
Table 7-2. Function Table

V_{CCI}	V_{CCO}	INPUT (INx) ⁽²⁾	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of the input.
		L	H or open	L	
		Open	H or open	Default	Default mode: When INx is open, the corresponding channel output goes to the default logic state. Default is <i>High</i> for ISO774x and <i>Low</i> for ISO774x with F suffix.
X	PU	X	L	Z	A low value of output enable causes the outputs to be high-impedance.
PD	PU	X	H or open	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is <i>High</i> for ISO774x and <i>Low</i> for ISO774x with F suffix. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined ⁽¹⁾ . When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input.

(1) The outputs are in undetermined state when $1.7\text{ V} < V_{CCI}$, $V_{CCO} < 2.25\text{ V}$.

(2) A strongly driven input signal can weakly power the floating V_{CC} through an internal protection diode and cause undetermined output.

7.4.1 Device I/O Schematics



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Figure 7-3. Device I/O Schematics

8.2.1 Design Requirements

To design with these devices, use the parameters listed in [Table 8-1](#).

Table 8-1. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	2.25 to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 μ F
Decoupling capacitor from V_{CC2} and GND2	0.1 μ F

8.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO774x family of devices only require two external bypass capacitors to operate.

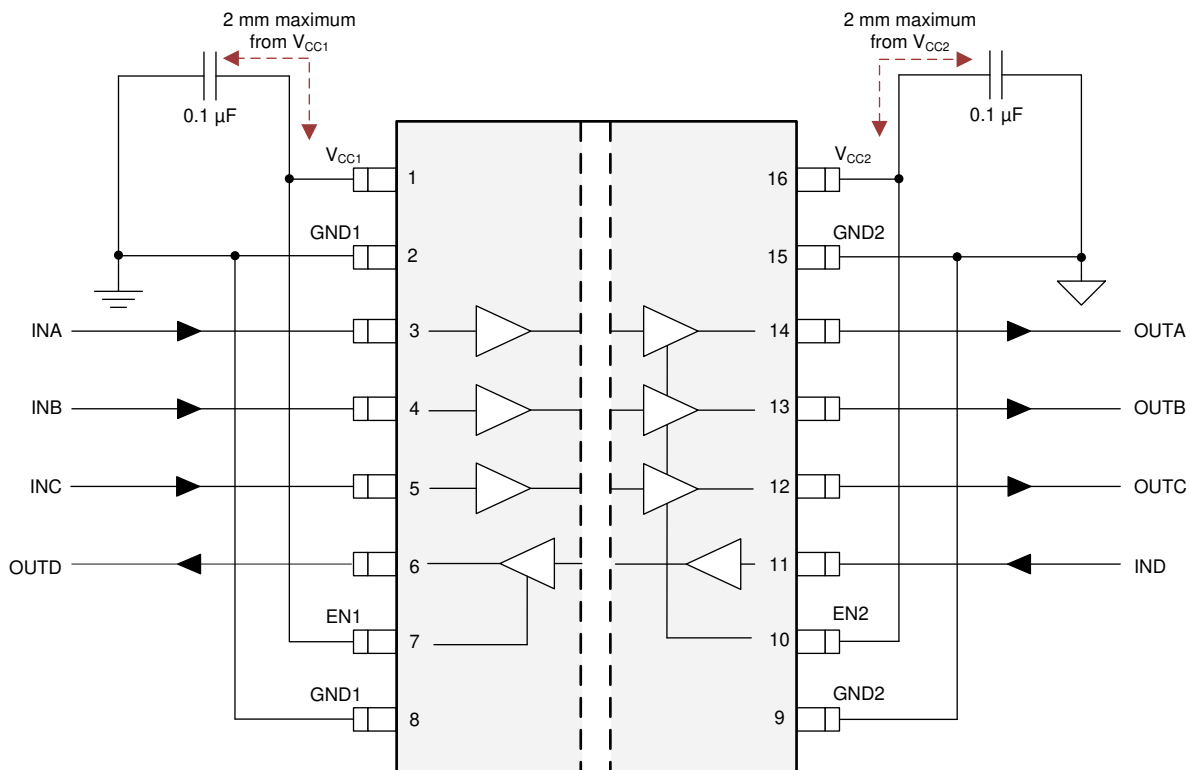


Figure 8-2. Typical ISO774x Circuit Hook-up

The DWW package provides wider creepage and clearance without the need for two isolators in series or an extra isolated power supply, saving design cost and board space. For more details, please refer to the technical document [How to Meet the Higher Isolation Creepage & Clearance Needs in Automotive Applications](#).

8.2.3 Application Curve

The following typical eye diagrams of the ISO774x family of devices indicates low jitter and wide open eye at the maximum data rate of 100 Mbps.

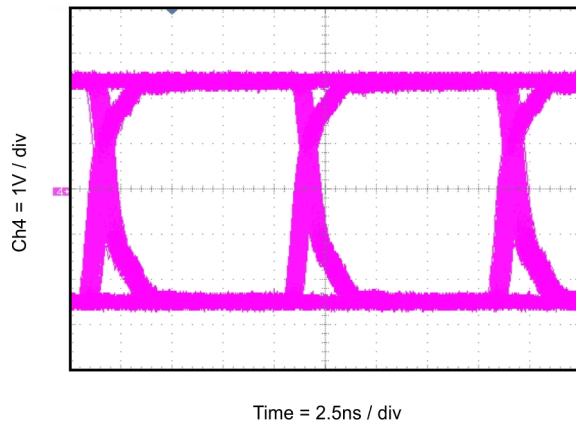


Figure 8-3. Eye Diagram at 100 Mbps PRBS $2^{16} - 1$, 5 V and 25°C

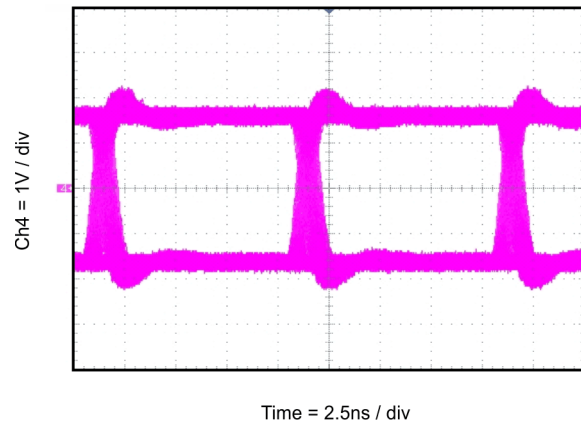


Figure 8-4. Eye Diagram at 100 Mbps PRBS $2^{16} - 1$, 3.3 V and 25°C

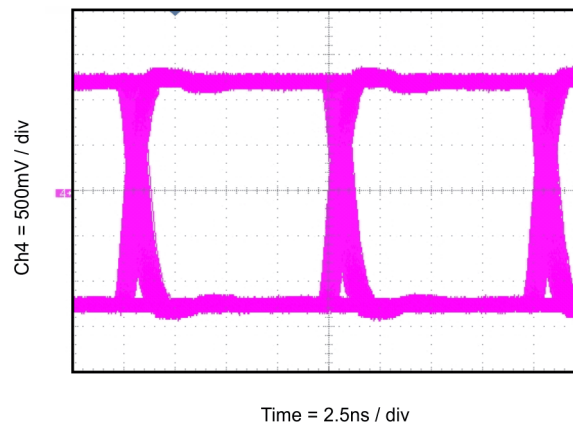


Figure 8-5. Eye Diagram at 100 Mbps PRBS $2^{16} - 1$, 2.5 V and 25°C

8.2.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See [Figure 8-6](#) for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that is 20% higher than the specified value.

[Figure 8-7](#) shows the intrinsic capability of the isolation barrier to withstand high voltage stress over the lifetime of the barrier. Based on the TDDB data, the intrinsic capability of the insulation is 1500V_{RMS} with a lifetime of 36 years. Other factors, such as package size, pollution degree, material group, and more can further limit the working voltage of the component. The working voltage of DW-16 package is specified up to 1500V_{RMS}. At the lower working voltages, the corresponding insulation lifetime is much longer than 36 years. DBQ-16 package at 400V_{RMS} working voltage has a much longer lifetime than DW-16 package.

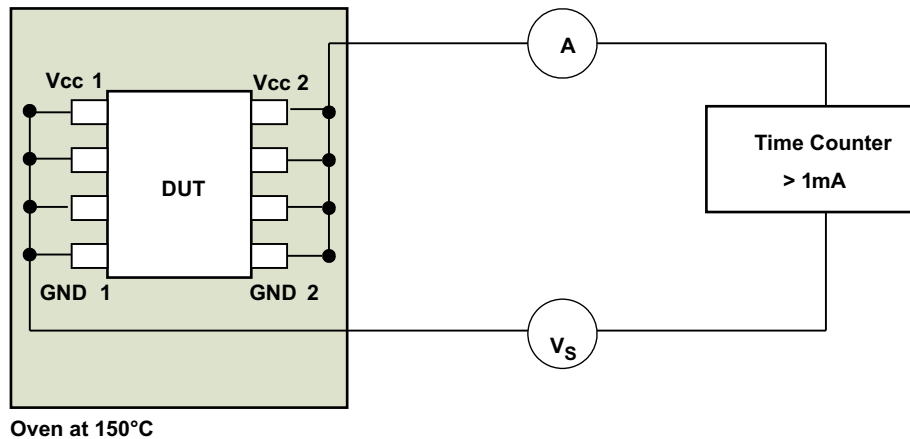


Figure 8-6. Test Setup for Insulation Lifetime Measurement

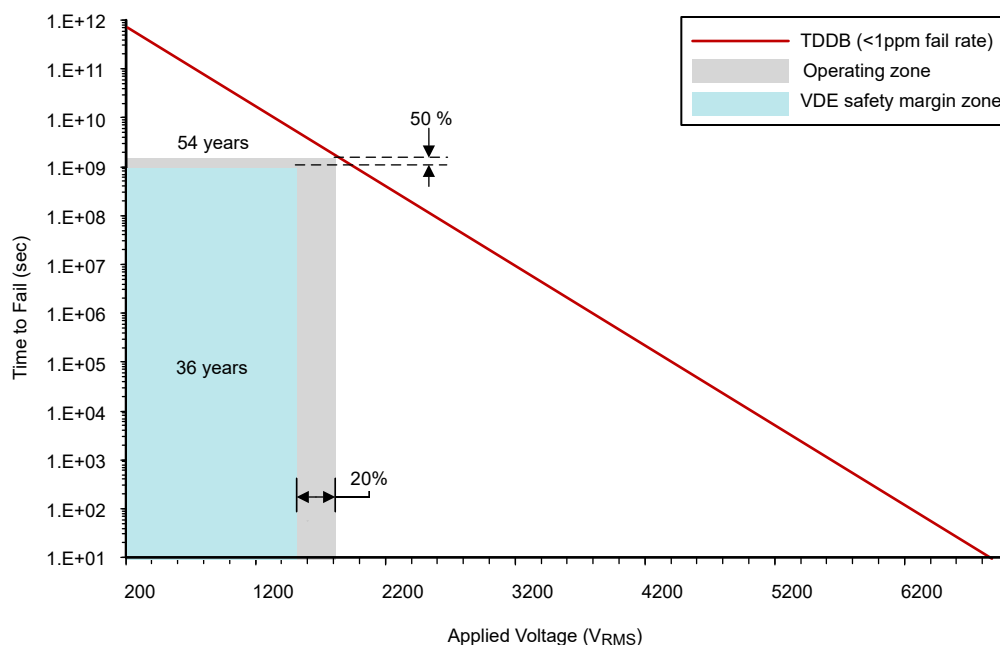


Figure 8-7. Insulation Lifetime Projection Data

8.3 Power Supply Recommendations

To help provide reliable operation at data rates and supply voltages, a 0.1- μ F bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' [SN6501](#) or [SN6505A](#). For such applications, detailed power supply design and transformer selection recommendations are available in [SN6501 Transformer Driver for Isolated Power Supplies data sheet](#) or [SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies data sheet](#).

8.4 Layout

8.4.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see [Figure 8-8](#)). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch².
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typical have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the [Digital Isolator Design Guide](#).

8.4.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit boards. This PCB is preferred over cheaper alternatives due to the lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability-characteristics.

8.4.2 Layout Example

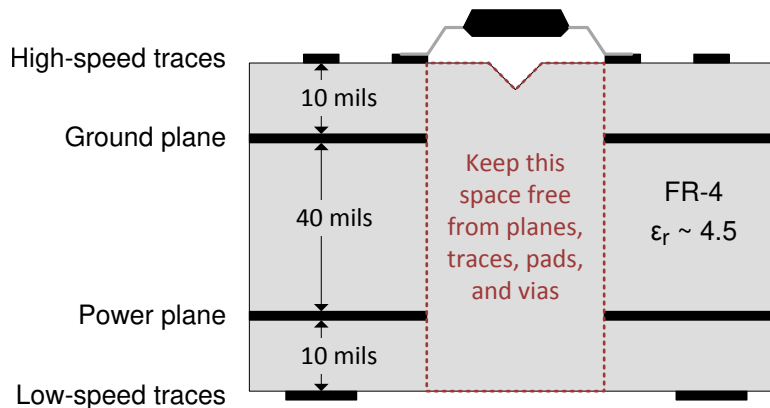


Figure 8-8. Layout Example Schematic

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [ADS79xx 12/10/8-Bit, 1 MSPS, 16/12/8/4-Channel, Single-Ended, MicroPower, Serial Interface ADCs](#), data sheet
- Texas Instruments, [Digital Isolator Design Guide](#), application note
- Texas Instruments, [Isolation Glossary](#), application note
- Texas Instruments, [How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems](#), application note
- Texas Instruments, [MSP430G2132 Mixed Signal Microcontroller](#), data sheet
- Texas Instruments, [REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference](#), data sheet
- Texas Instruments, [SN6501 Transformer Driver for Isolated Power Supplies](#), data sheet
- Texas Instruments, [SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies](#), data sheet
- Texas Instruments, [TLV707, TLV707P 200-mA, Low-IQ, Low-Noise, Low-Dropout Regulator for Portable Devices](#), data sheet

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (October 2024) to Revision K (August 2026)	Page
• Added information about ultra-wide and smaller, cost-optimized packages in the <i>Features</i> section.....	1
• Updated the numbering format for tables, figures, and cross-references throughout document.....	2
• Updated Safety-Related Certifications table by removing detailed ratings information as these details are available in actual certificates.....	11

Changes from Revision I (January 2024) to Revision J (October 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout document.....	2
• Updated distance through isolation, while maintaining other insulation specifications.....	9
• Updated the input leakage current for ENx pins throughout the electrical characteristic sections.....	13

Changes from Revision H (March 2023) to Revision I (January 2024)	Page
• Updated Features list.....	1
• Updated numbering format for tables, figures and cross-references throughout document.....	2
• Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations.....	6
• Updated electrical and switching characteristics to match device performance.....	6
• Updated the TDDb plot and the projected lifetime.....	33

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7740DBQR	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7740
ISO7740DBQR.A	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7740
ISO7740DWR	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7740
ISO7740DWR.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7740
ISO7740FDBQR	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7740F
ISO7740FDBQR.A	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7740F
ISO7740FDBQRG4	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7740F
ISO7740FDBQRG4.A	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7740F
ISO7740FDWR	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7740F
ISO7740FDWR.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7740F
ISO7741BDWR	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7741B
ISO7741BDWR.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7741B
ISO7741DBQR	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7741
ISO7741DBQR.A	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7741
ISO7741DBQRG4	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7741
ISO7741DBQRG4.A	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7741
ISO7741DWR	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7741
ISO7741DWR.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7741
ISO7741DWRG4	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7741
ISO7741DWRG4.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7741
ISO7741FBDWR	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7741FB
ISO7741FBDWR.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7741FB
ISO7741FDBQR	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7741F
ISO7741FDBQR.A	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7741F
ISO7741FDBQRG4	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7741F
ISO7741FDBQRG4.A	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7741F
ISO7741FDWR	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7741F
ISO7741FDWR.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7741F
ISO7741FDWRG4	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7741F

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7741FDWRG4.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7741F
ISO7741FSDBQR	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-55 to 125	7741FS
ISO7742DBQR	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7742
ISO7742DBQR.A	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7742
ISO7742DWR	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7742
ISO7742DWR.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7742
ISO7742FDBQR	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7742F
ISO7742FDBQR.A	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7742F
ISO7742FDWR	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7742F
ISO7742FDWR.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7742F
ISO7742FSDBQR	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-55 to 125	7742FS

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF ISO7740, ISO7741, ISO7742 :

- Automotive : [ISO7740-Q1](#), [ISO7741-Q1](#), [ISO7742-Q1](#)

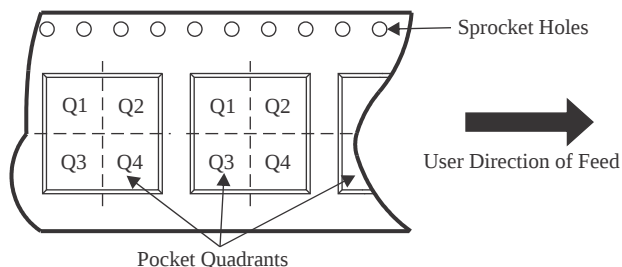
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7740DBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7740DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7740DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7740DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7740FDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7740FDBQRG4	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7740FDBQRG4	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7740FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7740FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7741BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7741BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7741DBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7741DBQRG4	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7741DBQRG4	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7741DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7741DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7741DWRG4	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7741DWRG4	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7741FBDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7741FDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7741FDBQRG4	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7741FDBQRG4	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7741FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7741FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7741FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7741FDWRG4	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7741FDWRG4	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7741FDWRG4	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7741FSDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7742DBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7742DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7742DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7742DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7742FDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7742FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7742FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7742FSDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7740DBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO7740DWR	SOIC	DW	16	2000	356.0	356.0	45.0
ISO7740DWR	SOIC	DW	16	2000	353.0	353.0	32.0
ISO7740DWR	SOIC	DW	16	2000	356.0	356.0	36.0
ISO7740FDBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO7740FDBQRG4	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7740FDBQRG4	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7740FDWR	SOIC	DW	16	2000	353.0	353.0	32.0
ISO7740FDWR	SOIC	DW	16	2000	356.0	356.0	45.0
ISO7741BDWR	SOIC	DW	16	2000	356.0	356.0	36.0
ISO7741BDWR	SOIC	DW	16	2000	353.0	353.0	32.0
ISO7741DBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO7741DBQRG4	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7741DBQRG4	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7741DWR	SOIC	DW	16	2000	356.0	356.0	36.0
ISO7741DWR	SOIC	DW	16	2000	353.0	353.0	32.0
ISO7741DWRG4	SOIC	DW	16	2000	356.0	356.0	36.0
ISO7741DWRG4	SOIC	DW	16	2000	353.0	353.0	32.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7741FBDWR	SOIC	DW	16	2000	353.0	353.0	32.0
ISO7741FDBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO7741FDBQRG4	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7741FDBQRG4	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7741FDWR	SOIC	DW	16	2000	356.0	356.0	36.0
ISO7741FDWR	SOIC	DW	16	2000	356.0	356.0	45.0
ISO7741FDWR	SOIC	DW	16	2000	353.0	353.0	32.0
ISO7741FDWRG4	SOIC	DW	16	2000	353.0	353.0	32.0
ISO7741FDWRG4	SOIC	DW	16	2000	356.0	356.0	36.0
ISO7741FDWRG4	SOIC	DW	16	2000	356.0	356.0	45.0
ISO7741FSDBQR	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7742DBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO7742DWR	SOIC	DW	16	2000	353.0	353.0	32.0
ISO7742DWR	SOIC	DW	16	2000	356.0	356.0	36.0
ISO7742DWR	SOIC	DW	16	2000	356.0	356.0	45.0
ISO7742FDBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO7742FDWR	SOIC	DW	16	2000	353.0	353.0	32.0
ISO7742FDWR	SOIC	DW	16	2000	356.0	356.0	45.0
ISO7742FSDBQR	SSOP	DBQ	16	2500	350.0	350.0	43.0

GENERIC PACKAGE VIEW

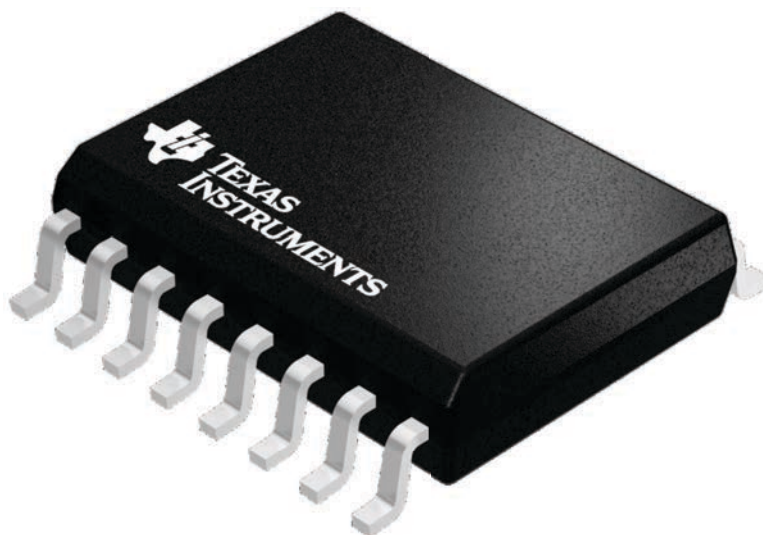
DW 16

SOIC - 2.65 mm max height

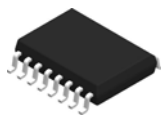
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

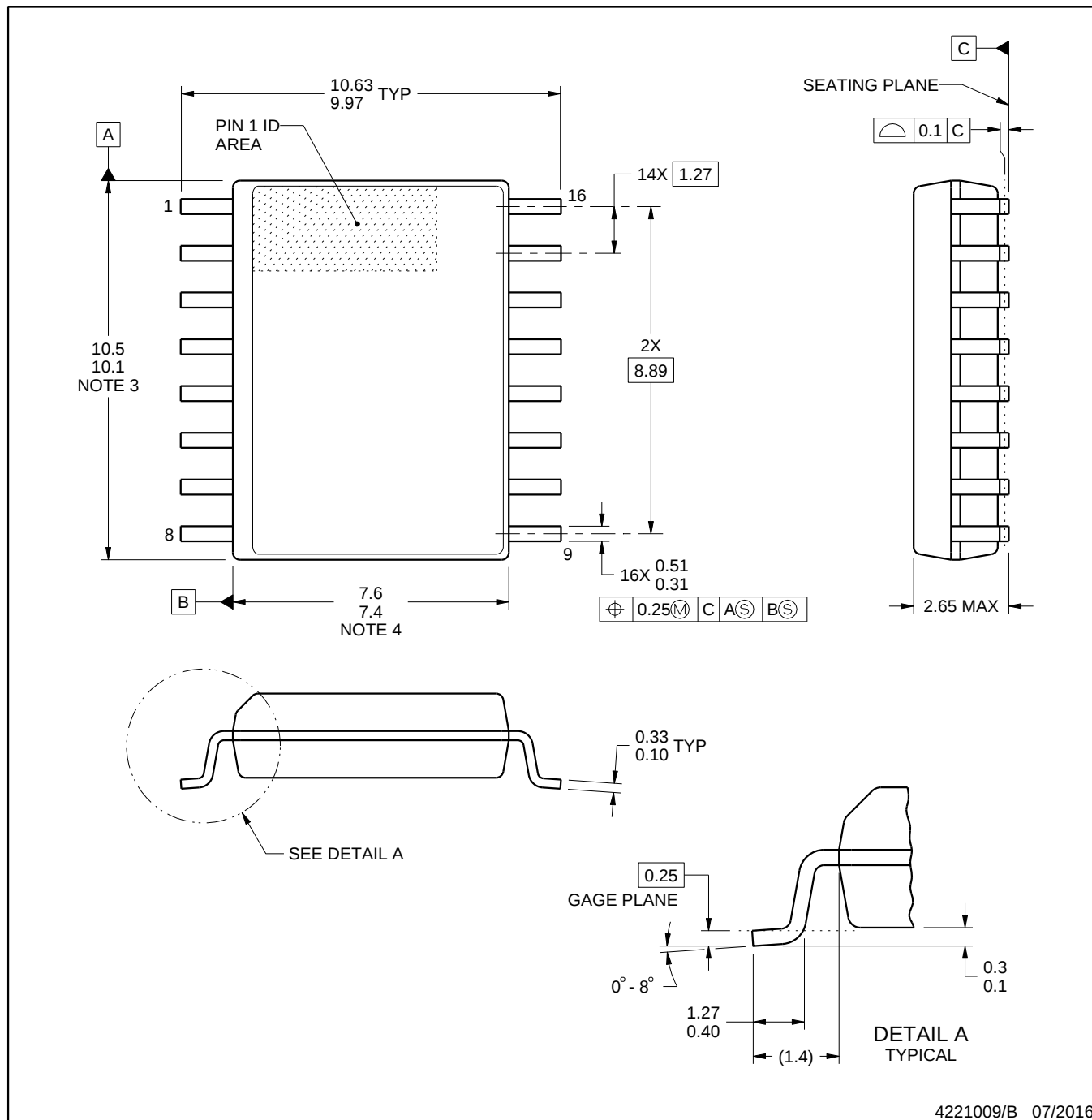


DW0016B

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4221009/B 07/2016

NOTES:

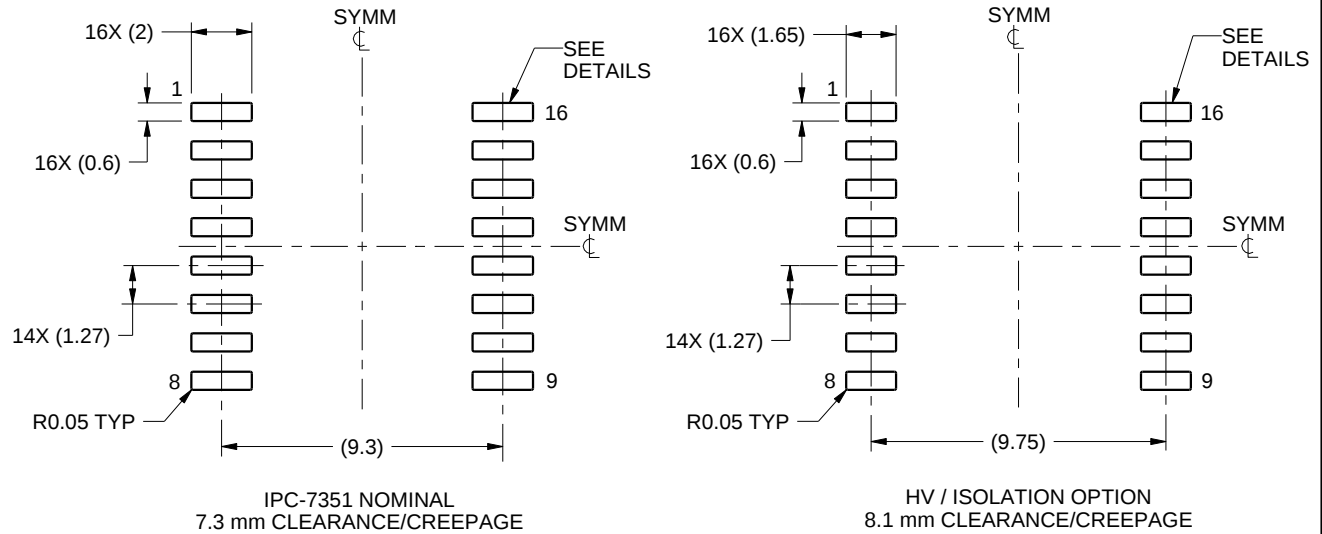
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

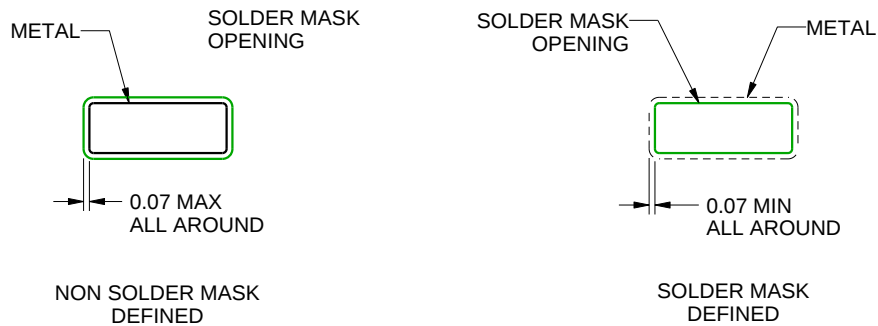
DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

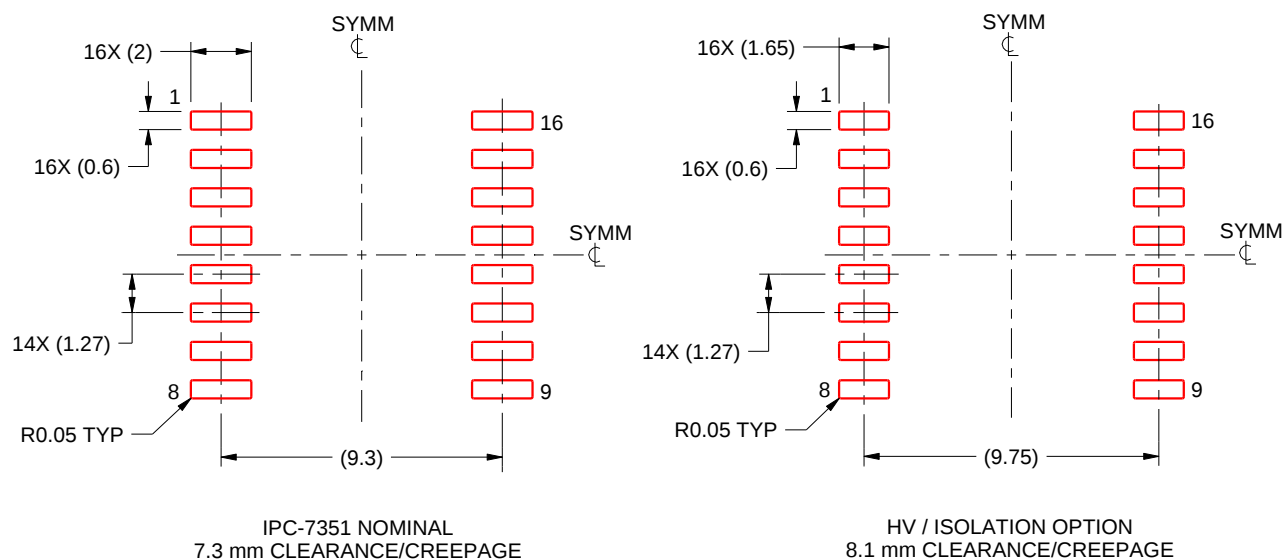
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC

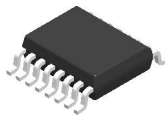


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

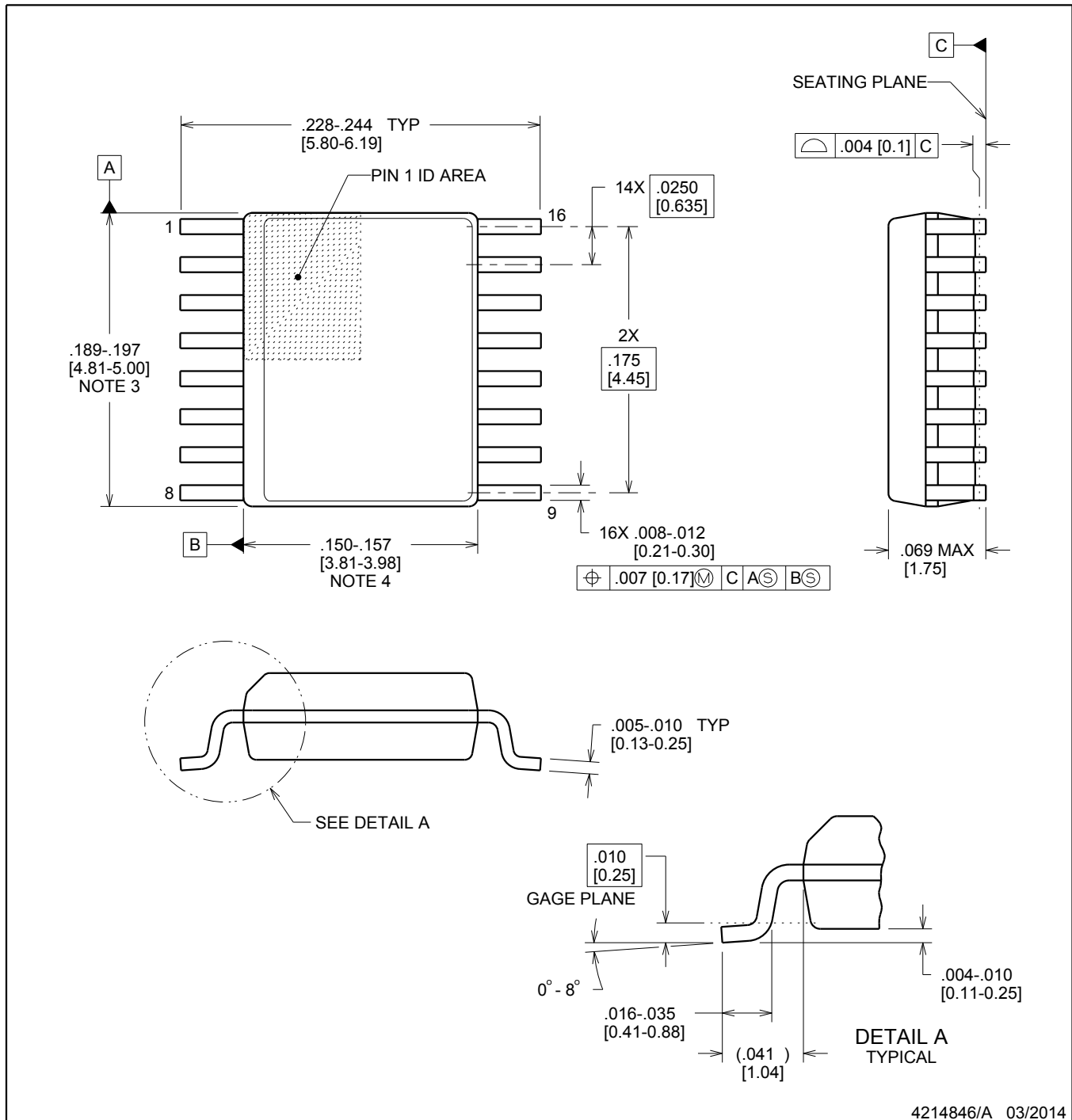


DBQ0016A

PACKAGE OUTLINE

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



NOTES:

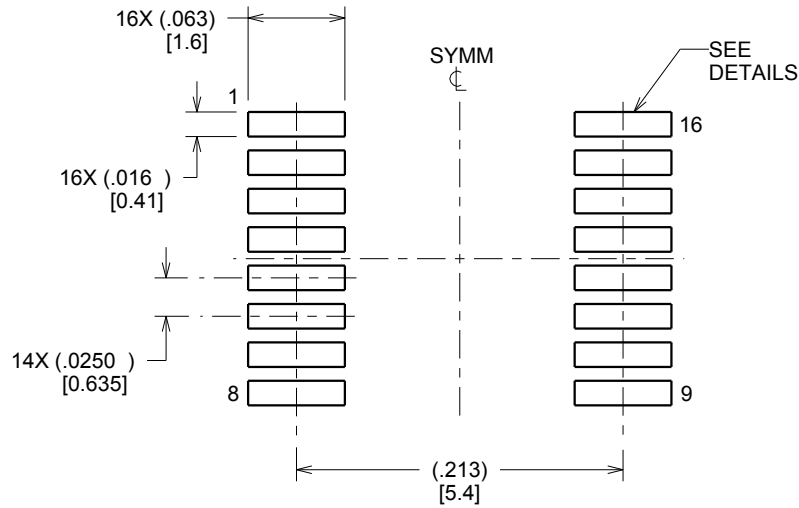
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

EXAMPLE BOARD LAYOUT

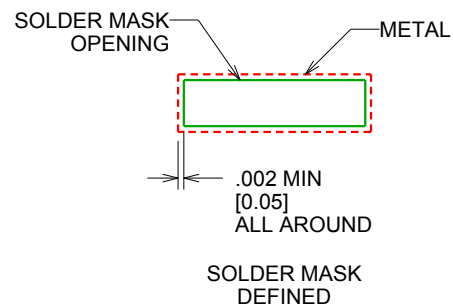
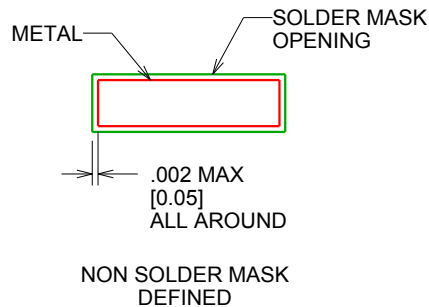
DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

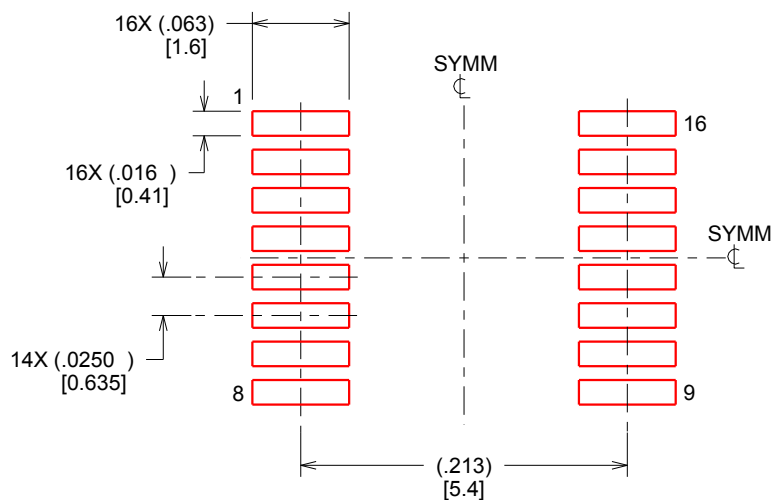
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025